



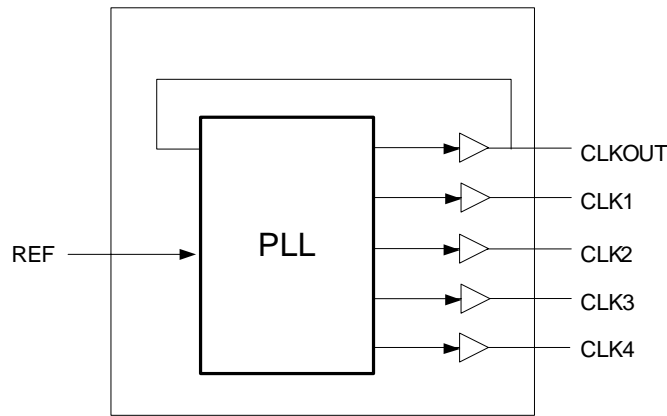
### Features

- Part of Silego's Media Timing Generator (MTG) Family
- 3.3V Supply Operation
- 5 Output Zero Delay Buffer
- Internal Feedback
- Frequency Range: 10 to 200 MHz
- Output to Output Skew: < 100ps
- Cycle-Cycle Jitter: < 80ps
- Spread-Spectrum Tracking Capability
- Pb-Free 8-Pin SOIC

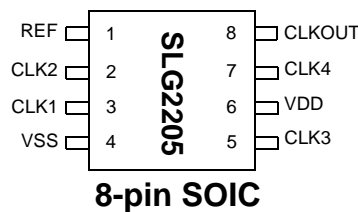
### Output Summary

- 5 - Single-Ended Clock Outputs @ 3.3V

### Block Diagram



### Pin Configuration





## General Description

The SLG2205 device features a High Performance PLL that supports 5 clock outputs. The High Performance PLL has been designed with a power supply rejection circuitry which limits the output frequency variation across the supply voltage. Included on the SLG2205 is the ability to track a spread spectrum input.

## Pin Description

Pin #	Pin Name	Type	Pin Description
1	REF	I	Reference clock input with weak pull-down resistor.
2	CLK2	O, SE	Clock output with weak pull-down resistor
3	CLK1	O, SE	Clock output with weak pull-down resistor
4	VSS	GND	Ground for outputs.
5	CLK3	O, SE	Clock output with weak pull-down resistor
6	VDD	PWR	Power supply.
7	CLK4	O, SE	Clock output with weak pull-down resistor
8	CLKOUT	O, SE	Clock output with weak pull-down resistor

**Absolute Maximum Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage		-0.5	4.6	V
V <sub>IN</sub>	Input Voltage	Relative to VSS	-0.5	V <sub>DD</sub> + 0.5	V
T <sub>S</sub>	Storage Temperature	Non-Functional	-65	+150	°C
ESD <sub>HBM</sub>	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	--	V
MSL	Moisture Sensitivity Level	8-Pin SOIC		1	

**Recommended Operating Conditions**

Parameter	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.0	--	3.6	V
T <sub>A</sub>	Ambient Temperature	-40	--	85	°C
C <sub>LOAD</sub>	Maximum Load Capacitance	--	--	25	pF

**DC Specifications**

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operating Voltage		3.0	3.3	3.6	V
V <sub>OH</sub>	Output High Voltage (SE)	I <sub>oh</sub> = -12mA (High Drive)/ -8mA (Regular Drive)	2.4	--	--	V
V <sub>OL</sub>	Output Low Voltage (SE)	I <sub>ol</sub> = +12mA (High Drive)/ +8mA (Regular Drive)	--	--	0.4	V
V <sub>IH</sub>	Input High Voltage	Input CMOS levels	2.0	--	V <sub>DD</sub> +0.2	V
V <sub>IL</sub>	Input Low Voltage	Input CMOS levels	V <sub>SS</sub> -0.3	--	0.8	V
I <sub>dd_3.3V</sub>	Operating Supply Current	F <sub>REF</sub> = 66 MHz, C <sub>LOAD</sub> = 0 pF	--	--	30	mA
I <sub>IH</sub>	Input High Current	V <sub>IH</sub> = V <sub>DD</sub>	--	--	125	μA
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V	--	--	50	μA
C <sub>IN</sub>	Input Capacitance	Input CMOS Pins	--	--	7	pF
T <sub>PU</sub>	Power-up Time	Power ramps must be monotonic.	--	--	1	ms



## Clock Timing Specifications<sup>(1)</sup>

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{DD} = 3.0\text{V}$  to  $3.6\text{V}$ , unless otherwise stated.

Parameter	Description	Conditions	Min.	Max.	Unit
$F_{OUT}$	Output Frequency	$C_{LOAD} = 25\text{pF}$	20	250	MHz
$PLL_{BW}$	PLL Bandwidth		1	3	MHz
$T_{CCJITTER}$	Cycle-Cycle Jitter	$F_{OUT} = 66.6\text{MHz}$ . All outputs equal load.	--	80	ps
$T_{Edge\ Rate}$	Rising Edge Rate	Measured from 20% to 80% of $V_{DD}$ in test board, 0.8V to 2.0V in system. $C_{LOAD} = 25\text{pF}$ . See Figure 1.	--	1.5	ns
$T_{Edge\ Rate}$	Falling Edge Rate	Measured from 80% to 20% of $V_{DD}$ in test board, 2.0V to 0.8V in system. $C_{LOAD} = 25\text{pF}$ . See Figure 1.	--	1.5	ns
$T_{ccjitter}$	Cycle to Cycle Jitter	Measured with respect to 1.5V.	--	80	ps
Duty Cycle	Duty Cycle	$C_{LOAD} = 25\text{pF}$ , $F_{OUT} = 66.6\text{MHz}$ . Measured at $V_{DD}/2$ . See Figure 2.	45	55	%
$T_{SKEW}$	Output to Output Skew	All outputs equal load. See Figure 3	--	100	ps

### NOTE:

1. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.

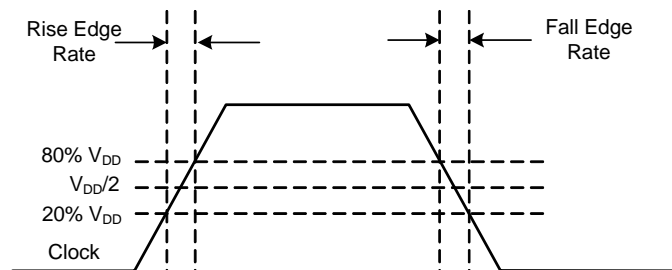


Figure 1.  $T_{RISE}/T_{FALL}$ .

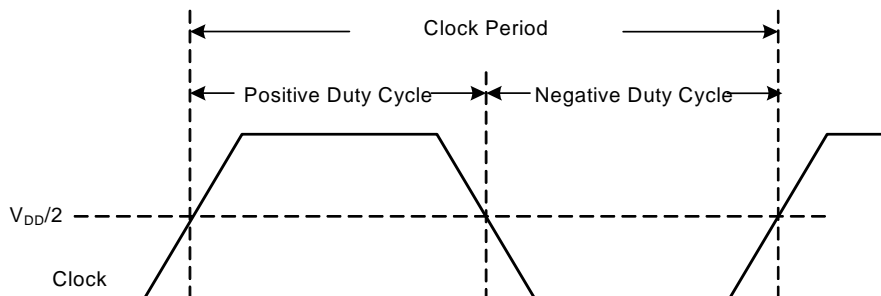


Figure 2. Duty Cycle.

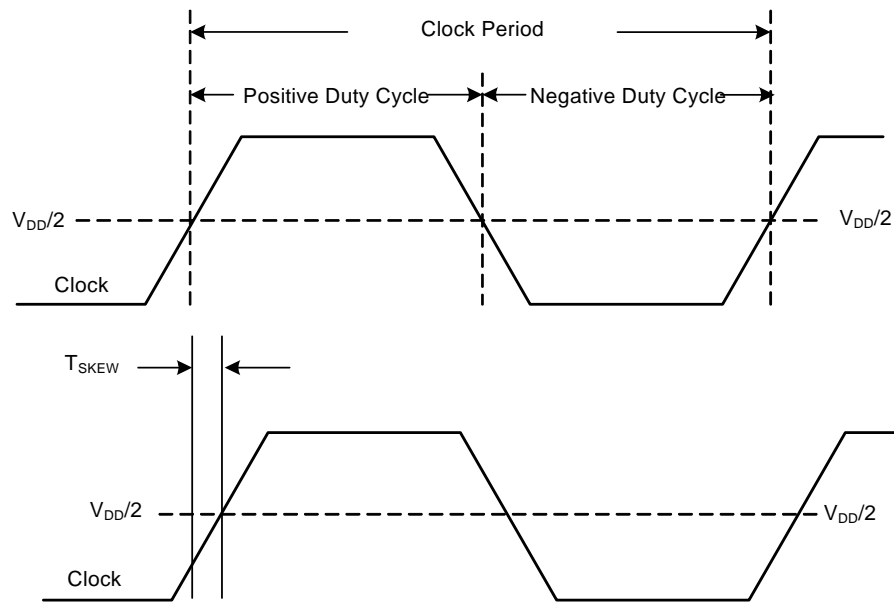


Figure 3. Output to Output Skew.

### Output Buffer

The SLG2205 contains a variable slew rate output that does not rely on increased drive strength (increased current) when driving additional loads. This is an advantage because the slew-rate can be maintained without over-and-undershoot problems while maintaining the same driver impedance  $Z_d$ .

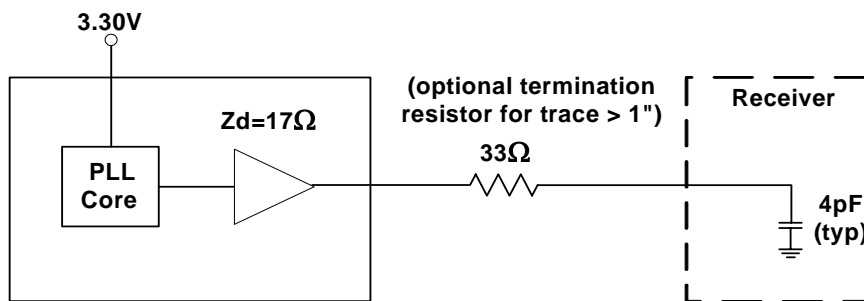


Figure 4. Output Buffer.

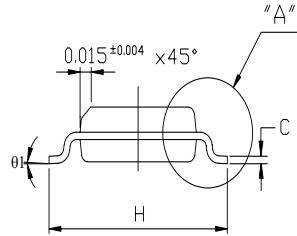
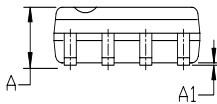
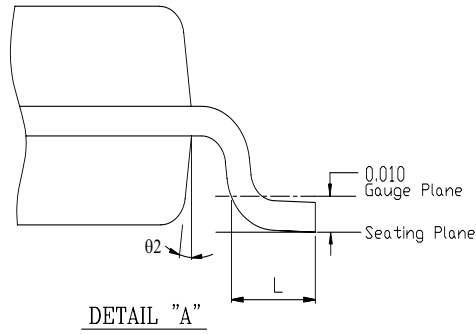
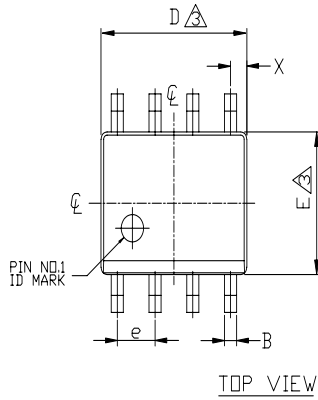
### Ordering Information

Part Number	Drive	Type	Production Flow
SLG2205	Regular	8-pin SOIC	Industrial, -40°C to 80°C
SLG2205H	High	8-pin SOIC	Industrial, -40°C to 80°C

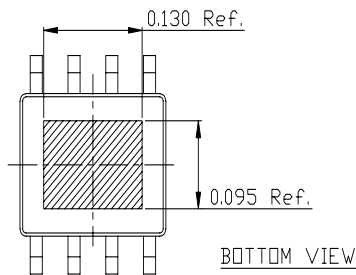


**Package Drawing and Dimensions**

**8 Lead SOIC Package**



SYMBOL	8 SOIC	
	MIN	MAX
A	0.054	0.068
A1	0.001	0.004
B	0.014	0.019
D	0.189	0.196
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.020	0.040
X	0.0215 REF	
θ1	0°	8°
θ2	7° BSC	



NOTE :

1. TOP PACKAGE SURFACE TO BE MATTE FINISH VDI 24~27.
2. BOTTOM PACKAGE SURFACE TO BE MATTE FINISH VDI 8~11.
3. DIMENSION ARE EXCLUSIVE MOLD FLASH AND GATE BURR.
4. FOOT LENGTH MEASURING IS BASED ON THE GAUGE PLANE METHOD.