



Features

- Supports ATI RS6xx (AMD K8) chipset family
- Ideal for both desktop and mobile application
- High PPM accuracy SRC outputs for PCI Express interfaces
- -0.5% Spread Spectrum support for EMI reduction
- CLK_REQ# inputs to support SRC clock power management
- 3.3 Volt Power Supply
- 56 Pin TSSOP Package

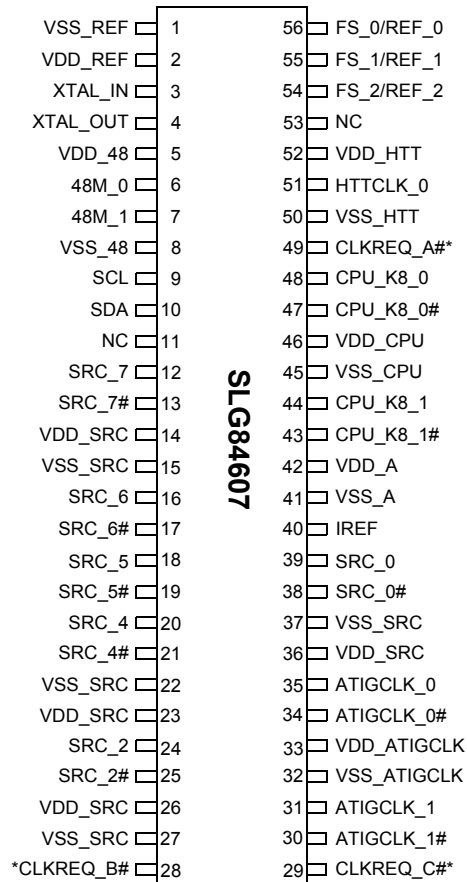
Output Summary

- 2 - AMD K8 CPU clock outputs
- 6 - differential Serial Reference Clock (SRC) clock outputs @ 0.7V
- 2 - differential ATI Graphic clock (SRC) clock outputs @ 0.7V
- 1 - HyperTransport 66.6MHz clock output @ 3.3V
- 2 - single-ended 48MHz clock output @ 3.3V
- 3 - single-ended 14.318MHz clock output @ 3.3V

Table 1. Frequency Select Table (FS_2:0)

FS_2	FS_1	FS_0	CPU (MHz)	HT-TCLK (MHz)	SRC (MHz)	ATIG-CLK (MHz)	USB (MHz)
0	0	0	Hi-Z	Hi-Z	100.0	100.0	48.0
0	0	1	REF	REF	100.0	100.0	48.0
0	1	0	230.0	76.7	100.0	100.0	48.0
0	1	1	240.0	80.0	100.0	100.0	48.0
1	0	0	100.0	66.6	100.0	100.0	48.0
1	0	1	133.3	66.6	100.0	100.0	48.0
1	1	0	166.6	66.6	100.0	100.0	48.0
1	1	1	200.0	66.6	100.0	100.0	48.0

Pin Configuration



56-pin TSSOP

Note: Signals with "*" have internal pull-up resistors

Other brands and names may be claimed as the property of others



Pin Description

Pin #	Name	Type	Description
1	VSS_REF	GND	Ground for outputs.
2	VDD_REF	PWR	3.3V power supply for outputs.
3	XTAL_IN	I	14.318MHz crystal input.
4	XTAL_OUT	O, SE	14.318MHz crystal output.
5	VDD_48	PWR	3.3V power supply for outputs.
6	48M_0	O, SE	USB clock output.
7	48M_1	O, SE	USB clock output.
8	VSS_48	GND	Ground for outputs.
9	SCL	I	Serial Interface bus clock input.
10	SDA	I/O, SE	Serial Interface bus data input and output.
11	NC	I	No connect.
12	SRC_7	O, DIF	Differential Serial Reference Clock output.
13	SRC_7#	O, DIF	Differential Serial Reference Clock output.
14	VDD_SRC	PWR	3.3V power supply for outputs.
15	VSS_SRC	GND	Ground for outputs.
16	SRC_6	O, DIF	Differential Serial Reference Clock output.
17	SRC_6#	O, DIF	Differential Serial Reference Clock output.
18	SRC_5	O, DIF	Differential Serial Reference Clock output.
19	SRC_5#	O, DIF	Differential Serial Reference Clock output.
20	SRC_4	O, DIF	Differential Serial Reference Clock output.
21	SRC_4#	O, DIF	Differential Serial Reference Clock output.
22	VSS_SRC	GND	Ground for outputs.
23	VDD_SRC	PWR	3.3V power supply for outputs.
24	SRC_2	O, DIF	Differential Serial Reference Clock output.
25	SRC_2#	O, DIF	Differential Serial Reference Clock output.
26	VDD_SRC	PWR	3.3V power supply for outputs.
27	VSS_SRC	GND	Ground for outputs.
28	CLKREQ_B#	I	CLKREQ# input.
29	CLKREQ_C#	I	CLKREQ# input.
30	ATIGCLK_1#	O, DIF	Differential ATI graphic clock output.
31	ATIGCLK_1	O, DIF	Differential ATI graphic clock output.
32	VSS_ATIGCLK	GND	Ground for outputs.
33	VDD_ATIGCLK	PWR	3.3V power supply for outputs.
34	ATIGCLK_0#	O, DIF	Differential ATI graphic clock output.
35	ATIGCLK_0	O, DIF	Differential ATI graphic clock output.
36	VDD_SRC	PWR	3.3V power supply for outputs.

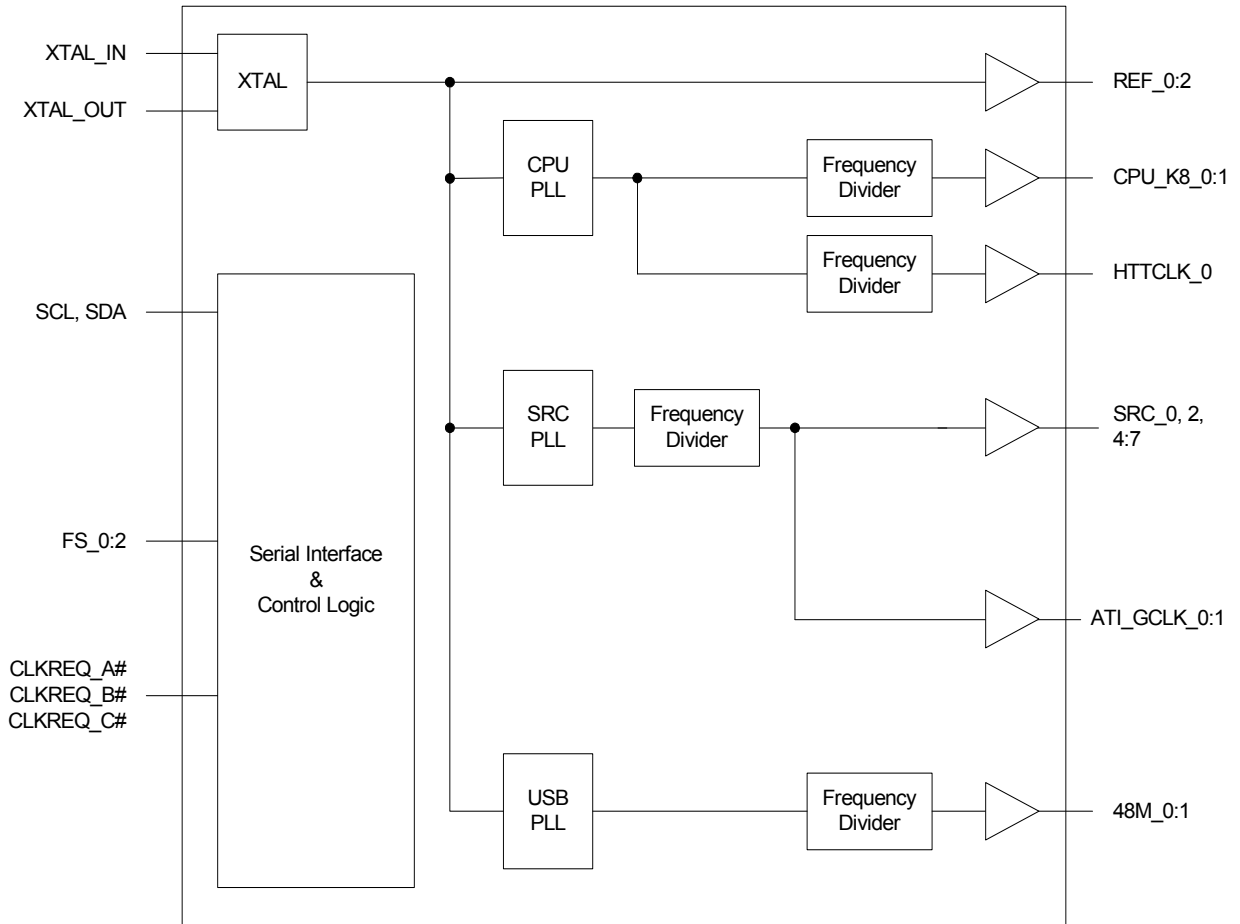


Pin Description (continued)

Pin #	Name	Type	Description
37	VSS_SRC	GND	Ground for outputs.
38	SRC_0#	O, DIF	Differential Serial Reference Clock output.
39	SRC_0	O, DIF	Differential Serial Reference Clock output.
40	IREF	I	A precision resistor is attached to this pin, which is connected to the internal current reference.
41	VSS_A	GND	Ground for PLL.
42	VDD_A	PWR	3.3V power supply for PLL.
43	CPU_K8_1#	O, SE	K8 CPU Clock output.
44	CPU_K8_1	O, SE	K8 CPU Clock output.
45	VSS_CPU	GND	Ground for outputs.
46	VDD_CPU	PWR	3.3V power supply for outputs.
47	CPU_K8_0#	O, SE	K8 CPU Clock output.
48	CPU_K8_0	O, SE	K8 CPU Clock output.
49	CLKREQ_A#	I	CLKREQ# input.
50	VSS_HTT	GND	Ground for outputs.
51	HTTCLK_0	O, SE	66.6MHz output clock
52	VDD_HTT	PWR	3.3V power supply for outputs.
53	NC	I	No connect.
54	FS_2/REF_2	I/O, SE	14.318 reference clock output. Frequency Select input to determine CPU output frequency.
55	FS_1/REF_1	I/O, SE	14.318 reference clock output. Frequency Select input to determine CPU output frequency.
56	FS_0/REF_0	I/O, SE	14.318 reference clock output. Frequency Select input to determine CPU output frequency.



Block Diagram





Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 2*. The slave receiver address is 11010010 (D2h).

Table 2. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit '00000000' stands for block operation	11:18	Command Code - 8 Bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		Data bytes from slave/Acknowledge
		Data byte N from slave - 8 bits
		Not Acknowledge
		Stop



Table 3. Byte Read and Byte Write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxx' stands for byte operationbit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxx' stands for byte operationbit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte 0 - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop



Control Register Summary

Control Register 0

Bit	Type	Description/Function	Power up condition
7	RW	Frequency Select Source 0 = HW (FS input latched value) 1 = SW Frequency Table	0
6	RW	Spread Spectrum Enable for ATIGCLK 0 = Disabled 1 = Enabled	0
5	RW	Spread Spectrum Enable for SRC 0 = Disabled 1 = Enabled	0
4	RW	Spread Spectrum Enable for CPU 0 = Disabled 1 = Enabled	0
3	RW	Reserved	0
2:0	RW	SW Frequency Select Please refer to Frequency Selection Table for details Power up condition for bit[2:0] are the latched input value of FS_2:0	xxx

Control Register 1

Bit	Type	Description/Function	Power up condition
7	RW	48M_1 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	48M_0 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	REF_2 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	REF_1 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	REF_0 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	HTTCLK_0 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	CPU_K8_1 Output Enabled 0 = Disabled 1 = Enabled	1
0	RW	CPU_K8_0 Output Enabled 0 = Disabled 1 = Enabled	1



Control Register 2

Bit	Type	Description/Function	Power up condition
7	RW	ATIGCLK_3 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	ATIGCLK_2 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	ATIGCLK_1 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	ATIGCLK_0 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	SRC_4/CLKREQ_B# control 0 = Disabled 1 = Enabled	0
2	RW	SRC_3/CLKREQ_B# control 0 = Disabled 1 = Enabled	0
1	RW	SRC_2/CLKREQ_B# control 0 = Disabled 1 = Enabled	0
0	RW	ATIGCLK_3/CLKREQ_B# control 0 = Disabled 1 = Enabled	0

Control Register 3

Bit	Type	Description/Function	Power up condition
7	RW	SRC_7 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	SRC_6 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	SRC_5 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	SRC_4 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	SRC_3 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	SRC_2 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	SRC_1 Output Enabled 0 = Disabled 1 = Enabled	1



Control Register 3 (continued)

Bit	Type	Description/Function	Power up condition
0	RW	SRC_0 Output Enabled 0 = Disabled 1 = Enabled	1

Control Register 4

Bit	Type	Description/Function	Power up condition
7	RW	SRC_7/CLKREQ_A# control 0 = Disabled 1 = Enabled	0
6	RW	SRC_6/CLKREQ_A# control 0 = Disabled 1 = Enabled	0
5	RW	SRC_5/CLKREQ_A# control 0 = Disabled 1 = Enabled	0
4	RW	SRC_1/CLKREQ_C# control 0 = Disabled 1 = Enabled	0
3	RW	ATIGCLK_2/CLKREQ_C# control 0 = Disabled 1 = Enabled	0
2	RW	ATIGCLK_1/CLKREQ_C# control 0 = Disabled 1 = Enabled	0
1	RW	ATIGCLK_0/CLKREQ_C# control 0 = Disabled 1 = Enabled	0
0	RW	SRC_0/CLKREQ_C# control 0 = Disabled 1 = Enabled	0

Control Register 5

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	00000000

Control Register 6

Bit	Type	Description/Function	Power up condition
7:0	RW	Device ID	01100010

Control Register 7

Bit	Type	Description/Function	Power up condition
7	R	Revision ID bit 3	0
6	R	Revision ID bit 2	0



Control Register 7 (continued)

Bit	Type	Description/Function	Power up condition
5	R	Revision ID bit 1	0
4	R	Revision ID bit 0	0
3	R	Vendor ID bit 3	0
2	R	Vendor ID bit 2	1
1	R	Vendor ID bit 1	1
0	R	Vendor ID bit 0	0

Control Register 8

Bit	Type	Description/Function	Power up condition
7:6	RW	Reserved	00
5:0	RW	Byte count register for block read operation Note: The default value is 9. To read more than 9 bytes, system BIOS needs to change this register to the number of bytes it intends to read.	001001

Control Register 9

Bit	Type	Description/Function	Power up condition
7	RW	REF_2 clock drive strength control 0 = Normal 1 = High	1
6	RW	48M_1 clock drive strength control 0 = Normal 1 = High	1
5	RW	48M_0 clock drive strength control 0 = Normal 1 = High	1
4	RW	Reserved	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

Control Register 10

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	REF_1 clock drive strength control 0 = Normal 1 = High	1
5	RW	REF_0 clock drive strength control 0 = Normal 1 = High	1
4:0	RW	Reserved	00000



Control Register 11 to 28 (Reserved)

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	0



Crystal Recommendations

The SLG84607 requires a **Parallel Resonance Crystal**. Substituting a series resonance crystal will cause the SLG84607 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 4. Crystal Recommendations.

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Cut Accuracy (max.)	Temp Stability (max.)	Aging (max.)
14.31818MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	35ppm	30ppm	5ppm

Absolute Maximum Ratings

Storage Temperature: -65°C to + 150°C

Supply Voltage (VDDA): -0.5 to 4.6V

Supply Voltage (VDD): -0.5 to 4.6V

3.3V Input Voltage: -0.5 to 4.6V

Operating Temperature (Ambient): 0°C to +70°C

ESD Protection (Min): 2000V

Lead Frame Material (for Green package): Sn/Bi

Reflow Temperature (for Green package): 260°C (10sec)

DC Electrical Characteristics

Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDDA	3.3V Core Supply Voltage	3.3V±5%	3.135		3.465	V
VDD	3.3V I/O Supply Voltage	3.3V±5%	3.135		3.465	V
Vih	3.3V Input High Voltage	VDD	2.0		VDD+0.3	V
Vil	3.3V Input Low Voltage		VSS-0.3		0.8	V
Vih_FS	3.3V Input High Voltage	VDD	0.7		VDD+0.3	V
Vil_FS	3.3V Input Low Voltage		VSS-0.3		0.35	V
Voh	3.3V Output High Voltage	Ioh = -1mA	2.4			V
Vol	3.3V Output Low Voltage	Iol = 1mA			0.4	V
Iil	Input Leakage Current	0 < Vin < VDD	-5		+5	uA
Cin	Input Pin Capacitance		3		5	pF
Cxtal	Xtal Pin Capacitance		3		5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Idd_ON	Operating Supply Current	VDD = 3.465V All static inputs = VDD or VSS			500	mA



AC Electrical Characteristics

Differential Outputs (CPU) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Trise	Rise edge rate	2	10	V/ns	Measured at CPU test load. 0V +/- 400mV (differential measurement)
Tfall	Fall edge rate	2	10	V/ns	Measured at CPU test load. 0V +/- 400mV (differential measurement)
Vdiff	Differential Voltage (single ended)	0.40	2.30	V	Measured at CPU test load (single ended measurement)
Δ Vdiff	Change in Vdiff_dc magnitude	-150	+150	mV	Measured at CPU test load (single ended measurement)
Vcm	Common mode voltage	1.05	1.45	V	Measured at CPU test load (single ended measurement)
Δ Vcm	Change in common mode voltage	-200	+200	mV	Measured at CPU test load (single ended measurement)
Tccjitter	Cycle to Cycle Jitter	0	200	ps	Measured at differential cross point
Duty Cycle	Duty Cycle	45	55	%	
Tja	Accumulated jitter	-1000	1000	ps	Measured using JIT2 software package with a Tek7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50ps Sample duration = 10us
Tfs	Frequency stabilization from power up	0	3	ms	Measured from full supply voltage
Ron	Output impedance	15	55	V	Average value during switching transition. Use for determining series termination value.
Tskew	Pin-to-Pin Skew		200	ps	

Differential Outputs (ATI_GCLK, SRC) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tab	Absolute Min/Max Period (100, SSC disabled)	9.872001	10.12800	ns	
Tab	Absolute Min/Max Period (100, SSC enabled)	9.872001	10.17827	ns	
Trise	Rise Time	175	700	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Tfall	Fall Time	175	700	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Δ Trise	Rise Time Variation		125	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Δ Tfall	Fall Time Variation		125	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Rise/Fall matching	Rise and Fall Time Matching		20	%	$2 * (Tr - Tf) / (Tr + Tf)$
Vhigh	Voltage High (typ 0.70v)	660	850	mV	Vhigh is defined as the statistical average "high" value as obtained by using the oscilloscope Vhigh Math function
Vlow	Voltage Low (typ 0.0v)	-150		mV	Vhigh is defined as the statistical average "high" value as obtained by using the oscilloscope Vhigh Math function
Vcross Absolute	Absolute Crossing Point Voltage	250	550	mV	



Differential Outputs (ATI_GCLK, SRC) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Vcross Relative	Relative Crossing Point Voltage	Calc.	Calc.	mV	For Vhigh < 0.7V, Vcross (rel) Max. = 0.550 - 0.5*(0.7 - Vhavg) For Vhigh > 0.7V, Vcross (rel) Min. = 0.250 + 0.5*(Vhavg - 0.7)
Total Δ Vcross	Total Variation of Vcross over all Edges		140	mV	It is defined as the total variation of all crossing voltages of Rising Clock and Falling Clock#.
Tccjitter	Cycle to Cycle Jitter		125	ps	
Duty Cycle	Duty Cycle	45	55	%	
Vovs	Maximum Voltage (Overshoot)		Vhigh + 0.3	V	
Vuds	Minimum Voltage (Undershoot)	-0.3		V	
Vrb	Ringback Voltage		0.2	V	
Tskew	Pin-to-Pin Skew (all SRC outputs)		250	ps	

PCI Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period (SSC disabled)	29.99100	30.00900	ns	Average period over 1 us
Tperiod	Average Period (SSC enabled)	29.99100	30.15980	ns	Average period over 1 us
Tabs	Absolute Min/Max Period (SSC disabled)	28.49100	30.50900	ns	
Tabs	Absolute Min/Max Period (SSC enabled)	28.49100	30.65980	ns	
Thigh	CLK high time	12	N/A	ns	
Tlow	CLK low time	12	N/A	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		500	ps	
Duty Cycle	Duty Cycle	45	55	%	
Tskew	Pin-to-Pin Skew		500	ps	

HTTCLK (66.6MHz) Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Thigh	CLK high time	5	N/A	ns	
Tlow	CLK low time	5	N/A	ns	
Trise	Rise Time		1.5	ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tfall	Fall Time		1.5	ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		300	ps	



HTTCLK (66.6MHz) Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Duty Cycle	Duty Cycle	45	55	%	
Tlong-term-jitter	Long term jitter		1	ns	1us sample period

USB_48 Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		100	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period	20.83125	20.83542	ns	Average period over 1 us
Tabs	Absolute Min/Max Period	20.48125	21.18542	ns	
Thigh	CLK high time	8.094	10.036	ns	
Tlow	CLK low time	7.694	9.836	ns	
Edge Rate	Rising edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		150	ps	
Duty Cycle	Duty Cycle	45	55	%	

REF Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period	69.82033	69.86224	ns	Average period over 1 us
Tabs	Absolute Min/Max Period	68.82033	70.86224	ns	
Trise	Rise Time		1.5	ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tfall	Fall Time		1.5	ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		200	ps	
Duty Cycle	Duty Cycle	45	55	%	
Tlong-term-jitter	Long term jitter		200	ps	1us sample period (LTJ performance depends on the quality of the Xtal being used)
Tlong-term-jitter	Long term jitter		300	ps	10us sample period (LTJ performance depends on the quality of the Xtal being used)



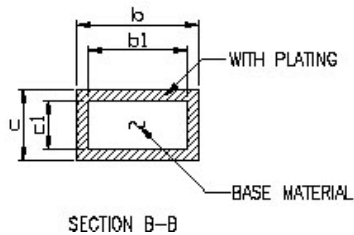
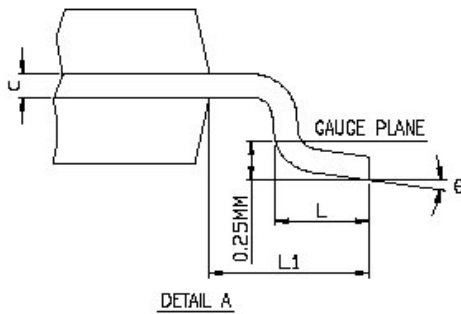
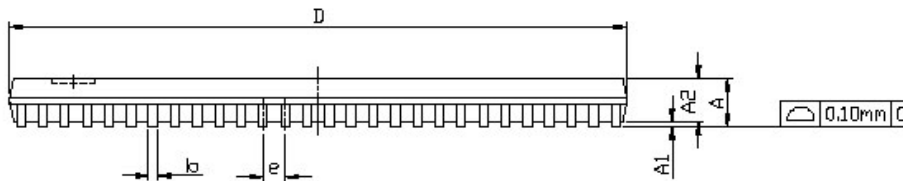
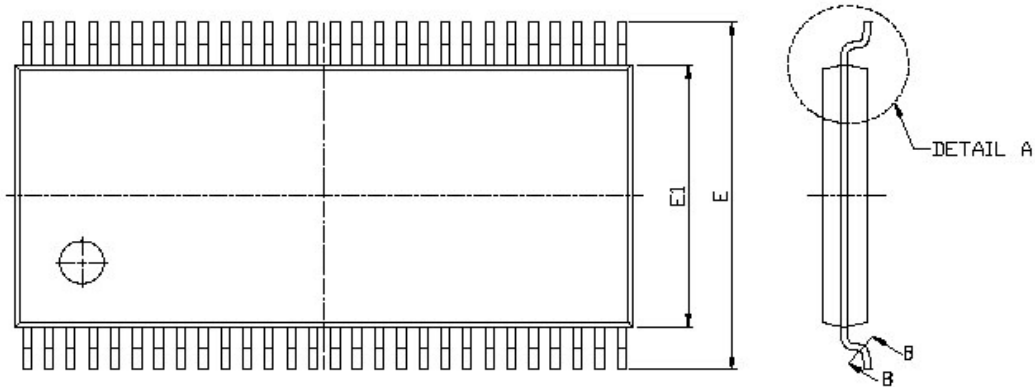
Ordering Information

Part Number	Package Type	Temperature Range
SLG84607T	56 Lead Green Package TSSOP	Commercial, 0° to 70°C
SLG84607TTR	56 Lead Green Package TSSOP - Tape and Reel	Commercial, 0° to 70°C



Package Drawing and Dimensions

56 Lead TSSOP Package



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
E	8.00	8.10	8.20	0.315	0.319	0.323
E1	6.00	6.10	6.20	0.236	0.240	0.244
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF.			0.039 REF.	
b		0.20 TYP.			0.008 TYP.	
b1		0.15 TYP.			0.006 TYP.	
c	0.09		0.20	0.004		0.008
c1	0.05	0.15	0.16	0.002		0.006
e		0.50 BSC.			0.020 BSC.	
theta	0		8	0		8

N	D (MM)			JEDEC
	MIN.	NOM	MAX.	
48	12.40	12.50	12.60	MO-153ED
56	13.90	14.00	14.10	MO-153EE
64	16.90	17.00	17.10	MO-153EF