SLG505YC256B

Clock Synthesizer for Intel PCI-Express Gen2 Chipset

Features

- SLG505YC256B is fully compliant to Intel CK505 clock specification revision 1.0
- SRC clocks compliant to PCI-Express Gen2 reference clock requirement (except SRC_0 and SRC_1)
- TME (Trusted Mode Enable) input to disable over-clocking support
- Two programmable single-ended outputs - 25MHz for LAN PHY with Wake-on-LAN support and 24.576MHz for 1394A controller
- 3.3 and low voltage (0.8V) I/O Power Supply
- 56 pin TSSOP Package

Output Summary

- 2- differential CPU clock outputs @ 0.8V
- 1 - selectable differential CPU/SRC clock output @ 0.8V
- 1 - selectable differential DOT96/SRC clock output @ 0.8V
- 6 - differential Serial Reference Clock (SRC) clock outputs @ 0.8V
- 1 - selectable differential SATA/SRC clock output @ 0.8V
- 1 - single-ended 48MHz clock output @ 3.3V
- 6 - single-ended 33MHz clock outputs @ 3.3V
- 1 - single-ended 14.318MHz clock output @ 3.3V

Table 1. Frequency Select Table (FS_C, FS_B, FS_A)

$\overline{FS\_C}$	$\overline{FS\_B}$	$\overline{FS\_A}$	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT_96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1	Reserved					

Table 2. PROG_SE_1 and PROG_SE_2 Configuration

B1b4	B1b3	B1b2	B1b1	PROG_SE_1 Pin 17	PROG_SE_2 Pin 18
0	0	0	0	SRC_1	SRC_1#
0	0	0	1	SRC_1 (LCD_CLK Stdby)	SRC_1# (LCD_CLK Stdby)
0	0	1	0	LCD_CLK (-0.5% SS)	LCD_CLK# (-0.5% SS)
0	0	1	1	LCD_CLK (-1.0% SS)	LCD_CLK# (-1.0% SS)
0	1	0	0	LCD_CLK (-1.5% SS)	LCD_CLK# (-1.5% SS)
0	1	0	1	LCD_CLK (-2.0% SS)	LCD_CLK# (-2.0% SS)
0	1	1	0	LCD_CLK (-2.5% SS)	LCD_CLK# (-2.5% SS)
0	1	1	1	Reserved	
1	0	0	0	24.576MHz	24.576MHz
1	0	0	1	24.576MHz	98.304MHz
1	0	1	0	98.304MHz	98.304MHz
1	0	1	1	27MHz	27MHz
1	1	0	0	25MHz	25MHz
1	1	0	1	25MHz (Free-running)	24.576MHz
1	1	1	0	25MHz (Free-running)	25MHz
1	1	1	1	Reserved	

Pin Configuration

Pin	Signal		Pin	Signal
1	PCI_0/CLKREQ_A#		56	SCL
2	VDD_PCI		55	SDA
3	PCI_1/CLKREQ_B#		54	REF/FS_C/TEST_SEL
4	TME/PCI_2		53	VDD_REF
5	CFG_0/PCI_3		52	XTAL_IN
6	PCI_4/SRC_5_EN		51	XTAL_OUT
7	PCIF_5/ITP_EN		50	VSS_REF
8	VSS_PCI		49	FS_B/TEST_MODE
9	VDD_48		48	CKPWRGD/PD#
10	USB/FS_A		47	VDD_CPU
11	VSS_48		46	CPU_0
12	VDD_I/O		45	CPU_0#
13	SRC_0/DOT_96		44	VSS_CPU
14	SRC_0#/DOT_96#		43	CPU_1_AMT
15	VSS_I/O		42	CPU_1_AMT#
16	VDD_PLL3		41	VDD_CPU_I/O
17	SRC_1/PROG_SE_1		40	I/O_Vout
18	SRC_1#/PROG_SE_2		39	SRC_8/CPU_ITP
19	VSS_PLL3		38	SRC_8#/CPU_ITP#
20	VDD_PLL3_I/O		37	VDD_SRC_I/O
21	SRC_2/SATA		36	SRC_7/CLKREQ_F#
22	SRC_2#/SATA#		35	SRC_7#/CLKREQ_E#
23	VSS_SRC		34	VSS_SRC
24	SRC_3/CLKREQ_C#		33	SRC_6
25	SRC_3#/CLKREQ_D#		32	SRC_6#
26	VDD_SRC_I/O		31	VDD_SRC
27	SRC_4		30	PCI_STOP#/SRC_5
28	SRC_4#		29	CPU_STOP#/SRC_5#

SLG505YC256B

56-pin TSSOP

Pin Description

Pin #	Name	Type	Description
1	PCI_0/CLKREQ_A#	I/O, SE	Configurable PCI clock output or CLKREQ input.
2	VDD_PCI	PWR	3.3V power supply for outputs.
3	PCI_1/CLKREQ_B#	I/O, SE	Configurable PCI clock output or CLKREQ input.
4	TME/PCI_2	I/O, SE	PCI clock output. TME (Trusted Mode Enabled) strap input for PLL allocation. Please refer to Table 3. for detail descriptions.
5	CFG_0/PCI_3	O, SE	PCI clock output. PLL allocation control input. Please refer to Table 3. for detail descriptions.
6	PCI_4/SRC_5_EN	I/O, SE	PCI clock output. When SRC_5_EN is sampled HIGH during CKPWRGD assertion, it will configure PCI_STOP#/SRC_5 and CPU_STOP#/SRC_5# as SRC_5 and SRC_5# respectively. When SRC_5_EN is sampled LOW, it will configure these pins as PCI_STOP# and CPU_STOP#.
7	PCIF_5/ITP_EN	I/O, SE	Free running PCI clock output. When ITP_EN input is sampled HIGH during CKPWRGD assertion, it will configure CPU_ITP/SRC_8 as CPU output.
8	VSS_PCI	GND	Ground for outputs.
9	VDD_48	PWR	3.3V power supply for outputs.
10	USB/FS_A	I/O, SE	USB clock output. Frequency Select input to determine CPU output frequency.
11	VSS_48	GND	Ground for outputs.
12	VDD_I/O	PWR	Low voltage I/O power supply for outputs.
13	SRC_0/DOT_96	O, DIF	Configurable SRC or 96 MHz DOT clock output.
14	SRC_0#/DOT_96#	O, DIF	Configurable SRC or 96 MHz DOT clock output.
15	VSS_I/O	GND	Ground for outputs.
16	VDD_PLL3	PWR	3.3V power supply for outputs.
17	SRC_1/PROG_SE_1	O, DIF/SE	Configurable SRC or Programmable SE output. SE output can be configured as 24.576MHz, 27MHz or 25MHz.
18	SRC_1#/PROG_SE_2	O, DIF/SE	Configurable SRC or Programmable SE output. SE output can be configured as 24.576MHz, 27MHz or 25MHz.
19	VSS_PLL3	GND	Ground for outputs.
20	VDD_PLL3_I/O	PWR	Low voltage I/O power supply for outputs.
21	SRC_2/SATA	O, DIF	Configurable Serial Reference clock for SATA or PCI Express device.
22	SRC_2#/SATA#	O, DIF	Configurable Serial Reference clock for SATA or PCI Express device.
23	VSS_SRC	GND	Ground for outputs.
24	SRC_3/CLKREQ_C#	I/O	Configurable differential CPU clock output or CLKREQ input.
25	SRC_3#/CLKREQ_D#	I/O	Configurable differential CPU clock output or CLKREQ input.
26	VDD_SRC_I/O	PWR	Low voltage I/O power supply for outputs.
27	SRC_4	O, DIF	Differential Serial Reference Clock output.
28	SRC_4#	O, DIF	Differential Serial Reference Clock output.
29	CPU_STOP#/SRC_5#	I/O	Configurable CPU_STOP# input or differential Serial Reference Clock output.

Pin Description (continued)

Pin #	Name	Type	Description
30	PCI_STOP#/SRC_5	I/O	Configurable PCI_STOP# input or differential Serial Reference Clock output.
31	VDD_SRC	PWR	3.3V power supply for outputs.
32	SRC_6#	O, DIF	Differential Serial Reference Clock output.
33	SRC_6	O, DIF	Differential Serial Reference Clock output.
34	VSS_SRC	GND	Ground for outputs.
35	SRC_7#/CLKREQ_E#	I/O	Configurable differential CPU clock output or CLKREQ input.
36	SRC_7/CLKREQ_F#	I/O	Configurable differential CPU clock output or CLKREQ input.
37	VDD_SRC_I/O	PWR	Low voltage I/O power supply for outputs.
38	SRC_8#/CPU_ITP#	O, DIF	Selectable differential CPU or SRC output. It will configure as CPU clock when ITP_EN is sampled HIGH. It will configure as SRC clock when ITP_EN is sampled LOW.
39	SRC_8/CPU_ITP	O, DIF	Selectable differential CPU or SRC output. It will configure as CPU clock when ITP_EN is sampled HIGH. It will configure as SRC clock when ITP_EN is sampled LOW.
40	I/O_Vout	O, SE	I/O voltage reference output.
41	VDD_CPU_I/O	PWR	Low voltage I/O power supply for outputs.
42	CPU_1_AMT#	O, DIF	Differential CPU Clock output.
43	CPU_1_AMT	O, DIF	Differential CPU Clock output.
44	VSS_CPU	GND	Ground for outputs.
45	CPU_0#	O, DIF	Differential CPU Clock output.
46	CPU_0	O, DIF	Differential CPU Clock output.
47	VDD_CPU	PWR	3.3V power supply for outputs.
48	CKPWRGD/PD#	I	CKPWRGD is a 3.3V LVTTL iput. It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs. After CKPWRGD assertion, it becomes a real time input for asserting power down (active high).
49	FS_B/TEST_MODE	I	Frequency Select input to determine CPU output frequency. When in test mode, FS_B/TEST_MODE will configure outputs to run at REF or Hi-Z. 0 = Hi-Z, 1 = REF
50	VSS_REF	GND	Ground for outputs.
51	XTAL_OUT	O, SE	14.318MHz crystal output.
52	XTAL_IN	I	14.318MHz crystal input.
53	VDD_REF	PWR	3.3V power supply for outputs.
54	REF/FS_C/TEST_SEL	I/O, SE	14.318 reference clock output. When FS_C/TEST_SEL input is pulled to 3.3V during CKPWRGD# assertion, the device will configure into TEST MODE. Refer to DC Parameters section for FS input voltage threshold. After CKPWRGD assertion, this pin will be configured as REF output.
55	SDA	I/O, SE	Serial Interface bus data input and output.
56	SCL	I	Serial Interface bus clock input.

*Note: Please do not leave unused hardware strap pin floating, please add external pull-up and pull-down resistors on the schematic.
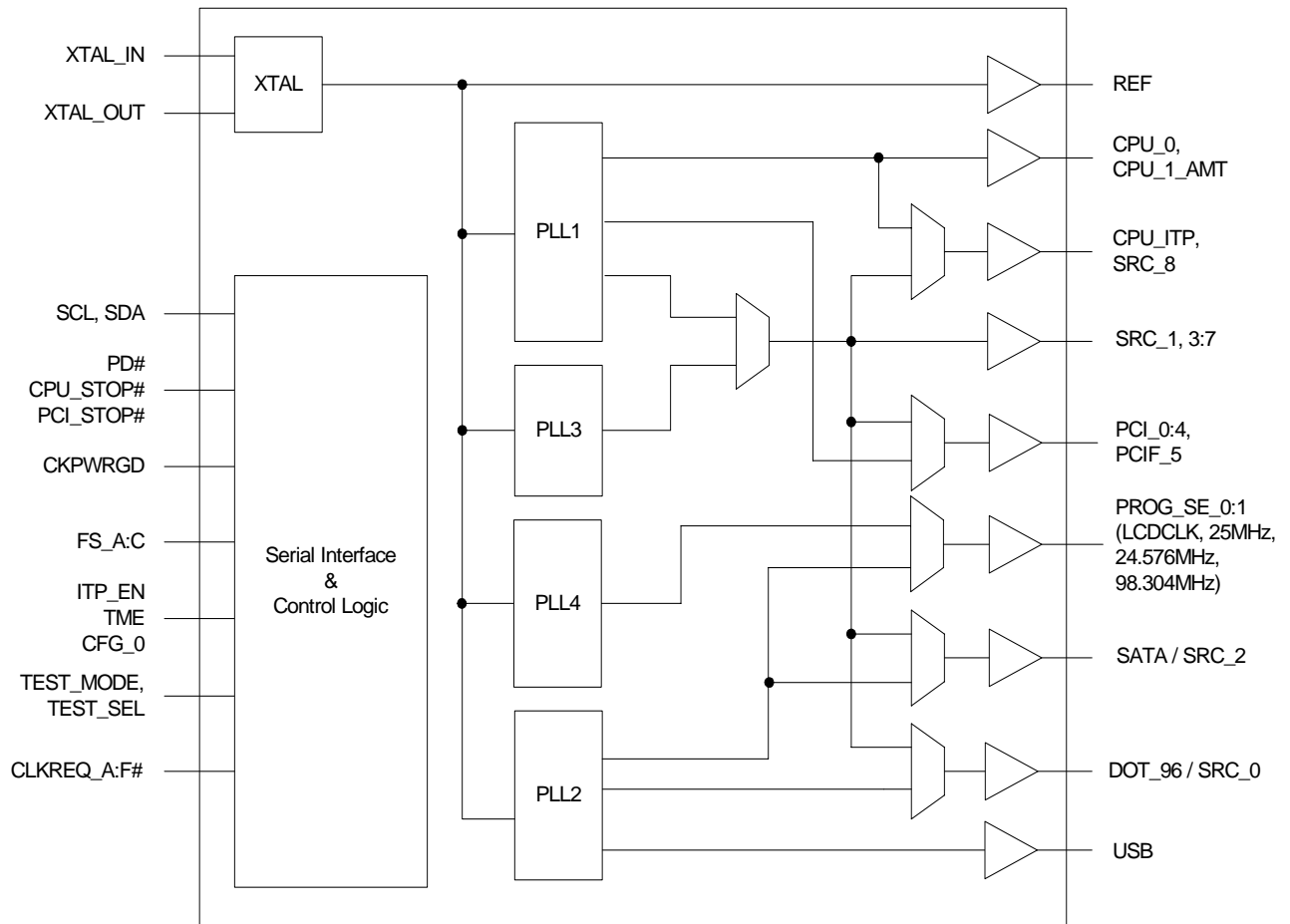
Block Diagram

Figure 1. Simplified Block Diagram

PLL Allocation & Over-clocking Control

Table 3. PLL configuration & over-clocking control (PCI_3/CFG_0 & PCI_2/TME HW strap inputs)

PCI_3/ CFG_0	PCI_2 /TME	PLL Allocation Mode	PLL1		PLL2		PLL3		PLL4		Over-clocking Support
			Outputs	SSC	Outputs	SSC	Outputs	SSC	Outputs	SSC	
Low	Low	0	CPU/SRC /PCI	Down	USB	N/A	LCDCLK	Down	OFF	N/A	Yes
Low	High	0	CPU/SRC /PCI	Down	USB	N/A	LCDCLK	Down	OFF	N/A	No
Mid	Low	1	CPU	Down	USB	N/A	SRC/PCI	Down	OFF	N/A	Yes
Mid	High	1	CPU	Down	USB	N/A	SRC/PCI	Down	OFF	N/A	No
High	Low	2	CPU	Center	USB	N/A	SRC/PCI	Down	OFF	N/A	Yes
High	High	3	CPU	Center	USB/ LAN25	N/A	SRC/PCI	Down	24.576M	OFF	Yes

Selecting N-Divider and M-Divider Value to Change CPU output Frequency

1. Select M-divider Value

      a. The M-Divider value for the desired CPU output frequency is determined by the current CPU frequency mode and Spread Spectrum mode. The following N-Divider Value Table lists the recommended M-divider value associated with each CPU frequency mode and Spread Spectrum option.

2. Select N-divider Value

      a. The N-divider value is calculated based on the following equation.

      N-divider value = ((Target Frequency - Base Frequency) / Frequency Resolution) + N-Divider Base Value

      b. The N-Divider Base Value and Frequency Resolution for the desired CPU output frequency is determined by the current CPU Frequency mode and Spread Spectrum mode, and they are listed under the following N-Divider Value Table.

      c. For example, the N-divider value for 170MHz under the "100MHz Frequency and Spread Spectrum OFF Mode" will be "755".

      755 = ((170 - 100) / 0.2237) + 442

N-Divider and M-Divider Value for Different CPU Output Frequency

Table 4. N-Divider Value Table

CPU Frequency Mode	Spread Spectrum Mode	CPU Frequency Range	Recommended M-Divider Value	N-Divider Base Value	Maximum N-Divider Value	Frequency Resolution
100MHz	OFF or Center	100 to 180	14	442	799	0.2237
133MHz	OFF or Center	133 to 240	14	442	799	0.2983
166MHz	OFF or Center	166 to 240	10	414	598	0.3977
200MHz	OFF or Center	200 to 360	14	442	799	0.4474
266MHz	OFF or Center	266 to 533[1]	14	442	887	0.5966
333MHz	OFF or Center	333 to 533	10	414	665	0.7955
400MHz	OFF or Center	400 to 720	14	442	799	0.8949
100MHz	Down	100 to 180	13	413	748	0.2386
133MHz	Down	133 to 240	13	413	748	0.3182
166MHz	Down	166 to 240	10	413	597	0.3977
200MHz	Down	200 to 360	13	413	748	0.4773
266MHz	Down	266 to 533[1]	13	413	831	0.6364
333MHz	Down	333 to 533	10	413	664	0.7955
400MHz	Down	400 to 720	13	413	748	0.9546

Note:

(1) To achieve better CPU output performance, we recommend system BIOS to change the CPU Frequency mode from 266MHz mode to 400MHz mode when the target CPU output frequency is higher than 480MHz. Changing CPU Frequency mode from 266MHz to 400MHz will change the CPU output divider from 3 to 2. As a result, it will require a lower VCO speed to generate the target CPU output frequency.

Selecting N-Divider and M-Divider Value to Change SRC output Frequency

1. Select M-divider Value

a. The M-Divider value for the desired SRC output frequency is determined by the current Spread Spectrum mode. The following N-Divider Value Table lists the recommended M-divider value associated with each Spread Spectrum option.

2. Select N-divider Value

a. The N-divider value is calculated based on the following equation.

N-divider value = ((Target Frequency - Base Frequency) / Frequency Resolution) + N-Divider Base Value

b. The N-Divider Base Value and Frequency Resolution for the desired SRC output frequency is determined by the current Spread Spectrum mode, and they are listed under the following N-Divider Value Table.

c. For example, the N-divider value for 105MHz under the "Spread Spectrum - Down Spread Mode" will be "434".

434 = ((105 - 100) / 0.2386) + 413

N-Divider and M-Divider Value for Different SRC Output Frequency

Table 5. N-Divider Value Table

Spread Spectrum Mode	SRC Frequency Range	Recommended M-Divider Value	N-Divider Base Value	Maximum N-Divider Value	Frequency Resolution
OFF or Center	100 to 120	14	442	536	0.2240
Down	100 to 120	13	413	502	0.2386

Low Voltage type "SR" differential output buffer

The CK505 utilizes a new output buffer for all differential clocks. The low power type SR buffer is a departure from the type X buffer used in previous CK410 clock generators. The type SR buffer uses efficient NMOS push-pull drivers powered off a low voltage power rail, offering a reduction in power consumption, improve edge rate performance, and cross point voltage control.
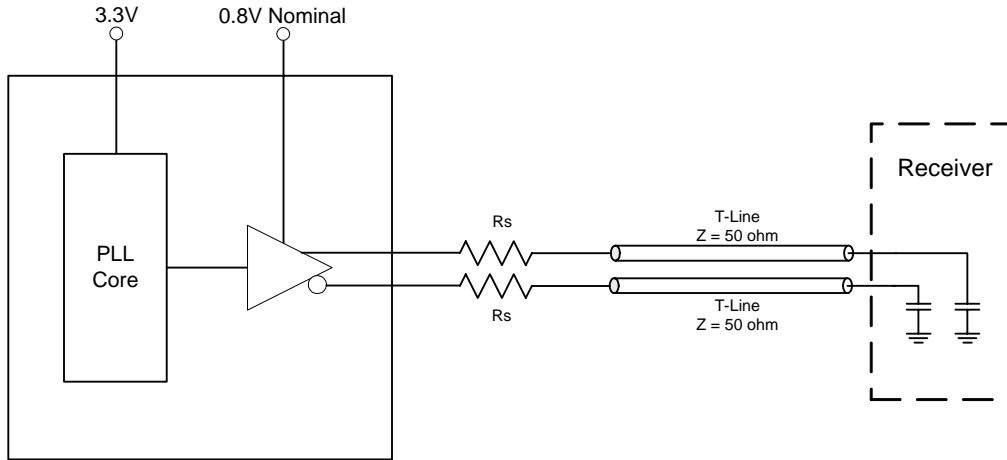
Figure 2. Type SR Differential Output Buffer

CK505 Integrated Linear Regulator and Control

The CK505 features an internal regulator to provide a low voltage reference not possible with common discrete low dropout (LDO) linear regulators. An on-die comparator is used to drive the variable IO_Vout reference voltage to an external pass element such as a common 2N3904 (SOT23) NPN transistor for platform using a Vin > +1.5V or a BSS138 MOSFET for platforms using a Vin < +1.5V to provide a low voltage power supply for the type SR buffers.
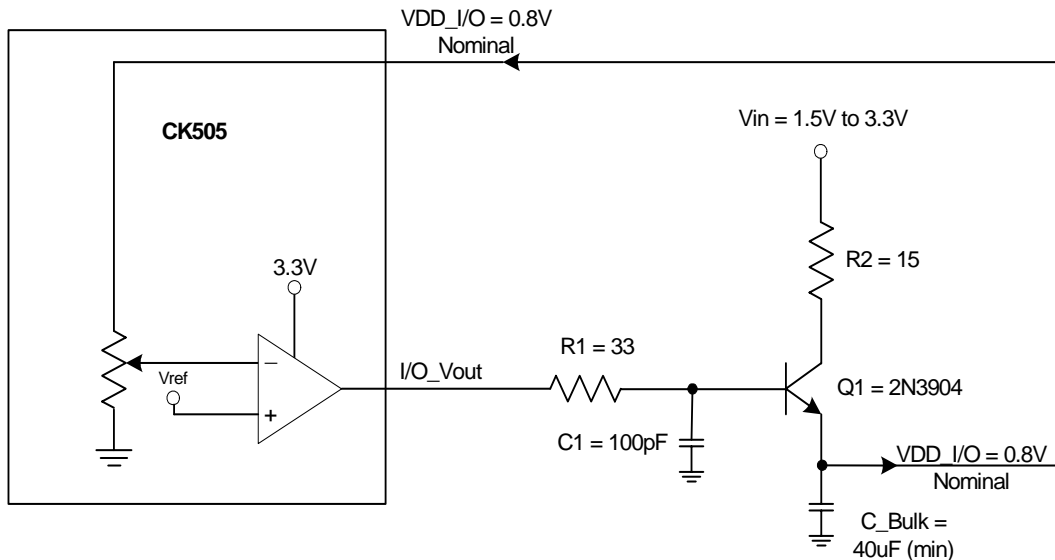
Figure 3. CK505 Integrated Linear Regulator

Output Drive Status Summary

Table 6. Output drive status for PCI_STOP#, CPU_STOP#, CR# asserted and SMBus OE disabled

		PCI_STOP# asserted	CPU_STOP# asserted	CR# asserted	SMBus OE Disabled
Single-ended clocks	**Stoppable**	Driven low	Running	Running	Driven low
	Non-Stoppable	Running	Running	Running	
Differential Clocks	**Stoppable**	Clock driven high Clock# driven low	Clock driven high Clock# driven low	Clock driven low Clock# driven low	Clock driven low or 20K pull-down Clock# driven low
	Non-Stoppable	Running	Running	Running	

Table 7. Output drive status during different power management state

	All Single-ended Clocks		All Differential Clocks, Except CPU1		CPU1	
	w/o strap	w strap	Clock	Clock#	Clock	Clock#
Latches Open State	Low	Hi-Z	Low or 20K pull-down	Low	Low or 20K pull-down	Low
Powerdown	Low	Hi-Z	Low or 20K pull-down	Low	Low or 20K pull-down	Low
M1	Low	Hi-Z	Low or 20K pull-down	Low	Running	Running
*Virtual Power Cycle to latches Open	Clock output status identical to "Latches Open State"					

*Note: Virtual Power Cycle - Latches open is accomplished by first programming the PD_RESTORE bit, byte 0, bit 0 = 0 which clears all configuration registers upon assertion of PD# low. Upon detection of PD# low, it will immediately go to "Latches Open State" and all registers and state machines will be reset as if a full power cycle has occurred.

Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 8*. The slave receiver address is 11010010 (D2h).

Table 8. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit '00000000' stands for block operation	11:18	Command Code - 8 Bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop

Table 9. Byte Read and Byte Write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Control Register Summary

Control Register 0

Bit	Type	Description/Function	Power up condition
7	R	Reflected the value of FS_C pin sampled on power up	X
6	R	Reflected the value of FS_B pin sampled on power up	X
5	R	Reflected the value of FS_A pin sampled on power up	X
4	RW	iAMT Enable 0 = Legacy Mode 1 = iAMT Mode Note: Once this bit is set, it cannot be disabled or cleared by writing a "0". This bit can only be cleared by a power-on-reset.	0
3	RW	Reserved	0
2	RW	SRC outputs PLL source 0 = PLL1 (CPU PLL) 1 = PLL3 (PCIEX PLL) Note: (1) When set to a '1', SRC_1 and other SRC outputs are sourced from PLL3 and PLL3 configuration control bits (B1b4 to B1b1) have no effect. (2) When PLL allocation mode = 0, default setting of this bit is "0" (3) When PLL allocation mode = 1, 2 or 3, default setting of this bit is "1"	Depends on TME and CFG_0 inputs
1	RW	SATA output PLL source 0 = Same source as SRC outputs 1 = PLL2 (48M PLL) and fixed at 100MHz	0
0	RW	Configuration control for power down mode 0 = Upon assertion of PD#, the clock generator will initiate a full reset. Under this condition, the clock generator will emulate a cold power on reset internally and re-latch the FS input pins 1 = Legacy PD# input mode	1

Control Register 1

Bit	Type	Description/Function	Power up condition
7	RW	SRC_0 and DOT_96 output selection 0 = SRC_0 output 1 = DOT_96 output	0
6	RW	PLL1 (CPU PLL) center spread enable 0 = down spread 1 = center spread	0
5	RW	PLL3 (PCIEX PLL) center spread enable 0 = down spread 1 = center spread Note: This bit has no impact if SRC clocks are sourced from PLL1 (CPU PLL)	0

Control Register 1 (continued)

Bit	Type	Description/Function	Power up condition
4:1	RW	PLL3 (PCIEX PLL) configuration control 0000 = PLL3 disabled, SRC_1 uses the same PLL as other SRC outputs 0001 = 100MHz 0.5% (SSC standby, PLL3 on, SRC_1 uses the same PLL as other SRC outputs) 0010 = 100MHz 0.5% (only SRC_1 sourced from PLL3) 0011 = 100MHz 1.0% (only SRC_1 sourced from PLL3) 0100 = 100MHz 1.5% (only SRC_1 sourced from PLL3) 0101 = 100MHz 2.0% (only SRC_1 sourced from PLL3) 0110 = 100MHz 2.5% (only SRC_1 sourced from PLL3) 0111 = Reserved 1000 = 24.576MHz for Prog_SE_1 & Prog_SE_2 (1394A support) 1001 = 24.576MHz for Prog_SE_1 & 98.304Mhz for Prog_SE_2 (1394A/B support) 1010 = 98.304MHz for Prog_SE_1 & Prog_SE_2 (1394B support) 1011 = 27MHz for Prog_SE_1 & Prog_SE_2 1100 = 25MHz for Prog_SE_1 & Prog_SE_2 1101 = 25MHz_F_0 (free-running) for Prog_SE_1 & 24.576MHz for Prog_SE_2 1110 = 25MHz_F_0 (free-running) for Prog_SE_1 & 25MHz_1 for Prog_SE_2 1111 = Reserved	0001
0	RW	PCI outputs PLL source 0 = PLL1 (CPU PLL) 1 = same source as SRC outputs	1

Control Register 2

Bit	Type	Description/Function	Power up condition
7	RW	REF Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	48MHz Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	PCIF_5 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	PCI_4 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	PCI_3 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	PCI_2 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	PCI_1 Output Enabled 0 = Disabled 1 = Enabled	1
0	RW	PCI_0 Output Enabled 0 = Disabled 1 = Enabled	1

Control Register 3

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	1
6	RW	Reserved	1
5	RW	Reserved	1
4	RW	SRC_8/CPU_ITP Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	SRC_7 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	SRC_6 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	SRC_5 Output Enabled 0 = Disabled 1 = Enabled	1
0	RW	SRC_4 Output Enabled 0 = Disabled 1 = Enabled	1

Control Register 4

Bit	Type	Description/Function	Power up condition
7	RW	SRC_3 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	SATA/SRC_2 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	SRC_1 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	SRC_0/DOT_96 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	CPU_1 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	CPU_0 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	PLL1 (CPU PLL) Spread Spectrum enable 0 = Disabled 1 = Enabled	1
0	RW	PLL3 (PCIEX PLL) Spread Spectrum enable 0 = Disabled 1 = Enabled Note: This bit has no impact if SRC clocks are sourced from PLL1 (CPU PLL)	1

Control Register 5

Bit	Type	Description/Function	Power up condition
7	RW	CLKREQ_A# enable 0 = Configure pin 1 as PCI_0 output 1 = Configure pin 1 as CLKREQ_A# input	0
6	RW	CLKREQ_A# mapping 0 = SRC_0 1 = SRC_2	0
5	RW	CLKREQ_B# enable 0 = Configure pin 3 as PCI_1 output 1 = Configure pin 3 as CLKREQ_B# input	0
4	RW	CLKREQ_B# mapping 0 = SRC_1 1 = SRC_4	0
3	RW	CLKREQ_C# enable 0 = Configure pin 24 as SRC_3 output 1 = Configure pin 24 as CLKREQ_C# input Note: To configure this pin as CLKREQ_C# input, SRC_3 needs to be disabled by clearing Byte[4], bit[7] to "0" before setting this bit.	0
2	RW	CLKREQ_C# mapping 0 = SRC_0 1 = SRC_2	0
1	RW	CLKREQ_D# enable 0 = Configure pin 25 as SRC_3# output 1 = Configure pin 25 as CLKREQ_D# input Note: To configure this pin as CLKREQ_D# input, SRC_3 needs to be disabled by clearing Byte[4], bit[7] to "0" before setting this bit.	0
0	RW	CLKREQ_D# mapping 0 = SRC_1 1 = SRC_4	0

Control Register 6

Bit	Type	Description/Function	Power up condition
7	RW	CLKREQ_E# enable 0 = Configure pin 35 as SRC_7# output 1 = Configure pin 35 as CLKREQ_E# input to control SRC_6 output Note: To configure this pin as CLKREQ_E# input, SRC_7 needs to be disabled by clearing Byte[3], bit[3] to "0" before setting this bit.	0
6	RW	CLKREQ_F# enable 0 = Configure pin 36 as SRC_7 output 1 = Configure pin 36 as CLKREQ_F# input to control SRC_8 output Note: To configure this pin as CLKREQ_F# input, SRC_7 needs to be disabled by clearing Byte[3], bit[3] to "0" before setting this bit.	0
5	RW	Reserved	0
4	RW	Reserved	0
3	RW	Reserved	0
2	RW	Reserved	0

Control Register 6 (continued)

Bit	Type	Description/Function	Power up condition
1	RW	PCI_STOP# control for SSCD output 0 = Free-running 1 = SSCD clock are stopped when PCI_STOP# is active	0
0	R	PCI_STOP# control for SRC outputs 0 = Free-running 1 = SRC clock are stopped when PCI_STOP# is active	0

Control Register 7

Bit	Type	Description/Function	Power up condition
7	R	Revision ID bit 3	0
6	R	Revision ID bit 2	0
5	R	Revision ID bit 1	1
4	R	Revision ID bit 0	0
3	R	Vendor ID bit 3	0
2	R	Vendor ID bit 2	1
1	R	Vendor ID bit 1	1
0	R	Vendor ID bit 0	0

Control Register 8

Bit	Type	Description/Function	Power up condition
7:4	R	Device ID 0000 = 56 pin TSSOP or SSOP 0001 = 64 pin TSSOP 0010 to 1111 = Reserved	0000
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Prog_SE_1 output enable 0 = Disabled 1 = Enabled Note: (1) When PLL allocation mode = 0, 1 or 2, the default setting of this bit is "0" (2) When PLL allocation mode = 3, the default setting of this bit is "1"	Depends on TME and CFG_0 inputs
0	RW	Prog_SE_2 output enable 0 = Disabled 1 = Enabled Note: (1) When PLL allocation mode = 0, 1 or 2, the default setting of this bit is "0" (2) When PLL allocation mode = 3, the default setting of this bit is "1"	Depends on TME and CFG_0 inputs

Control Register 9

Bit	Type	Description/Function	Power up condition
7	RW	PCI_STOP# control for PCIF_5 0 = Free-running 1 = PCIF_5 is stopped when PCI_STOP# is active	0
6	R	Trusted mode enabled input status 0 = Normal operation (full function) 1 = Trusted mode enabled (no over-clocking allowed)	*latched status of input*
5	RW	REF output drive strength control 0 = 1x (2 loads) 1 = 2x (3 loads)	1
4	RW	REF or Tristate Select for Test Mode 0 = Tristate 1 = REF	0
3	RW	Test Clock Mode Entry Control 0 = Normal operation 1 = REF or Tristate mode	0
2:0	RW	IO_VOUT control 000 = 0.3V 001 = 0.4V 010 = 0.5V 011 = 0.6V 100 = 0.7V 101 = 0.8V 110 = 0.9V 111 = 1.0V	101

Control Register 10

Bit	Type	Description/Function	Power up condition
7	R	SRC_5_EN input strap status 0 = Pins are configured as CPU_STOP# and PCI_STOP# inputs 1 = Pins are configured as SRC_5 and SRC_5# outputs.	X
6	RW	PLL3 control 0 = Disabled 1 = Enabled	1
5	RW	PLL2 control 0 = Disabled 1 = Enabled	1
4:2	RW	Reserved	000
1	RW	Allow control of CPU_1_AMT with assertion of CPU_STOP# 0 = Free Running 1 = Stopped with CPU_STOP# asserted	1
0	RW	Allow control of CPU_0 with assertion of CPU_STOP# 0 = Free Running 1 = Stopped with CPU_STOP# asserted	1

Control Register 11

Bit	Type	Description/Function	Power up condition
7:6	R	PLL allocation control 00 = Mode 0 01 = Mode 1 10 = Mode 2 11 = Mode 3 Note: Please refer to Table 3. PLL Allocation Control for the definitions of different PLL modes.	Depends on TME and CFG_0 inputs
5	RW	MS25 mode enable (Enable free-running 25MHz in power down or M1 mode) 0 = Disabled 1 = Enabled Note: (1) This bit is defined as "Reserved" when the PLL allocation is under Mode 0, 1 or 2. System BIOS should NOT enable or set this bit when the clock generated is configured as these modes. (2) Once this bit is set, it cannot be disabled or cleared by writing a "0". This bit can only be cleared by a power-on-reset. (3) When PLL allocation mode = 0, 1 or 2, the default setting of this bit is "0". (4) When PLL allocation mode = 3, the default setting of this bit is "1".	Depends on TME and CFG_0 inputs
4	RW	PLL4 control 0 = Disabled 1 = Enabled	1
3	RW	CPU_ITP output enable during M1 mode 0 = Disabled 1 = Enabled	0
2	RW	CPU_1_AMT output enable during M1 mode 0 = Disabled 1 = Enabled	1
1	R	PCI-Express Compliant Status 0 = Gen1 1 = Gen2	1
0	RW	Allow control of CPU_ITP with assertion of CPU_STOP# 0 = Free Running 1 = Stopped with CPU_STOP# asserted	1

Control Register 12

Bit	Type	Description/Function	Power up condition
7:6	RW	Reserved	00
5:0	RW	Byte count register for block read operation Note: The default value is 13. To read more than 13 bytes, system BIOS needs to change this register to the number of bytes it intends to read.	001101

Control Register 13

Bit	Type	Description/Function	Power up condition
7:2	RW	Reserved	000000

Control Register 13 (continued)

Bit	Type	Description/Function	Power up condition
1:0	RW	SRC Spread Spectrum % 00 = 0.5% 01 = 0.4% 10 = 0.3% 11 = 0.6%	00

Control Register 14 (Frequency Table Control)

Bit	Type	Description/Function	Power up condition
7	RW	Frequency Select Source 0 = HW (Latched FS inputs) 1 = SW (Output frequency controlled by the value of bit[6:2] Note: This bit will be forced to a "0" when TME is enabled.	0
6:2	RW	SW Frequency Select bit[4:0] Note: Default settings for bit[2:0] are determined by the latched value of FS_C to FS_A inputs.	00xxx
1	RW	Reserved	0
0	RW	Reserved	1

Control Register 15 (Programmable CPU PLL M-Divider Value)

Bit	Type	Description/Function	Power up condition
7:6	RW	CPU PLL N-Divider Value bit[1:0]	00
5:0	RW	CPU PLL M-Divider Value bit[5:0]	000000

Control Register 16 (Programmable CPU PLL N-Divider Value)

Bit	Type	Description/Function	Power up condition
7:0	RW	CPU PLL N-Divider Value bit[9:2]	00000000

Control Register 17 (Programmable CPU/SRC Control)

Bit	Type	Description/Function	Power up condition
7	RW	CPU PLL M/N Control 0 = Disabled 1 = Enabled Note: This bit will be forced to a "0" when TME is enabled.	0
6	RW	SRC PLL M/N Control 0 = Disabled 1 = Enabled Note: This bit will be forced to a "0" when TME is enabled.	0
5	RW	Reserved	0

Control Register 17 (Programmable CPU/SRC Control) (continued)

Bit	Type	Description/Function	Power up condition
4:0	RW	Reserved	00000

Control Register 18 (Watchdog Timer Value)

Bit	Type	Description/Function	Power up condition
7	RW	Time Base Select 0 = 293.6 msec 1 = 1.174 second	0
6:5	RW	Reserved	00
4:2	RW	Hard Alarm Watchdog Timer Value 000 = 0 x Time base (0 sec.) 001 = 4 x Time base (1.176 or 4.704 sec.) 010 = 8 x Time base (2.352 or 9.408 sec.) 011 = 12 x Time base (3.528 or 14.112 sec.) 100 = 16 x Time base (4.704 or 18.816 sec.) 101 = 20 x Time base (5.880 or 23.520 sec.) 110 = 24 x Time base (7.056 or 28.224 sec.) 111 = 28 x Time base (8.232 or 32.928 sec.)	001
1	RW	Reserved	1
0	RW	Manufacturing Test Control. Write with "0".	0

Control Register 19 (Watchdog Timer Control)

Bit	Type	Description/Function	Power up condition
7	RW	Watchdog Enable 0 = Stop Watchdog Timer 1 = Enable Watchdog. Timer will start counting down after a frequency change occurs	0
6	RW	Watchdog Hard Alarm Time-out Status 0 = No time-out occurs (read). Ignore (write) 1 = Hard Alarm time-out occurred (read). Clear Watchdog Hard Alarm time-out status bit (write)	0
5	RW	Reserved	0
4	RW	Reserved	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

Control Register 20 (Drive strength Control)

Bit	Type	Description/Function	Power up condition
7	RW	48MHz clock drive strength control 0 = Normal 1 = High	0
6	RW	Reserved	1
5	RW	Reserved	1

Control Register 20 (Drive strength Control) (continued)

Bit	Type	Description/Function	Power up condition
4	RW	PCIF_5 output drive strength 0 = Normal 1 = High	0
3	RW	Reserved	1
2	RW	PCI_3:4 output drive strength 0 = Normal 1 = High	0
1	RW	Reserved	1
0	RW	PCI_0:2 output drive strength 0 = Normal 1 = High	0

Control Register 21 (Manufacturing Test Control)

Bit	Type	Description/Function	Power up condition
7:1	RW	Reserved	000000
0	RW	Manufacturing Test Control. Write with "0".	0

Control Register 22 (Programmable SRC PLL M-Divider Value)

Bit	Type	Description/Function	Power up condition
7:6	RW	SRC PLL N-Divider Value bit[1:0]	00
5:0	RW	SRC PLL M-Divider Value bit[5:0]	000000

Control Register 23 (Programmable SRC PLL N-Divider Value)

Bit	Type	Description/Function	Power up condition
7:0	RW	SRC PLL N-Divider Value bit[9:2]	00000000

Control Register 24

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Prog_SE_1 output drive control 0 = 1x 1 = 2x	0
5	RW	Prog_SE_2 output drive control 0 = 1x 1 = 2x	0
4	RW	Reserved	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

Control Register 24 to 28 (Reserved)

Bit	Type	Description/Function	Power up condition
7:0	RW	Manufacturing Test Control. Write with "0".	0

Crystal Recommendations

The SLG505YC256B requires a **Parallel Resonance Crystal.** Substituting a series resonance crystal will cause the SLG505YC256B to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 10. Crystal Recommendations.

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Cut Accuracy (max.)	Temp Stability (max.)	Aging (max.)
14.31818MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	35ppm	30ppm	5ppm

Absolute Maximum Ratings

Max VDD Supply Voltage (VDD_3.3):.............................4.6V

Max VDD_I/O Supply Voltage (VDD_I/O): 1.5V

Max Input Voltage (Vih):...4.6V

Min Input Voltage (Vil):...-0.5V

Storage Temperature::................................ −65°C to + 150°C

Operating Temperature (Ambient, no airflow): . 0°C to +70°C

ESD Protection (Min):... 2000V

DC Electrical Characteristics

Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDD_3.3	3.3V Supply Voltage	±5%	3.135		3.465	V
Vih	Input High Voltage (SE)		2.0		VDD+0.3	V
Vil	Input Low Voltage (SE)		VSS-0.3		0.8	V
Vih_FS_Test	Input High Voltage (SE)		2.0		VDD+0.3	V
Vih_FS (FSC)	Input High Voltage (FS)		0.7		1.5	V
Vih_FS (FSA, FSB)	Input High Voltage (FS)		0.7		VDD+0.3	V
Vil_FS	Input Low Voltage (FS)		VSS-0.3		0.35	V
Vih_PCI3_CFG0	Input High Voltage 2.75 typ		2.4		VDD+0.3	V
Vim_PCI3_CFG0	Input Mid Voltage 1.65 typ)		1.3		2.0	V
Vil_PCI3_CFG0	Input Low Voltage 0.55 typ		VSS-0.3		0.90	V
Iil	Input Leakage Current	0 < Vin < VDD	-5		+5	uA
Voh	Output High Voltage (SE)	Ioh = -1mA	2.4			V
Vol	Output Low Voltage (SE)	Iol = 1mA			0.4	V
VDD_I/O	Low Voltage Differential I/O Supply Voltage		0.72		0.88	V
Cin	Input Pin Capacitance		1.5		5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Idd_3.3V	Operating Supply Current, default configuration				250	mA
Idd_IO_0.8V	Differential I/O current, all output enabled		25		80	mA
Idd_PD_3.3V	Powerdown Supply Current, 3.3V				1.0	mA
Idd_PD_0.8V	Powerdown Supply Current, 0.8V				0.1	mA
Idd_M1_3.3V	M1 Mode Supply Current, 3.3V				25	mA

Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
Idd_M1_0.8V	M1 Mode Supply Current, 0.8V				8.0	mA

AC Electrical Characteristics

Differential Outputs (CPU, SRC, DOT_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Laccurracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average CPU Period (100MHz, SSC disabled)	9.997001	10.003000	ns	Average period over 1 us
Tperiod	Average CPU Period (133MHz, SSC disabled)	7.497751	7.502251	ns	Average period over 1 us
Tperiod	Average CPU Period (166MHz, SSC disabled)	5.998201	6.001801	ns	Average period over 1 us
Tperiod	Average CPU Period (200MHz, SSC disabled)	4.998500	5.001500	ns	Average period over 1 us
Tperiod	Average CPU Period (266MHz, SSC disabled)	3.748875	3.751125	ns	Average period over 1 us
Tperiod	Average CPU Period (333MHz, SSC disabled)	2.999100	3.000900	ns	Average period over 1 us
Tperiod	Average CPU Period (400MHz, SSC disabled)	2.499250	2.500750	ns	Average period over 1 us
Tperiod	Average CPU Period (100MHz, SSC enabled)	9.997001	10.05327	ns	Average period over 1 us
Tperiod	Average CPU Period (133MHz, SSC enabled)	7.497751	7.539950	ns	Average period over 1 us
Tperiod	Average CPU Period (166MHz, SSC enabled)	5.998201	6.031960	ns	Average period over 1 us
Tperiod	Average CPU Period (200MHz, SSC enabled)	4.998500	5.026634	ns	Average period over 1 us
Tperiod	Average CPU Period (266MHz, SSC enabled)	3.748875	3.769975	ns	Average period over 1 us
Tperiod	Average CPU Period (333MHz, SSC enabled)	2.999100	3.015980	ns	Average period over 1 us
Tperiod	Average CPU Period (400MHz, SSC enabled)	2.499250	2.513317	ns	Average period over 1 us
Tperiod	Average SRC Period (100MHz, SSC disabled)	9.997001	10.003000	ns	Average period over 1 us
Tperiod	Average SRC Period (100MHz, SSC enabled)	9.997001	10.05327	ns	Average period over 1 us
Tperiod	Average DOT_96 Period (96MHz)	10.41354	10.41979	ns	Average period over 1 us
Tabs	Absolute Min/Max CPU Period (100, SSC disabled)	9.912001	10.08800	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC disabled)	7.412751	7.587251	ns	
Tabs	Absolute Min/Max CPU Period (166, SSC disabled)	5.913201	6.086801	ns	
Tabs	Absolute Min/Max CPU Period (200, SSC disabled)	4.913500	5.086500	ns	
Tabs	Absolute Min/Max CPU Period (266, SSC disabled)	3.663875	3.836125	ns	
Tabs	Absolute Min/Max CPU Period (333, SSC disabled)	2.914100	3.085900	ns	
Tabs	Absolute Min/Max CPU Period (400, SSC disabled)	2.414250	2.585750	ns	
Tabs	Absolute Min/Max CPU Period (100, SSC enabled)	9.912001	10.13827	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC enabled)	7.412751	7.624950	ns	
Tabs	Absolute Min/Max CPU Period (166, SSC enabled)	5.913201	6.116960	ns	
Tabs	Absolute Min/Max CPU Period (200, SSC enabled)	4.913500	5.111634	ns	
Tabs	Absolute Min/Max CPU Period (266, SSC enabled)	3.663875	3.854975	ns	
Tabs	Absolute Min/Max CPU Period (333, SSC enabled)	2.914100	3.100980	ns	
Tabs	Absolute Min/Max CPU Period (400, SSC enabled)	2.414250	2.598317	ns	
Tabs	Absolute Min/Max SRC Period (100, SSC disabled)	9.872001	10.12800	ns	

Differential Outputs (CPU, SRC, DOT_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Tabs	Absolute Min/Max SRC Period (100, SSC enabled)	9.872001	10.17827	ns	
Tabs	Absolute Min/Max DOT_96 Period (96MHz)	10.16354	10.66979	ns	
Slew_rise	Rising slew rate	2.5	8.0	V/ns	1. Use 'average' acquisition mode of the scope 2. Measurement taken from differential waveform 3. Slew rate measured through V_swing voltage range centered about differential zero
Slew_fall	Falling slew rate	2.5	8.0	V/ns	1. Use 'average' acquisition mode of the scope 2. Measurement taken from differential waveform 3. Slew rate measured through V_swing voltage range centered about differential zero
Slew_var	Slew rate matching		20	%	1. Use 'average' acquisition mode of the scope 2. Measurement taken from single ended waveform 3. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculation
V_swing	Differential output swing	300		mV	Measurement taken from differential waveform
V_cr	Crossing point voltage	300	550	mV	1. Measurement taken from single ended waveform 2. V_cross is defined as the voltage where Clock = Clock# 3. Only applies to the differential rising edge (i.e. Clock rising and Clock# falling)
V_cr_dlt	Variation of V_cr		140	mV	1. Measurement taken from single ended waveform 2. V_cross is defined as the voltage where Clock = Clock# 3. V_cross delta is defined as the total variation of all crossing voltages of rising Clock and falling Clock#
Tccjitter	Cycle to Cycle Jitter (CPU)		85	ps	
Tccjitter	Cycle to Cycle Jitter (SRC)		125	ps	
Tccjitter	Cycle to Cycle Jitter (DOT_96)		250	ps	
Duty Cycle	Duty Cycle	45	55	%	
Tskew	Pin-to-Pin Skew (CPU_0 & CPU_1)		100	ps	
Tskew	Pin-to-Pin Skew (CPU_2)		150	ps	
Tskew	Pin-to-Pin Skew (all SRC outputs)		TBD	ps	

PCI Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		300	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 33.333333MHz
Tperiod	Average Period (SSC disabled)	29.99100	30.00900	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tperiod	Average Period (SSC enabled, -0.5%)	29.99100	30.15980	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tabs	Absolute Min/Max Period (SSC disabled)	29.49100	30.50900	ns	
Tabs	Absolute Min/Max Period (SSC enabled, -0.5%)	29.49100	30.65980	ns	
Thigh	CLK high time	12	N/A	ns	

PCI Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Tlow	CLK low time	12	N/A	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		500	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45	55	%	Measured with respect to 1.5V
Tskew	Pin-to-Pin Skew		1000	ps	

USB_48 Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		300	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 48.000000MHz
Tperiod	Average Period	20.83125	20.83542	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tabs	Absolute Min/Max Period	20.48125	21.18542	ns	
Thigh	CLK high time	8.094	10.036	ns	
Tlow	CLK low time	7.694	9.836	ns	
Edge Rate	Rising edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		350	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45	55	%	Measured with respect to 1.5V

REF Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		300	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 14.318180MHz
Tperiod	Average Period	69.82033	69.86224	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tabs	Absolute Min/Max Period	68.82033	70.86224	ns	
Thigh	CLK high time	TBD	TBD	ns	
Tlow	CLK low time	TBD	TBD	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		1000	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45	55	%	Measured with respect to 1.5V

Measurement Points for Differential Clocks
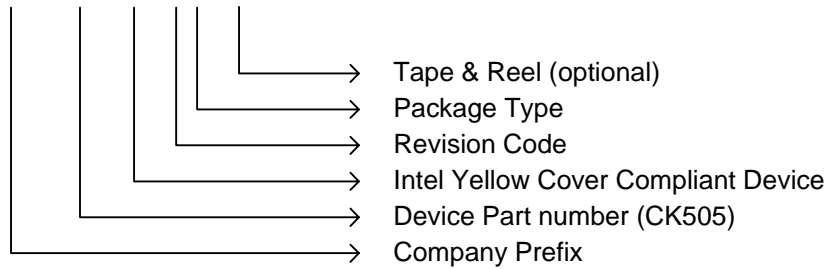
Single ended (SE) measurement waveforms

Vmax = 1.15V   Vmax = 1.15V

Clock#

Vcross max = 550mV   Vcross max = 550mV

Vcross min = 300mV   Vcross min = 300mV

Clock

Vmin = - 0.30V   Vmin = - 0.30V

Clock#

Vcross delta = 140mV   Vcross delta = 140mV

Clock

Clock#

Vcross median

Clock

Clock#

Vcross median + 75mV

Vcross median

Vcross median - 75mV

Clock

Trise

Tfall
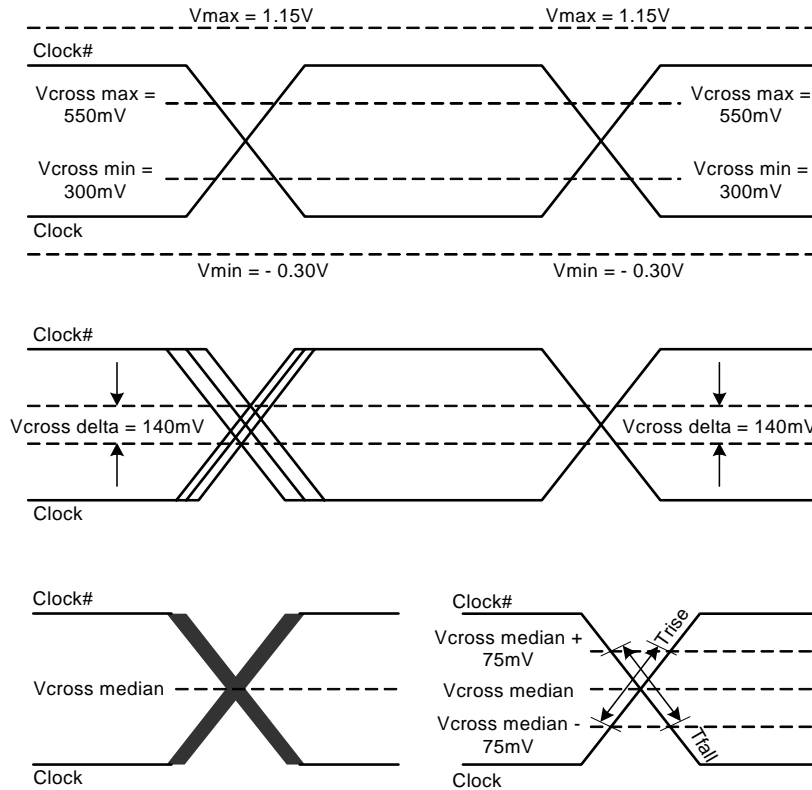
Differential (DIFF) measurement waveforms

Clock Period (Differential)

Positive Duty Cycle (Differential)   Negative Duty Cycle (Differential)

0.0V   0.0V

Clock - Clock#

Rise Edge Rate   Fall Edge Rate

Vih = +150mV   Vih = +150mV
0.0V   0.0V
Vil = +150mV   Vil = +150mV

Clock - Clock#
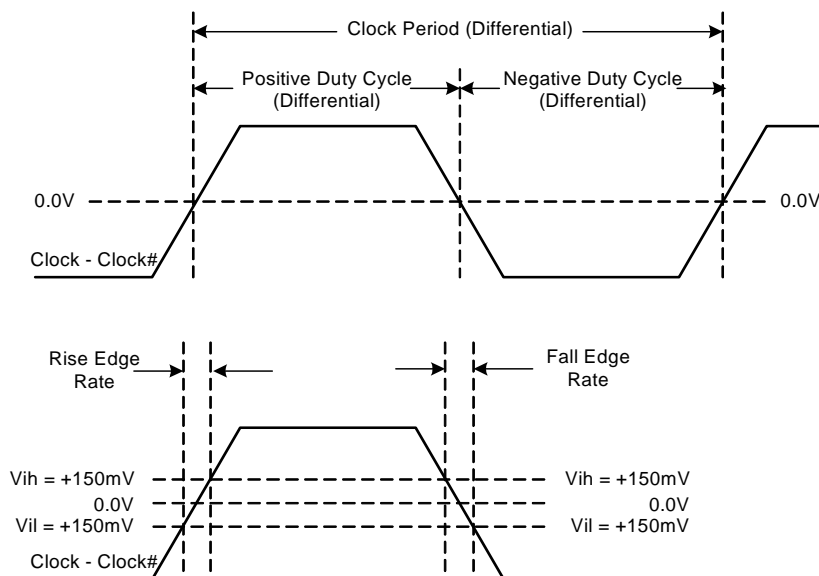
Ordering Information

SLG xxx YC y z TR

$\longrightarrow$ Tape & Reel (optional)
$\longrightarrow$ Package Type
$\longrightarrow$ Revision Code
$\longrightarrow$ Intel Yellow Cover Compliant Device
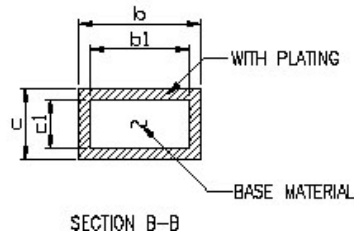$\longrightarrow$ Device Part number (CK505)
$\longrightarrow$ Company Prefix

Part Number	Package Type	Temperature Range
SLG505YC256BT	56 Lead Green Package TSSOP	Commercial, 0° to 70°C
SLG505YC256BTTR	56 Lead Green Package TSSOP - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

56 Lead TSSOP Package

DETAIL A

SECTION B-B
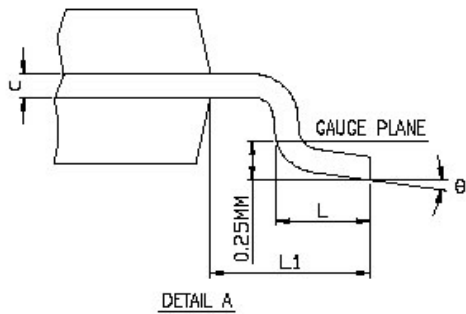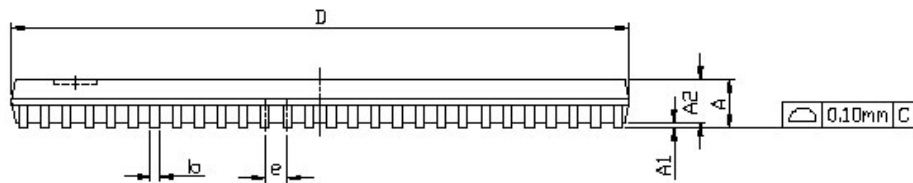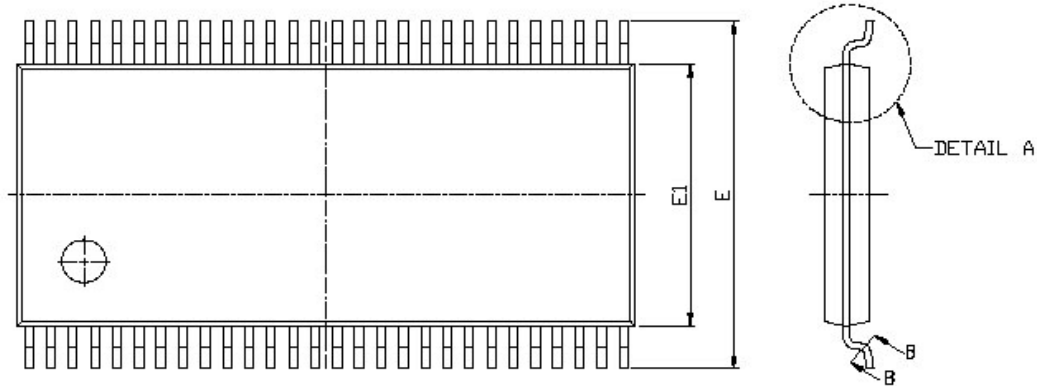
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
E	8.00	8.10	8.20	0.315	0.319	0.323
E1	6.00	6.10	6.20	0.236	0.240	0.244
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
b	0.20 TYP.			0.008 TYP.		
b1	0.15 TYP.			0.006 TYP.		
c	0.09		0.20	0.004		0.008
c1	0.05	0.15	0.16	0.002		0.006
e	0.50 BSC.			0.020 BSC.		
θ	0		8	0		8

N	D (MM)			JEDEC
	MIN.	NOM.	MAX.	
48	12.40	12.50	12.60	MO-153ED
56	13.90	14.00	14.10	MO-153EE
64	16.90	17.00	17.10	MO-153EF