



### Features

- Supports Intel PCI-Epress Chipset (CK410)
- Compliance to PCI-Express reference clock specification
- Seven selectable CPU output frequencies - 100, 133, 166, 200, 266, 333 and 400
- One CPU/SRC selectable differential clock pair
- Individual tristate control for all CPU outputs
- High PPM accuracy SRC outputs for SATA and PCI Express interfaces
- -0.5% Spread Spectrum support for EMI reduction
- 3.3 Volt Power Supply
- 56 Pin SSOP Package

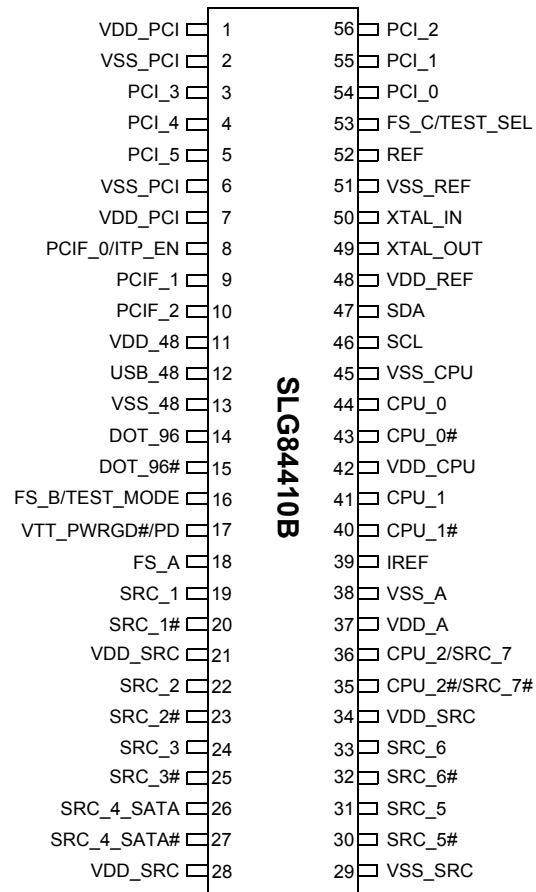
### Output Summary

- 2 - differential CPU clock outputs @ 0.7V
- 1 - selectable differential CPU/SRC clock output @ 0.7V
- 6 - differential Serial Reference Clock (SRC) clock outputs @ 0.7V
- 1 - differential 96MHz clock output @ 0.7V
- 1 - single-ended 48MHz clock output @ 3.3V
- 9- single-ended 33MHz clock outputs @ 3.3V
- 1 - single-ended 14.318MHz clock output @ 3.3V

Table 1. Frequency Select Table (FS\_C, FS\_B, FS\_A)

FS_C	FS_B	FS_A	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT_96 (MHz)	USB (MHz)	
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0	
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0	
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0	
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0	
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0	
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0	
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0	
1	1	1	Reserved						

### Pin Configuration



Other brands and names may be claimed as the property of others



## Pin Description

Pin #	Name	Type	Description
1	VDD_PCI	PWR	3.3V power supply for outputs.
2	VSS_PCI	GND	Ground for outputs.
3	PCI_3	O, SE	PCI clock output.
4	PCI_4	O, SE	PCI clock output.
5	PCI_5	O, SE	PCI clock output.
6	VSS_PCI	GND	Ground for outputs.
7	VDD_PCI	PWR	3.3V power supply for outputs.
8	PCIF_0/ITP_EN	I/O, SE	Free running PCI clock output. When ITP_EN input is sampled HIGH during VTT_PWRGD# assertion, it will configure CPU_2_ITP/SRC_7 as CPU output.
9	PCIF_1	O, SE	Free running PCI clock output.
10	PCIF_2	O, SE	Free running PCI clock output.
11	VDD_48	PWR	3.3V power supply for outputs.
12	USB_48	O, SE	USB clock output.
13	VSS_48	GND	Ground for outputs.
14	DOT_96	O, DIF	96 MHz DOT clock output.
15	DOT_96#	O, DIF	96 MHz DOT clock output.
16	FS_B/TEST_MODE	I	Frequency Select input to determine CPU output frequency. When in test mode, FS_B/TEST_MODE will configure outputs to run at Ref or Hi-Z. 0 = Hi-Z, 1 = Ref
17	VTT_PWRGD#/PD	I	VTT_PWRGD# is a 3.3V LVTTTL iput. It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs. After VTT_PWRGD# assertion, it becomes a real time input for asserting power down (active high).
18	FS_A	I	Frequency Select input to determine CPU output frequency.
19	SRC_1	O, DIF	Differential Serial Reference Clock output.
20	SRC_1#	O, DIF	Differential Serial Reference Clock output.
21	VDD_SRC	PWR	3.3V power supply for outputs.
22	SRC_2	O, DIF	Differential Serial Reference Clock output.
23	SRC_2#	O, DIF	Differential Serial Reference Clock output.
24	SRC_3	O, DIF	Differential Serial Reference Clock output.
25	SRC_3#	O, DIF	Differential Serial Reference Clock output.
26	SRC_4_SATA	O, DIF	Differential Serial Reference Clock output, recommended reference clock for SATA.
27	SRC_4_SATA#	O, DIF	Differential Serial Reference Clock output, recommended reference clock for SATA.
28	VDD_SRC	PWR	3.3V power supply for outputs.
29	VSS_SRC	GND	Ground for outputs.
30	SRC_5#	O, DIF	Differential Serial Reference Clock output.
31	SRC_5	O, DIF	Differential Serial Reference Clock output.

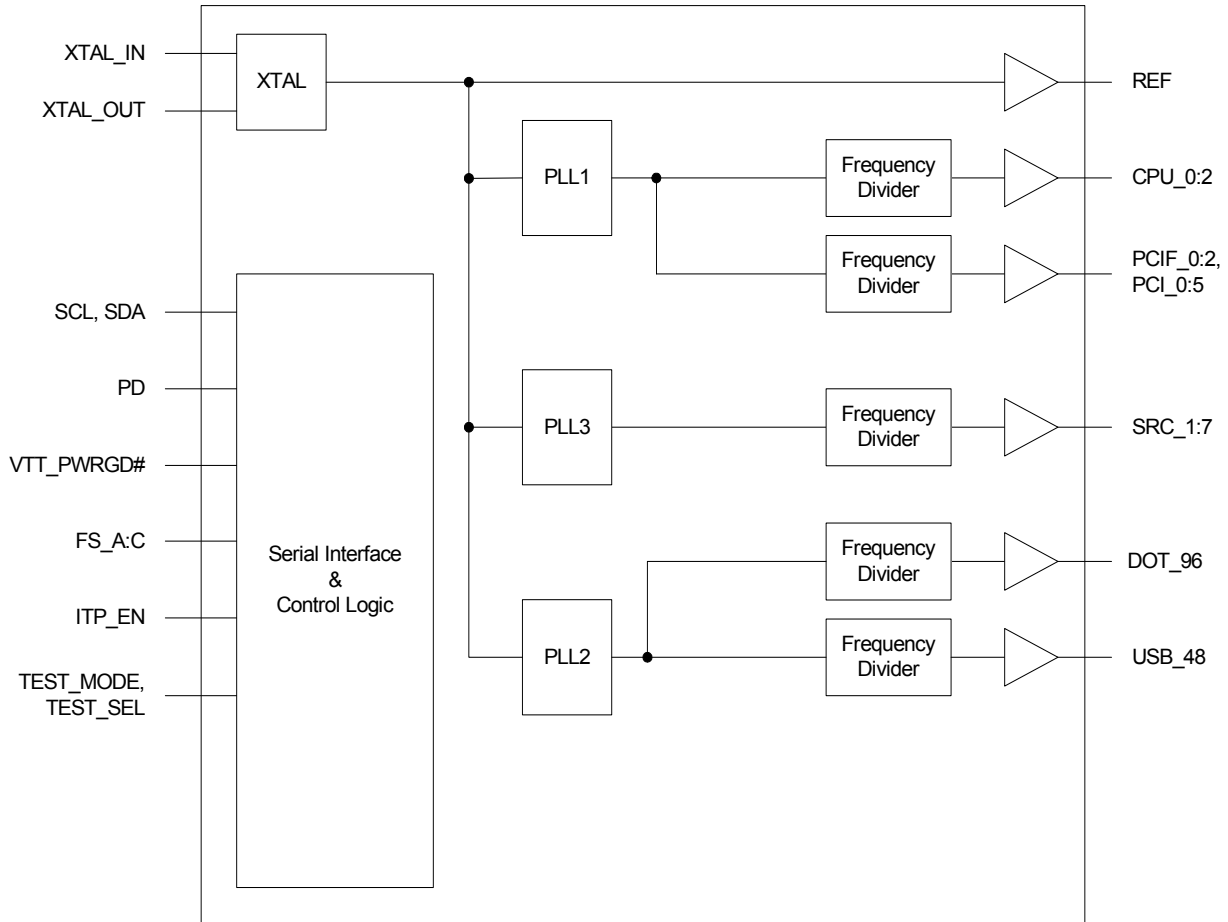


## Pin Description (continued)

Pin #	Name	Type	Description
32	SRC_6#	O, DIF	Differential Serial Reference Clock output.
33	SRC_6	O, DIF	Differential Serial Reference Clock output.
34	VDD_SRC	PWR	3.3V power supply for outputs.
35	CPU_2#/SRC_7#	O, DIF	Selectable differential CPU or SRC output. It will configure as CPU clock when ITP_EN is sampled HIGH. It will configure as SRC clock when ITP_EN is sampled LOW.
36	CPU_2/SRC_7	O, DIF	Selectable differential CPU or SRC output. It will configure as CPU clock when ITP_EN is sampled HIGH. It will configure as SRC clock when ITP_EN is sampled LOW.
37	VDD_A	PWR	3.3V power supply for PLL.
38	VSS_A	GND	Ground for PLL.
39	IREF	I	A precision resistor is attached to this pin, which is connected to the internal current reference.
40	CPU_1#	O, DIF	Differential CPU Clock output.
41	CPU_1	O, DIF	Differential CPU Clock output.
42	VDD_CPU	PWR	3.3V power supply for outputs.
43	CPU_0#	O, DIF	Differential CPU Clock output.
44	CPU_0	O, DIF	Differential CPU Clock output.
45	VSS_CPU	GND	Ground for outputs.
46	SCL	I	Serial Interface bus clock input.
47	SDA	I/O, SE	Serial Interface bus data input and output.
48	VDD_REF	PWR	3.3V power supply for outputs.
49	XTAL_OUT	O, SE	14.318MHz crystal output.
50	XTAL_IN	I	14.318MHz crystal input.
51	VSS_REF	GND	Ground for outputs.
52	REF	O, SE	14.318 reference clock output.
53	FS_C/TEST_SEL	I	Frequency Select input to determine CPU output frequency. When FS_C/TEST_SEL input is pulled to 3.3V during VTT_PWRGD# assertion, the device will configure into TEST MODE. Refer to DC Parameters section for FS input voltage threshold.
54	PCI_0	O, SE	PCI clock output.
55	PCI_1	O, SE	PCI clock output.
56	PCI_2	O, SE	PCI clock output.



## Block Diagram



## Frequency Select Pins (FS\_A, FS\_B, FS\_C)

Host clock frequency selection is achieved by applying the appropriate logic levels to Frequency Select (FS) inputs prior to VTT\_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT\_PWRGD# being sampled low by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS input values. VTT\_PWRGD# employs a one-shot functionality in that once a valid low on VTT\_PWRGD# has been sampled low, all further VTT\_PWRGD#, FS input transitions will be ignored. Please refer to Frequency Select Table for different CPU frequency configurations.

## FS\_C/TEST\_SEL Clarification

The FS\_C/TEST\_SEL input is a three level input. When voltage levels are below Vih min., the frequency selection latched on the assertion of VTT\_PWRGD# is determined by Vih\_FS and Vil\_FS thresholds in the DC Electrical Characteristics section. However, if the voltage level sampled during VTT\_PWRGD# assertion is equal or greater than Vih min., the device will invoke test clock operation. Test clock operation is used in bed of nails testing to verify clock functionality. Test clock operation can be invoked in two ways, via writing a logic "1" to the "Test Clock Mode Entry Control" bit in the control register or by placing a logic high equal or greater than Vih min. on the FS\_C/TEST\_SEL pin prior to the assertion of VTT\_PWRGD#. Once test clock operation has been invoked, the device will remain in test clock operation until power is cycled with the voltage on FS\_C/TEST\_CLK is less than Vih min.



## TEST\_SEL Hardware Control Via FS\_B/TEST\_MODE pin

Once test clock operation has been invoked, the FS\_B/TEST\_MODE pin will select between the Hi-Z and REF mode as shown in the table below using the standard low voltage  $V_{ih\_FS}$  and  $V_{il\_FS}$  thresholds.

**Table 2. Test Mode Selection Table**

TEST_MODE	CPU	SRC	PCIF/PCI	REF	DOT_96	USB_48
1	REF	REF	REF	REF	REF	REF
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

## TEST\_CLK Software Control via Control Register bits

When the “Test Clock Mode Entry Control” bit in the control register is set high, the device will invoke test clock operation. Once test clock operation has been invoked via software control, the Test\_Mode bit in the control register will select between Hi-Z and REF modes taking priority over the external FS\_B/TEST\_MODE pin.

## PD (Power Down) Clarification

The VTT\_PWRGD#/PD pin is a dual function pin. During initial power-up, the pin functions as VTT\_PWRGD#. Once VTT\_PWRGD# has been sampled low by the device, the pin assumes PD functionality. The PD pin is an asynchronous active high input used to shut off ALL clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. When PD is asserted high, all clocks are driven to a low value and held prior to turning off the VCOs and the crystal oscillator.

**Table 3. PD Functionality**

PD	CPU	CPU#	SRC	SRC#	PCIF/PCI	DOT	USB	REF
0	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal
1	Iref*2 or Float	Float	Iref*2 or Float	Float	Low	Iref*2 or Float	Low	Low

## PD# - Assertion

When PD is sampled high by two consecutive rising edges of CPU#, all single-ended outputs will be held low on their next high to low transition and differential clocks will be held high or tristated (depending on the state of the control register drive mode bit) on the next “Diff clock#” high to low transition. When the PD drive mode bit corresponding to the differential (CPU, SRC and DOT\_96) clock output of interest is programmed to ‘0’, the clock output will be held with the “Diff clock” pin driven high at 2 x Iref, and “Diff clock#” tristated. If the control register PD drive mode bit corresponding to the output of interest is programmed to ‘1’, then both the “Diff clock” and the “Diff clock#” are tristated.

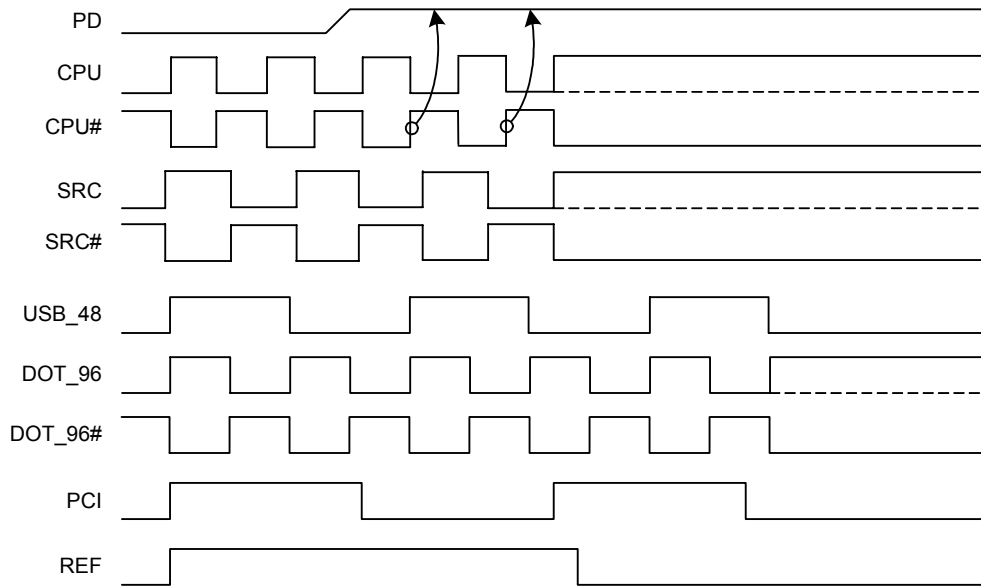


Figure 1. Power Down Assertion

**PD De-assertion**

The power-up latency is less than 1.8ms. This is the time from the de-assertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock device. All differential outputs stopped in a tristate condition resulting from power down will be driven high in less than 300us of PD de-assertion to voltage greater than 200mV.

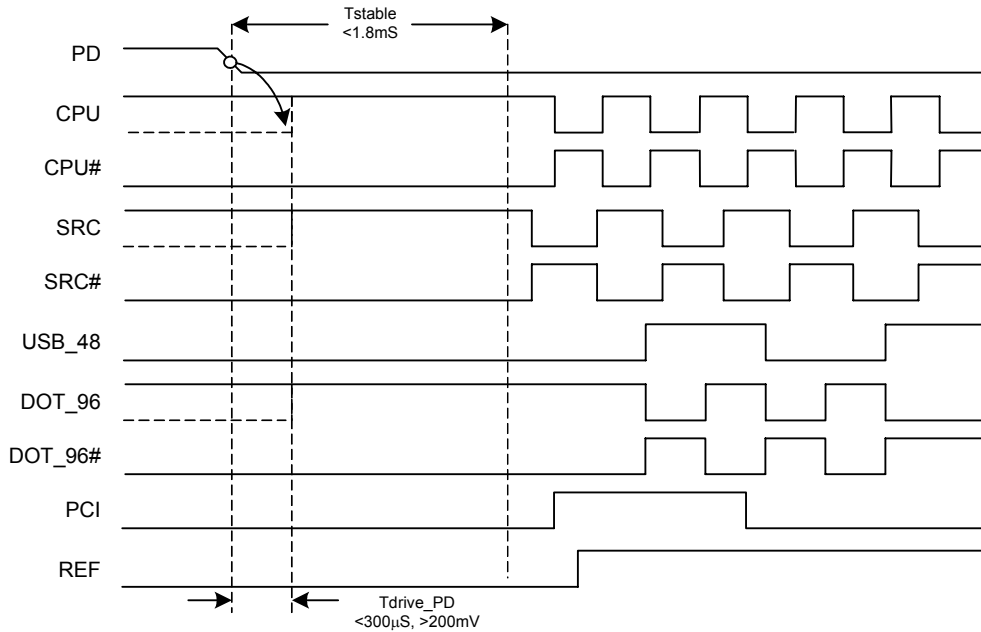
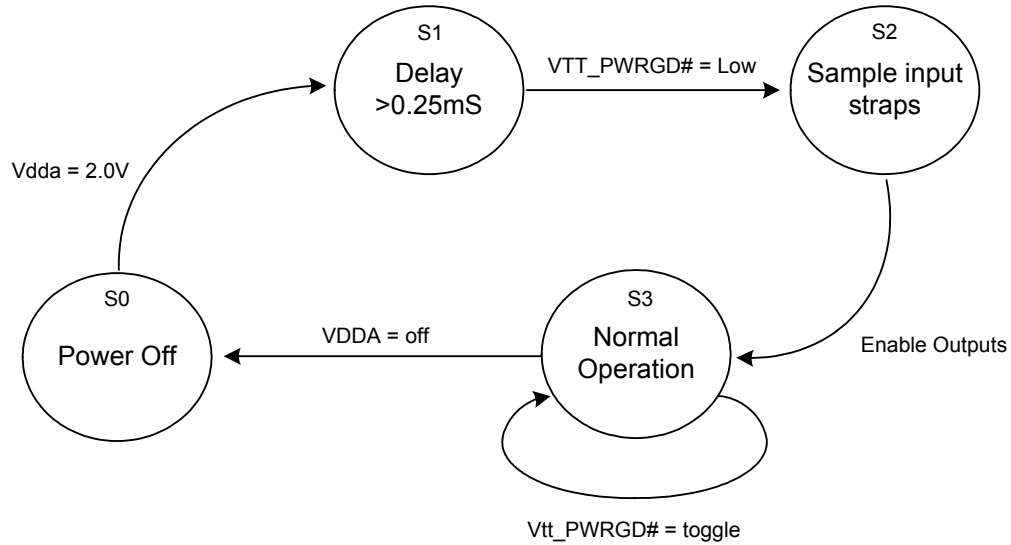


Figure 2. Power Down De-assertion



**VTT\_PWRGD# Operation**

VTT\_PWRGD# is an active low signal to indicate when the processor VTT voltage has stabilized. The significance of the VTT supply being stable is that only after VTT is stable are the processor frequency select (FS) and VID bits become valid.



**Figure 3. Clock Generator Power Up/Run State Diagram**



## Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 4*. The slave receiver address is 11010010 (D2h).

**Table 4. Block Read and Block Write protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit'00000000' stands for block operation	11:18	Command Code - 8 Bit'00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop





## Control Register Summary

### Control Register 0

Bit	Type	Description/Function	Power up condition
7	RW	CPU_2/SRC_7 Output Enable 0 = Disabled 1 = Enabled	1
6	RW	SRC_6 Output Enable 0 = Disabled 1 = Enabled	1
5	RW	SRC_5 Output Enable 0 = Disabled 1 = Enabled	1
4	RW	SRC_4 Output Enable 0 = Disabled 1 = Enabled	1
3	RW	SRC_3 Output Enable 0 = Disabled 1 = Enabled	1
2	RW	SRC_2 Output Enable 0 = Disabled 1 = Enabled	1
1	RW	SRC_1 Output Enable 0 = Disabled 1 = Enabled	1
0	RW	Reserved	1

### Control Register 1

Bit	Type	Description/Function	Power up condition
7	RW	PCIF_0 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	DOT_96 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	USB_48 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	REF Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	Reserved	1
2	RW	CPU_1 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	CPU_0 Output Enabled 0 = Disabled 1 = Enabled	1
0	RW	Spread Spectrum Enable 0 = Disabled 1 = Enabled	0



### Control Register 2

Bit	Type	Description/Function	Power up condition
7	RW	PCI_5 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	PCI_4 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	PCI_3 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	PCI_2 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	PCI_1 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	PCI_0 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	PCIF_2 Output Enabled 0 = Disabled 1 = Enabled	1
0	RW	PCIF_1 Output Enabled 0 = Disabled 1 = Enabled	1

### Control Register 3

Bit	Type	Description/Function	Power up condition
7	RW	Allow control of SRC_7 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
6	RW	Allow control of SRC_6 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
5	RW	Allow control of SRC_5 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
4	RW	Allow control of SRC_4 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
3	RW	Allow control of SRC_3 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
2	RW	Allow control of SRC_2 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
1	RW	Allow control of SRC_1 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
0	RW	Reserved	0



### Control Register 4

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	DOT_96 powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0
5	RW	Allow control of PCIF_2 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
4	RW	Allow control of PCIF_1 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
3	RW	Allow control of PCIF_0 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
2	RW	Reserved	1
1	RW	Reserved	1
0	RW	Reserved	1

### Control Register 5

Bit	Type	Description/Function	Power up condition
7	RW	SRC STOP drive mode 0 = Driven in PCI_STOP# mode 1 = Tristate	0
6	RW	Reserved	0
5	RW	Reserved	0
4	RW	Reserved	0
3	RW	SRC powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0
2	RW	CPU_2 powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0
1	RW	CPU_1 powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0
0	RW	CPU_0 powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0

### Control Register 6

Bit	Type	Description/Function	Power up condition
7	RW	REF or Tristate Select for Test Mode 0 = Tristate 1 = REF	0
6	RW	Test Clock Mode Entry Control 0 = Normal operation 1 = REF or Tristate mode	0



### Control Register 6 (continued)

Bit	Type	Description/Function	Power up condition
5	RW	Reserved	0
4	RW	REF Output Drive Strength 0 = 1x 1 = 2x	1
3	RW	PCI_STOP# control 0 = Enabled, all stoppable PCI and SRC clocks are stopped 1 = disabled	1
2	R	Reflected the value of FS_C pin sampled on power up	X
1	R	Reflected the value of FS_B pin sampled on power up	X
0	R	Reflected the value of FS_A pin sampled on power up	X

### Control Register 7

Bit	Type	Description/Function	Power up condition
7	R	Revision ID bit 3	0
6	R	Revision ID bit 2	0
5	R	Revision ID bit 1	0
4	R	Revision ID bit 0	0
3	R	Vendor ID bit 3	0
2	R	Vendor ID bit 2	1
1	R	Vendor ID bit 1	1
0	R	Vendor ID bit 0	0

### Control Register 8

Bit	Type	Description/Function	Power up condition
7	RW	Manufacturing Test Mode. Write with "0".	0
6	RW	Manufacturing Test Mode. Write with "0".	0
5	RW	Manufacturing Test Mode. Write with "0".	0
4	RW	Manufacturing Test Mode. Write with "0".	0
3	RW	Manufacturing Test Mode. Write with "0".	0
2	RW	Manufacturing Test Mode. Write with "0".	0
1	RW	Manufacturing Test Mode. Write with "0".	0
0	RW	Manufacturing Test Mode. Write with "0".	0



## Crystal Recommendations

The SLG84410B requires a **Parallel Resonance Crystal**. Substituting a series resonance crystal will cause the SLG84410B to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

**Table 5. Crystal Recommendations.**

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Cut Accuracy (max.)	Temp Stability (max.)	Aging (max.)
14.31818MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	35ppm	30ppm	5ppm

## Absolute Maximum Ratings

Storage Temperature: -65°C to +150°C

Supply Voltage (VDDA): -0.5 to 4.6V

Supply Voltage (VDD): -0.5 to 4.6V

3.3V Input Voltage: -0.5 to 4.6V

Operating Temperature (Ambient): 0°C to +70°C

ESD Protection (Min): 2000V

Lead Frame Material (for Green package): Sn/Bi

Reflow Temperature (for Green package): 260°C (10sec)

## DC Electrical Characteristics

### Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDDA	3.3V Core Supply Voltage	3.3V±5%	3.135		3.465	V
VDD	3.3V I/O Supply Voltage	3.3V±5%	3.135		3.465	V
Vih	3.3V Input High Voltage	VDD	2.0		VDD+0.3	V
Vil	3.3V Input Low Voltage		VSS-0.3		0.8	V
Vih_FS	3.3V Input High Voltage	VDD	0.7		VDD+0.3	V
Vil_FS	3.3V Input Low Voltage		VSS-0.3		0.35	V
Voh	3.3V Output High Voltage	Ioh = -1mA	2.4			V
Vol	3.3V Output Low Voltage	Iol = 1mA			0.4	V
Iil	Input Leakage Current	0 < Vin < VDD	-5		+5	uA
Cin	Input Pin Capacitance		3		5	pF
Cxtal	Xtal Pin Capacitance		3		5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Idd_ON	Operating Supply Current	VDD = 3.465V All static inputs = VDD or VSS			500	mA
Idd_PD_DR	Powerdown Current	VDD = 3.465V All static inputs = VDD or VSS All differential pairs driven			70	mA
Idd_ON_TRI	Powerdown Current	VDD = 3.465V All static inputs = VDD or VSS All differential pairs tristated			12	mA



## AC Electrical Characteristics

### Differential Outputs (CPU, SRC, DOT\_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average CPU Period (100MHz, SSC disabled)	9.997001	10.003000	ns	Average period over 1 us
Tperiod	Average CPU Period (133MHz, SSC disabled)	7.497751	7.502251	ns	Average period over 1 us
Tperiod	Average CPU Period (166MHz, SSC disabled)	5.998201	6.001801	ns	Average period over 1 us
Tperiod	Average CPU Period (200MHz, SSC disabled)	4.998500	5.001500	ns	Average period over 1 us
Tperiod	Average CPU Period (266MHz, SSC disabled)	3.748875	3.751125	ns	Average period over 1 us
Tperiod	Average CPU Period (100MHz, SSC enabled)	9.997001	10.05327	ns	Average period over 1 us
Tperiod	Average CPU Period (133MHz, SSC enabled)	7.497751	7.539950	ns	Average period over 1 us
Tperiod	Average CPU Period (166MHz, SSC enabled)	5.998201	6.031960	ns	Average period over 1 us
Tperiod	Average CPU Period (200MHz, SSC enabled)	4.998500	5.026634	ns	Average period over 1 us
Tperiod	Average CPU Period (266MHz, SSC enabled)	3.748875	3.769975	ns	Average period over 1 us
Tperiod	Average SRC Period (100MHz, SSC disabled)	9.997001	10.003000	ns	Average period over 1 us
Tperiod	Average SRC Period (100MHz, SSC enabled)	9.997001	10.05327	ns	Average period over 1 us
Tperiod	Average DOT_96 Period (96MHz)	10.41354	10.41979	ns	Average period over 1 us
Tabs	Absolute Min/Max CPU Period (100, SSC disabled)	9.912001	10.08800	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC disabled)	7.412751	7.587251	ns	
Tabs	Absolute Min/Max CPU Period (166, SSC disabled)	5.913201	6.086801	ns	
Tabs	Absolute Min/Max CPU Period (200, SSC disabled)	4.913500	5.086500	ns	
Tabs	Absolute Min/Max CPU Period (266, SSC disabled)	3.663875	3.836125	ns	
Tabs	Absolute Min/Max CPU Period (100, SSC enabled)	9.912001	10.13827	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC enabled)	7.412751	7.624950	ns	
Tabs	Absolute Min/Max CPU Period (166, SSC enabled)	5.913201	6.116960	ns	
Tabs	Absolute Min/Max CPU Period (200, SSC enabled)	4.913500	5.111634	ns	
Tabs	Absolute Min/Max CPU Period (266, SSC enabled)	3.663875	3.854975	ns	
Tabs	Absolute Min/Max SRC Period (100, SSC disabled)	9.872001	10.12800	ns	
Tabs	Absolute Min/Max SRC Period (100, SSC enabled)	9.872001	10.17827	ns	
Tabs	Absolute Min/Max DOT_96 Period (96MHz)	10.16354	10.66979	ns	
Trise	Rise Time	175	700	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Tfall	Fall Time	175	700	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Δ Trise	Rise Time Variation		125	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Δ Tfall	Fall Time Variation		125	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Rise/Fall matching	Rise and Fall Time Matching		20	%	2* (Tr-Tf)/(Tr+Tf)



### Differential Outputs (CPU, SRC, DOT\_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Vhigh	Voltage High (typ 0.70v)	660	850	mV	Vhigh is defined as the statistical average "high" value as obtained by using the oscilloscope Vhigh Math function
Vlow	Voltage Low (typ 0.0v)	-150		mV	Vhigh is defined as the statistical average "high" value as obtained by using the oscilloscope Vhigh Math function
Vcross Absolute	Absolute Crossing Point Voltage	250	550	mV	
Vcross Relative	Relative Crossing Point Voltage	Calc.	Calc.	mV	For Vhigh < 0.7V, Vcross (rel) Max. = 0.550 - 0.5*(0.7 - Vhavg) For Vhigh > 0.7V, Vcross (rel) Min. = 0.250 + 0.5*(Vhavg - 0.7)
Total Δ Vcross	Total Variation of Vcross over all Edges		140	mV	It is defined as the total variation of all crossing voltages of Rising Clock and Falling Clock#.
Tccjitter	Cycle to Cycle Jitter (CPU)		85	ps	
Tccjitter	Cycle to Cycle Jitter (SRC)		125	ps	
Tccjitter	Cycle to Cycle Jitter (DOT_96)		250	ps	
Duty Cycle	Duty Cycle	45	55	%	
Vovs	Maximum Voltage (Overshoot)		Vhigh + 0.3	V	
Vuds	Minimum Voltage (Undershoot)	-0.3		V	
Vrb	Ringback Voltage		0.2	V	
Tskew	Pin-to-Pin Skew (CPU_0 & CPU_1)		100	ps	
Tskew	Pin-to-Pin Skew (CPU_2)		150	ps	
Tskew	Pin-to-Pin Skew (all SRC outputs)		250	ps	

### PCI Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period (SSC disabled)	29.99100	30.00900	ns	Average period over 1 us
Tperiod	Average Period (SSC enabled)	29.99100	30.15980	ns	Average period over 1 us
Tabs	Absolute Min/Max Period (SSC disabled)	28.49100	30.50900	ns	
Tabs	Absolute Min/Max Period (SSC enabled)	28.49100	30.65980	ns	
Thigh	CLK high time	12	N/A	ns	
Tlow	CLK low time	12	N/A	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		500	ps	
Duty Cycle	Duty Cycle	45	55	%	
Tskew	Pin-to-Pin Skew		500	ps	



### USB\_48 Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period	20.83125	20.83542	ns	Average period over 1 us
Tab	Absolute Min/Max Period	20.48125	21.18542	ns	
Thigh	CLK high time	8.094	10.036	ns	
Tlow	CLK low time	7.694	9.836	ns	
Edge Rate	Rising edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		350	ps	
Duty Cycle	Duty Cycle	45	55	%	

### REF Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period	69.82033	69.86224	ns	Average period over 1 us
Tab	Absolute Min/Max Period	68.82033	70.86224	ns	
Thigh	CLK high time	TBD	TBD	ns	
Tlow	CLK low time	TBD	TBD	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		1000	ps	
Duty Cycle	Duty Cycle	45	55	%	





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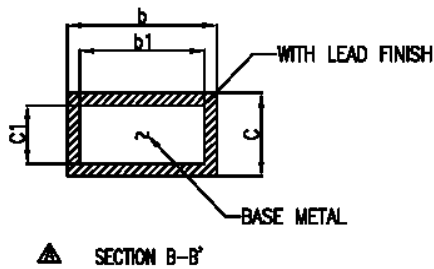
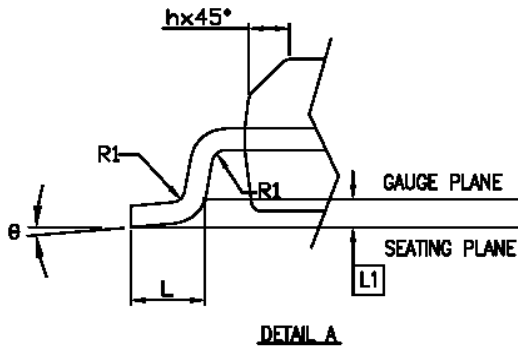
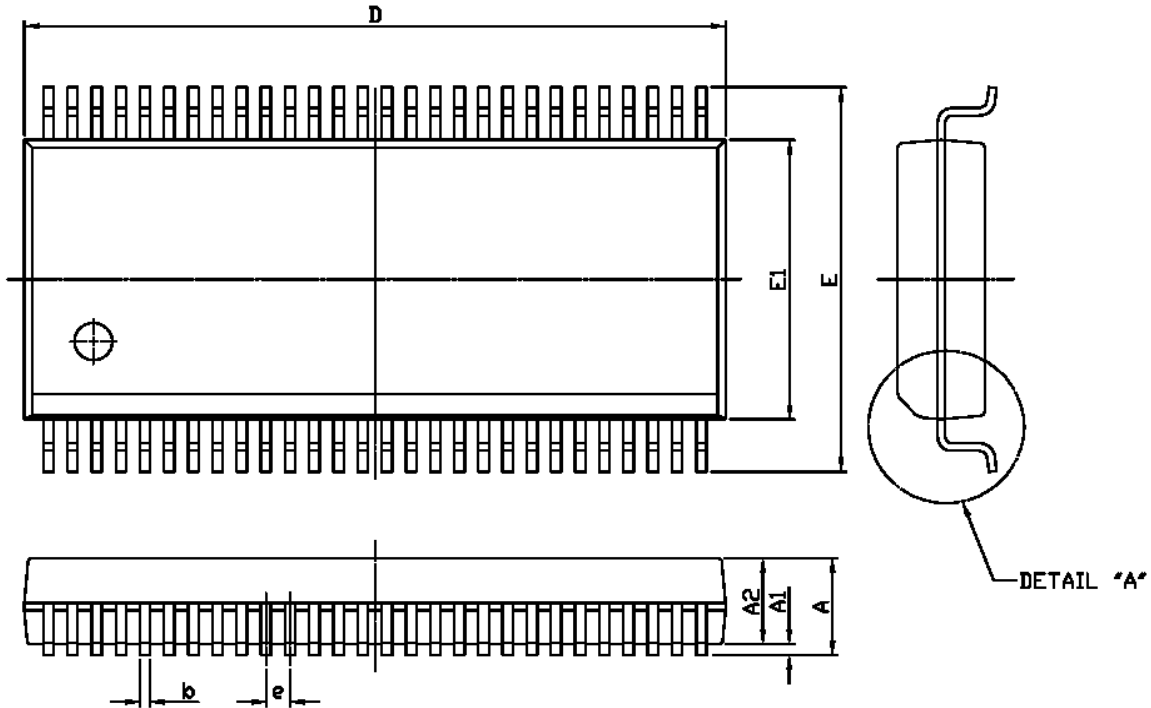
## Ordering Information

Part Number	Package Type	Temperature Range
SLG84410BP	56 Lead SSOP	Commercial, 0° to 70°C
SLG84410BPTR	56 Lead SSOP - Tape and Reel	Commercial, 0° to 70°C
SLG84410BE	56 Lead Green Package SSOP	Commercial, 0° to 70°C
SLG84410BETR	56 Lead Green Package SSOP - Tape and Reel	Commercial, 0° to 70°C



**Package Drawing and Dimensions**

**56 Lead SSOP Package**



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.413	2.591	2.794	0.095	0.102	0.110
A1	0.203	0.305	0.406	0.008	0.012	0.016
b	0.203		0.343	0.008		0.014
b1	0.203	0.254	0.305	0.008	0.010	0.012
c	0.127		0.254	0.005		0.010
c1	0.127		0.216	0.005		0.008
E	10.058	10.312	10.566	0.396	0.406	0.416
E1	7.391	7.493	7.595	0.291	0.295	0.299
e	0.635 BASIC			0.025 BASIC		
h	0.381		0.635	0.015		0.025
L	0.508		1.016	0.020		0.040
L1	0.254 BASIC			0.010 BASIC		
R1						
θ	0		5	0		5

N	D (MM)			JEDEC
	MIN.	NOM	MAX.	
48	15.748	15.875	16.002	MO-118AA
56	18.288	18.415	18.542	MO-118AB



**SILEGO**

**SLG84410B**

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