SLG8LV630

CK-NET

Features

- 1.5V V_{DD} Low Power clock synthesizer with integrated voltage regulator for mobile applications
- Scalable Low Voltage VDD I/O (1.5V to 1.05V) to reduce power consumptionf
- PCI Gen2 Compliant
- Low Power differential outputs with integrated series termination resistors (50 ohm resistor to GND and 33 ohm series resistor not needed)
- CLKREQ inputs to support SRC clock power management
- 48 pin QFN RoHS Compliant Package

Output Summary

- 2- differential CPU clock outputs
- 1 - selectable differential DOT96 or SRC clock output
- 4 - differential Serial Reference Clock (SRC) clock outputs
- 1 - differential LCDCLK clock output
- 1 - differential SATA clock output
- 1 - single-ended 48MHz clock output @ 3.3V
- 3 - single-ended 33MHz PCI clock outputs @ 3.3V
- 1 - selectable 25MHz or PCI clock output @ 3.3V
- 1 - single-ended 14.318MHz clock output @ 3.3V

CPU Frequency

- 100 MHz
- 133 MHz
- 200 MHz

Block Diagram