SLG46400

GreenPAK 2™ Rev. B
Programmable Mixed Signal Array

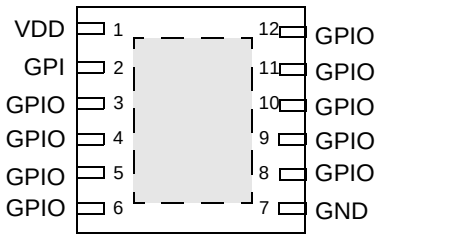
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macro Cells
- Read Back Protection (Read Lock)
- 1.8V (±5%) to 5V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Pb-Free TDFN-12 2.5mm x 2.5mm Package

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

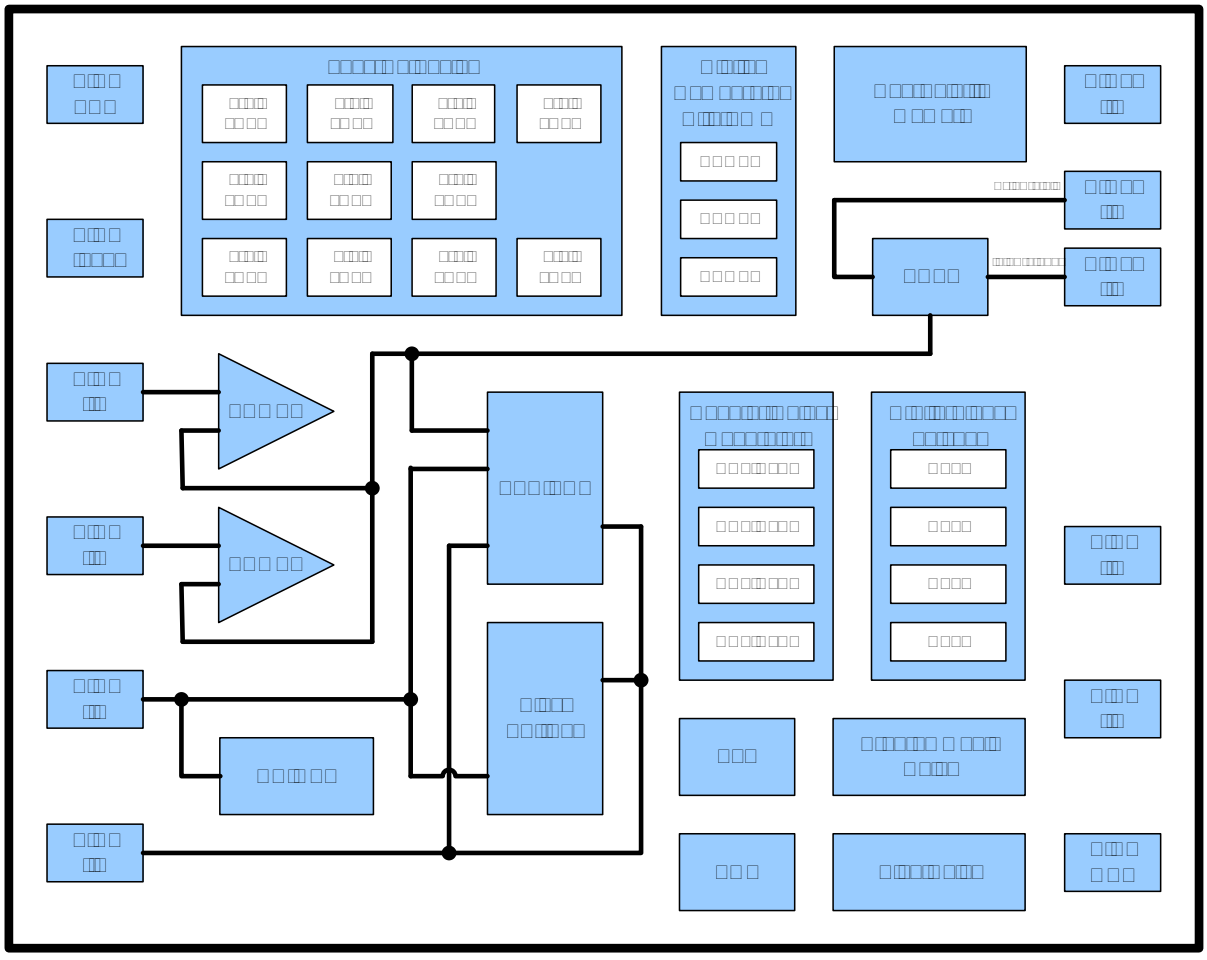
Pin Configuration



TDFN-12 (Top View)

Thermal Pad connected to GND

Block Diagram



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1.0 Overview

The SLG46400 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macro cells of the SLG46400. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macro cells in the device include the following:

- 8-Bit Successive Approximation Register Analog to Digital Converter (SAR ADC)
- Power-On Reset Device (POR)
- Voltage Reference (V_{REF})
- RC Oscillator (RC OSC)
- 4 Counter/Delay Generators (CNT/DLY)
- 4 D Flip-Flop/Latches (DFF)
- 3 Digital Comparators (DCMP) or Pulse Width Modulator (PWM)
- 2 Analog Comparators (ACMP)
- 11 Combinatorial Look-Up Tables (LUT)
- Slave SPI
- Configurable I/O Pins (Open Drain, Push-Pull, Schmitt Trigger Input, Low Voltage Digital Input and Analog I/O)
- Delay (20ns/40ns/60ns/80ns)
- Pipe Delay

The specific functions that can be designed using the SLG46400 include:

- Power-On-Reset Generators
- Signal Delay Elements
- One-Shot Detection
- Voltage Level Detectors
- Voltage Level-Shift Circuits
- Battery Charge Controller
- LED Lighting Control
- Fan Controller
- Optical Encoder
- Level Shifters
- Hall Effect Driver
- Signal De-Glitches

The PWM and ADC macro cells also support more complex control circuits such as fan speed controllers, stepper motor controllers and interface to a wide variety of sensor devices. Traditionally these devices were designed from combinations of low complexity logic and discrete devices requiring costly board space while having complex testing strategies. Silego's SLG46400 allows the functionality of these circuits to be fully tested before being mounted onto a PCB – greatly simplifying the system design and testing procedures.

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	1.8V to 5V Supply
2	GPI	General Input
3	GPIO	General IO or Analog Comparator 0 Input
4	GPIO	General IO or Analog Comparator 1 Input
5	GPIO	General IO or External Clock of OSC, ADC, and S2P
6	GPIO	General IO or Serial Output Data of ADC and Serial Input/Output Data of S2P
7	GND	GND
8	GPIO	General IO or Positive Input of ADC
9	GPIO	General IO or Negative Input of ADC
10	GPIO	General IO or V_{REF} Output
11	GPIO	General IO or V_{REF} Input
12	GPIO	General IO or Single-ended Mode ADC Input Selection
Exposed Bottom Pad	GND	GND

2.2 Programming Pin Description

Pin #	Pin Name	Programming Description
1	VDD	VDD
2	GPI	VPP
3	GPIO	Reset
4	GPIO	N/A
5	GPIO	N/A
6	GPIO	N/A
7	GND	GND
8	GPIO	Program Mode Control
9	GPIO	Die ID
10	GPIO	NVM Read Mode Output Data
11	GPIO	NVM Write Mode Input Data
12	GPIO	NVM Clock

3.0 User Programmability

The SLG46400 is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to construct combinatorial logic elements. Three of the I/O Pins provide a connection for the bit patterns into the OTP on board memory. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gp2 file) is forwarded to Silego to integrate into a production process.

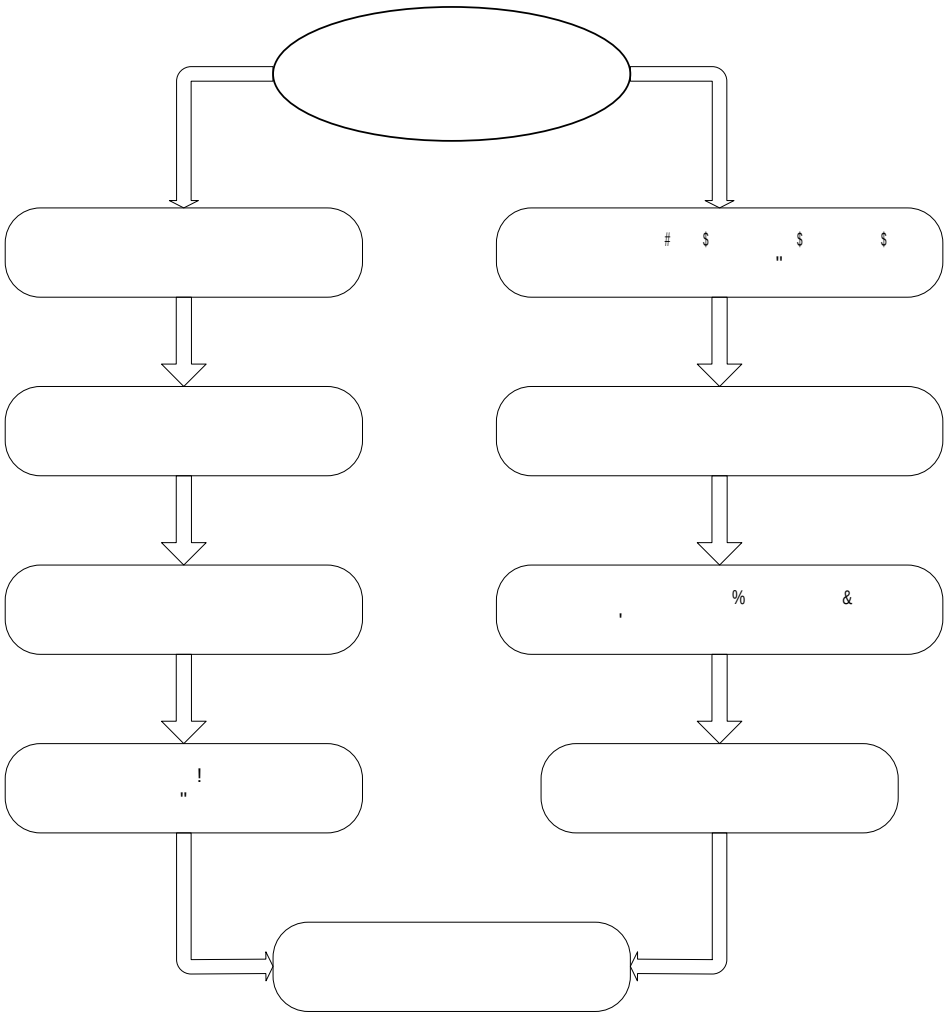

Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46400V	TDFN-12
SLG46400VTR	TDFN-12 - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at Input Pin	-0.3	7	V
Current at Input Pin	-1.0	1.0	mA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	6000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.8	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	--	1	∝A
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.5	7.75	V
V_{AIR}	Analog Input Voltage Range	ADC V_{REF}	0	--	1.0	V
		ACMP Negative Input	0	--	1.0	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.1	--	--	V
		Logic Input with Schmitt Trigger	1.35	--	--	V
		LOW-Level Logic Input	1.1	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.65	V
		Logic Input with Schmitt Trigger	--	--	0.45	V
		LOW-Level Logic Input	--	--	0.50	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN}=1.8V	-1.0	--	1.0	∝A
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN}=0V	-1.0	--	1.0	∝A
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 100∝A, 1X Drive	1.66	--	--	V
		Push-Pull, I_{OH} = 700∝A, 1X Drive	1.21	--	--	V
		Push-Pull, I_{OH} = 1mA, 2X Drive	1.42	--	--	V
		Push-Pull, I_{OH} = 100∝A, 2X Drive	1.68	--	--	V
		Push-Pull, I_{OH} = 700∝A, 2X Drive	1.53	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 100∝A, 1X Drive	--	--	0.040	V
		Push-Pull, I_{OL} = 700∝A, 1X Drive	--	--	0.415	V
		Push-Pull, I_{OL} = 1mA, 2X Drive	--	--	0.245	V
		Push-Pull, I_{OL} = 100∝A, 2X Drive	--	--	0.020	V
		Push-Pull, I_{OL} = 700∝A, 2X Drive	--	--	0.155	V
		Open Drain, I_{OL} = 5mA, 1X Drive	--	--	0.340	V
		Open Drain, I_{OL} = 5mA, 2X Drive	--	--	0.138	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL}	LOW-Level Output Current	Push-Pull, V_{OL} = 0.15V, 1X Drive	0.34	--	--	mA
		Push-Pull, V_{OL} = 0.15V, 2X Drive	0.68	--	--	mA
		Open Drain, V_{OL} = 0.15V, 1X Drive	2.72	--	--	mA
		Open Drain, V_{OL} = 0.15V, 2X Drive	5.44	--	--	mA
T_{SU}	Startup Time	After VDD reaches 1.4-1.6V level	--	7[1]	--	ms

1. If startup time lower than 7 ms is required, please contact Silego regarding a potential custom mixed-signal IC with a reduced startup time for your design.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	--	1	∝A
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.5	7.75	V
V_{AIR}	Analog Input Voltage Range	ADC	0	--	1.0	V
		ACMP	0	--	1.5	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.8	--	--	V
		Logic Input with Schmitt Trigger	2.3	--	--	V
		LOW-Level Logic Input	1.5	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.10	V
		Logic Input with Schmitt Trigger	--	--	0.92	V
		LOW-Level Logic Input	--	--	0.66	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN}=3.3V	-1.0	--	1.0	∝A
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN}=0V	-1.0	--	1.0	∝A
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 3mA, 1X Drive	2.1	--	--	V
		Push-Pull, I_{OH} = 3mA, 2X Drive	2.6	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL} = 3mA, 1X Drive	--	--	0.81	V
		Push-Pull, I_{OL} = 3mA, 2X Drive	--	--	0.32	V
		Open Drain, I_{OL} = 20mA, 1X Drive	--	--	0.605	V
		Open Drain, I_{OL} = 20mA, 2X Drive	--	--	0.252	V
I_{OL}	LOW-Level Output Current	Push-Pull, V_{OL} = 0.4V, 1X Drive	1.836	--	--	mA
		Push-Pull, V_{OL} = 0.4V, 2X Drive	3.672	--	--	mA
		Open Drain, V_{OL} = 0.4V, 1X Drive	14.688	--	--	mA
		Open Drain, V_{OL} = 0.4V, 2X Drive	29.376	--	--	mA
T_{SU}	Startup Time	After VDD reaches 1.4-1.6V level	--	7[1]	--	ms

1. If startup time lower than 7 ms is required, please contact Silego regarding a potential custom mixed-signal IC with a reduced startup time for your design.

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	--	1	∝A
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.5	7.75	V
V_{AIR}	Analog Input Voltage Range	ADC	0	--	1.0	V
		ACMP	0	--	1.5	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.6	--	--	V
		Logic Input with Schmitt Trigger	3.2	--	--	V
		LOW-Level Logic Input	1.7	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.7	V
		Logic Input with Schmitt Trigger	--	--	1.3	V
		LOW-Level Logic Input	--	--	0.77	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN}=5V	-1.0	--	1.0	∝A
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN}=0V	-1.0	--	1.0	∝A
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 5mA, 1X Drive	3.6	--	--	V
		Push-Pull, I_{OH} = 8mA, 1X Drive	2.9	--	--	V
		Push-Pull, I_{OH} = 5mA, 2X Drive	4.1	--	--	V
		Push-Pull, I_{OH} = 8mA, 2X Drive	3.8	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL} = 5mA, 1X Drive	--	--	0.85	V
		Push-Pull, I_{OL} = 8mA, 1X Drive	--	--	1.20	V
		Push-Pull, I_{OL} = 5mA, 2X Drive	--	--	0.36	V
		Push-Pull, I_{OL} = 8mA, 2X Drive	--	--	0.63	V
		Open Drain, I_{OL} = 20mA, 1X Drive	--	--	0.36	V
		Open Drain, I_{OL} = 20mA, 2X Drive	--	--	0.17	V
I_{OL}	LOW-Level Output Current	Push-Pull, V_{OL} = 0.4V, 1X Drive	2.745	--	--	mA
		Push-Pull, V_{OL} = 0.4V, 2X Drive	5.490	--	--	mA
		Open Drain, V_{OL} = 0.4V, 1X Drive	21.960	--	--	mA
		Open Drain, V_{OL} = 0.4V, 2X Drive	43.920	--	--	mA
T_{SU}	Startup Time	After VDD reaches 1.4-1.6V level	--	7[1]	--	ms

1. If startup time lower than 7 ms is required, please contact Silego regarding a potential custom mixed-signal IC with a reduced startup time for your design.

6.0 Summary of Macro Cell Function

6.1 I/O Pins (10 total)

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain
- Push Pull
- Analog I/O
- 50K/100K/300K pull-up/pull-down resistors

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Analog to Digital Converter

- 8-bit, 10kHz, Successive Approximation Register ADC
- DNL < ±1LSB, INL < ±1LSB
- V_{IN} Range: 0 ~ 1V
- Common Mode Voltage Range: $V_{PP}/2$ ~ $V_{DD}/2$
- 3-bit Programmable Gain Amplifier with gain values of (1, 2, 4, 8,16X in differential mode and 0.5, 1, 2, 4, 8X in single-ended mode)
- SPI output format

6.4 Analog Comparators (2 total)

- 0mV/12mV/50mV/150mV Hysteresis

6.5 Voltage Reference Out

- Provides an external voltage based on either ACMP0 reference or $V_{DD}/3$

6.6 Digital Comparators or PWM (3 total)

- Three 8-bit 10MHz PWMs or Digital Comparators

6.7 Delays/Counters (4 total)

- Delay Time Range: 1-16384 clock cycles (clock cycle based on RC Oscillator or External Clock Input)
- Three 14-bit delays/counters: Range 1-16384 clock cycles
- One 8-bit delay/counter: Range 1-255 clock cycles
- Two counters can function as FSM counters

6.8 Programmable Delay

- 20ns/40ns/60ns/80ns

6.9 Pipe Delay Output

- 1 pipe
- 2/4/8/12 pipes
- 3/5/7/11 pipes

6.10 RC Oscillator

- 16 frequencies ranging from 27kHz – 10MHz

6.11 Slave SPI/S2P

- Supports Slave SPI to control DCMP/PWM/FSM counter
- ADC SPI Output

6.12 Combinatorial Logic LUTs (11 total)

- Used to create either standard or custom digital logic cells
- Four 2-bit Lookup Tables
- Six 3-bit Lookup Tables
- One 4-bit Lookup Table

6.13 Digital Storage Elements (4 total)

- Four D Flip-Flops or Latches

6.14 Power On Reset

- V_{DD} >1.6V

7.0 I/O Pins

The SLG46400 has a total of 10 multi-function I/O Pins which can function as either a user defined Input or Output as well as serve as a programmable function for the one time Non-Volatile Memory to configure interconnect logic.

Normal Mode Pin Definition is as follows:

- PIN 2: Input Pin only
- PIN 3: GPIO or Input for Analog Comparator 0
- PIN 4: GPIO or Input for Analog Comparator 1
- PIN 5: GPIO or External Clock Input for ADC, RC OSC and S2P
- PIN 6: GPIO or ADC Serial Output Data, S2P input/output data (reg<712:711>)
- PIN 8: GPIO or ADC IN+
- PIN 9: GPIO or ADC IN-
- PIN 10: GPIO or V_{REF} Output
- PIN 11: GPIO or V_{REF} Input
- PIN 12: GPIO or Single-Ended mode ADC channel selection

Programming Mode Pin Definition is as follows:

- PIN 2: Voltage for Programming Power (7.5V needed)
- PIN 3: Program Reset
- PIN 8: Program Mode Control
- PIN 9: Die ID
- PIN 10: NVM Read Mode Output Data
- PIN 11: NVM Write Mode Input Data
- PIN 12: NVM Clock

Of the ten user defined I/O Pins in the SLG46400, nine pins (PINs 3, 4, 5, 6, 8, 9, 10, 11, and 12) can be used for either input or output and one pin (PIN 2) is defined as input only.

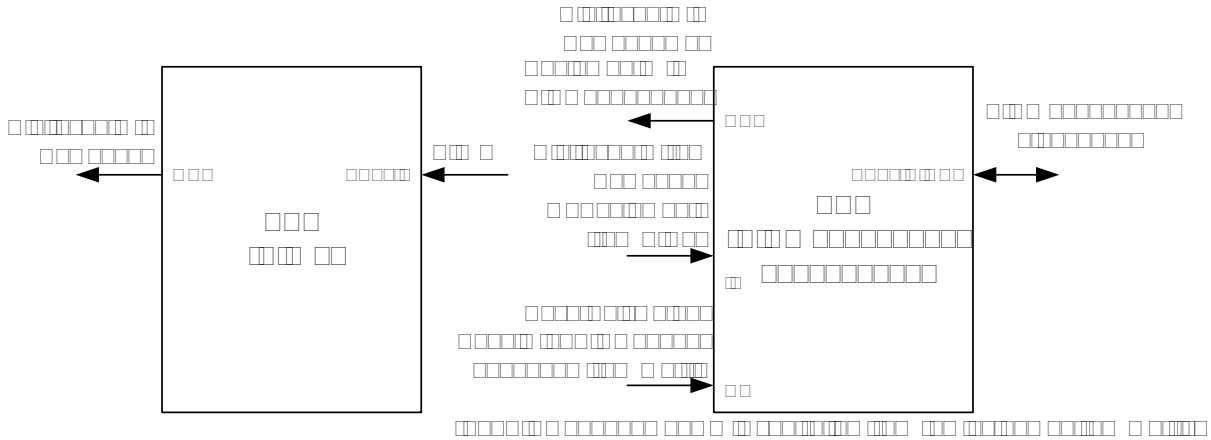

Figure 2. I/O Pads Layout

7.1 Input Modes

Each input pin can be configured as a Digital Input with/without Buffered Schmitt Trigger, Low Voltage Digital In (1.5V), or Analog In to control the user signals that are inputted into the SLG46400. All digital input pins will either have a logic “1” or “0” value inputted into the SLG46400, based on the configuration of the input pin which is defined by the user.

7.2 Output Modes

PINs 3, 4, 5, 6, 8, 9, 10, 11 and 12 can be configured as either an open drain output or push-pull output (with Output Enable). Additionally PIN 10 can be also be configured as an analog output in the SLG46400 device.

The OE functionality for each of the output pins is controlled by the connection matrix except for PINs 3, 8, and 9. Those pins are controlled by the following registers:

reg<685> for PIN3

reg<547> for PIN8

reg<556> for PIN9

7.2.1 Open Drain Output

The Open Drain Output setting has a 1X current ratio. The open drain output signal from the SLG46400 design will decide the port's output state (Hi-Z or ground).

If the signal = 1, output will be Hi-Z (high impedance)

If the signal = 0, output will be connected to ground

PINs 6 and 12 have a 2X current sinking option where the current value depends on V_{DD}.

7.2.2 Push Pull with Output Enable

The Push Pull with Output Enable setting has either a 1X or 2x current ratio and the Output Enable signal will make the output Hi-Z

All output pins have Push Pull 2X current sinking option where the current value depends on V_{DD}. With 1X option these currents will be one half the value of the 2X value.

7.2.3 Analog Input and Open Drain Output

PINs 3, 4, 8, 9, and 11, can be configured as Analog Inputs/Open Drain Outputs on this device. Using this configuration will make the pin bi-directional, but the output will be Open Drain. This means that a logic LOW state on the pin will cause both the output and the input to go LOW.

7.2.4 Analog Output

Analog output functionality is only available on PIN 10 and is configured via the V_{REF} cell

Analog Output = internal signal value

7.2.5 Digital Bi-Directional Input / Output Pin by Configuring Settings

PIN 4, PIN 5, PIN 6, PIN 10, PIN 11, and PIN 12 can be configured as a Bi-Directional Pins by configuring the Analog Input and Open Drain Output settings in the GreenPAK II Designer tool. This is done by going to the PIN's propertly menu in the GreenPAK II Designer software and changing the Mode Setting to "Analog In/Out and Open Drain".

7.2.6 Creating a Digital Bi-Directional Input / Output Pin using an OE Signal

The PINs can also be configured as Digital Bi-Directional Input / Output Pins using an external Output Enable signal with the following steps:

1. Configure the I/O Pins as one of the following:

    a. Digital Input with Schmitt Trigger
    b. Digital Input without Schmitt Trigger
    c. Low Voltage Digital Input

2. Use a control signal for the Output Enable on the I/O Pin

3. The I/O Pin will function as Push Pull 1x current by setting the OE signal of the pin to HIGH.

7.3 Pull Up/Down Resistors

All 10 I/O Pins have the option of a 50k/100k/300k pull up/down resistor. Resistors can be used with any of the input or output pin configurations previously defined.

7.4 I/O Pins Register Settings

7.4.1 PIN 2 Register Settings

Table 1. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	<673:672>	00: Digital In with Schmitt Trigger 01: Digital In without Schmitt Trigger 10: Low Voltage Digital In 11: Reserved
PIN 2 Pull Up/Down Resistor Value Selection	<675:674>	00: Floating 01: 50k Resistor 10: 100k Resistor 11: 300k Resistor
PIN 2 Pull Up/Down Resistor	<676>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 2 Reset Enable	<808>	0: Disable 1: Enable
PIN 2 Edge Detect Mode	<807>	0: Rising Edge 1: Falling Edge Note: N/A of Reset Enable signal is ‘0’
PIN 2 Bypass	<806>	0: PIN 2 Edge Active 1: PIN 2 High Active Note: N/A of Reset Enable signal is ‘0’

7.4.2 PIN 3 Register Settings

Table 2. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Initial State Control	<678:677>	00: Output Floating 01: Output Ground 10: Output Power 11: Output Follow Input
PIN 3 Mode Control	<681:679>	000: Digital In with Schmitt Trigger 001: Digital In without Schmitt Trigger 010: Low Voltage Digital In without Schmitt Trigger 011: Analog IO 100: 2X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable) 101: 1x Current Open Drain 110: Analog Input & Open Drain Mode 111: 1X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable)
PIN 3 Pull Up/Down Resistor Value Selection	<683:682>	00: Floating 01: 50k Resistor 10: 100k Resistor 11: 300k Resistor
PIN 3 Pull Up/Down Resistor	<684>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 3 Push Pull Output Enable	<685>	0: Push Pull Output Disable 1: Push Pull Output Enable

7.4.3 PIN 4 Register Settings

Table 3. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Initial State Control	<687:686>	00: Output Floating 01: Output Ground 10: Output Power 11: Output Follow Input
PIN 4 Mode Control	<690:688>	000: Digital In with Schmitt Trigger 001: Digital In without Schmitt Trigger 010: Low Voltage Digital In without Schmitt Trigger 011: Analog IO 100: 2X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable) 101: Open Drain 110: Analog Input & Open Drain Mode 111: 1X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable)
PIN 4 Pull Up/Down Resistor Value Selection	<692:691>	00: Floating 01: 50k Resistor 10: 100k Resistor 11: 300k Resistor
PIN 4 Pull Up/Down Resistor	<693>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.4 PIN 5 Register Settings

Table 4. PIN 5 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 5 Initial State Control	<695:694>	00: Output Floating 01: Output Ground 10: Output Power 11: Output Follow Input
PIN 5 Mode Control	<698:696>	000: Digital In with Schmitt Trigger 001: Digital In without Schmitt Trigger 010: Low Voltage Digital In without Schmitt Trigger 011: Reserved 100: 2X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable) 101: Open Drain 110: Reserved 111: 1X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable)
PIN 5 Pull Up/Down Resistor Value Selection	<700:699>	00: Floating 01: 50k Resistor 10: 100k Resistor 11: 300k Resistor
PIN 5 Pull Up/Down Resistor	<701>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.5 PIN 6 Register Settings

Table 5. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Initial State Control	<703:702>	00: Output Floating 01: Output Ground 10: Output Power 11: Output Follow Input
PIN 6 Mode Control	<706:704>	000: Digital In with Schmitt Trigger 001: Digital In without Schmitt Trigger 010: Low Voltage Digital In without Schmitt Trigger 011: Reserved 100: 2X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable) 101: Open Drain 110: Reserved 111: 1X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable)
PIN 6 Pull Up/Down Resistor Value Selection	<708:707>	00: Floating 01: 50k Resistor 10: 100k Resistor 11: 300k Resistor
PIN 6 Pull Up/Down Resistor	<709>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 6 Open Drain Double Current	<710>	0: Normal 1: Double Current
PIN6 Digital Output Selection Source	<712:711>	0X: From Connection Matrix (Out25) 10: From S2P (MISO) 11: From ADC Serial Output

7.4.6 PIN 8 Register Settings

Table 6. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Initial State Control	<540:539>	00: Output Floating 01: Output Ground 10: Output Power 11: Output Follow Input
PIN 8 Mode Control	<543:541>	000: Digital In with Schmitt Trigger 001: Digital In without Schmitt Trigger 010: Low Voltage Digital In without Schmitt Trigger 011: Analog IO 100: 2X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable) 101: Open Drain 110: Analog Input & Open Drain Mode 111: 1X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable)
PIN 8 Pull Up/Down Resistor Value Selection	<545:544>	00: Floating 01: 50k Resistor 10: 100k Resistor 11: 300k Resistor
PIN 8 Pull Up/Down Resistor	<546>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Push Pull Output Enable	<547>	0: Push Pull Output Disable 1: Push Pull Output Enable

7.4.7 PIN 9 Register Settings

Table 7. PIN 9 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 9 Initial State Control	<549:548>	00: Output Floating 01: Output Ground 10: Output Power 11: Output Follow Input
PIN 9 Mode Control	<552:550>	000: Digital In with Schmitt Trigger 001: Digital In without Schmitt Trigger 010: Low Voltage Digital In without Schmitt Trigger 011: Analog IO 100: 2X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable) 101: Open Drain 110: Analog Input & Open Drain Mode 111: 1X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable)
PIN 9 Pull Up/Down Resistor Value Selection	<554:553>	00: Floating 01: 50k Resistor 10: 100k Resistor 11: 300k Resistor
PIN 9 Pull Up/Down Resistor	<555>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 9 Push Pull Output Enable	<556>	0: Push Pull Output Disable 1: Push Pull Output Enable

7.4.8 PIN 10 Register Settings

Table 8. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Initial State Control	<558:557>	00: Output Floating 01: Output Ground 10: Output Power 11: Output Follow Input
PIN 10 Mode Control	<561:559>	000: Digital In with Schmitt Trigger 001: Digital In without Schmitt Trigger 010: Low Voltage Digital In without Schmitt Trigger 011: Analog IO 100: 2X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable) 101: Open Drain 110: Reserved 111: 1X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable)
PIN 10 Pull Up/Down Resistor Value Selection	<563:562>	00: Floating 01: 50k Resistor 10: 100k Resistor 11: 300k Resistor
PIN 10 Pull Up/Down Resistor	<564>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.9 PIN 11 Register Settings

Table 9. PIN 11 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 11 Initial State Control	<566:565>	00: Output Floating 01: Output Ground 10: Output Power 11: Output Follow Input
PIN 11 Mode Control	<569:567>	000: Digital In with Schmitt Trigger 001: Digital In without Schmitt Trigger 010: Low Voltage Digital In without Schmitt Trigger 011: Analog IO 100: 2X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable) 101: Open Drain 110: Analog Input & Open Drain Mode 111: 1X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable)
PIN 11 Pull Up/Down Resistor Value Selection	<571:570>	00: Floating 01: 50k Resistor 10: 100k Resistor 11: 300k Resistor
PIN 11 Pull Up/Down Resistor	<572>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.10 PIN 12 Register Settings

Table 10. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Initial State Control	<574:573>	00: Output Floating 01: Output Ground 10: Output Power 11: Output Follow Input
PIN 12 Mode Control	<577:575>	000: Digital In with Schmitt Trigger 001: Digital In without Schmitt Trigger 010: Low Voltage Digital In without Schmitt Trigger 011: Reserved 100: 2X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable) 101: Open Drain 110: Reserved 111: 1X Current Push Pull (OE = 0 then Output TriState, OE = 1 Output Enable)
PIN 12 Pull Up/Down Resistor Value Selection	<579:578>	00: Floating 01: 50k Resistor 10: 100k Resistor 11: 300k Resistor
PIN 12 Pull Up/Down Resistor	<580>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 12 2X Current Open Drain Mode	<581>	0: Normal 1: Double Current

8.0 Connection Matrix

The Connection Matrix in the SLG46400 is used to create the internal routing for the 832 register bits of the SLG46400 device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection point for each logic cell within the SLG46400 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 832 register bits within the SLG46400 are programmed a fully custom circuit will be created.

For a complete list of the SLG46400’s register table, see Appendix A.

8.1 Connection Matrix Register Settings

Table 11. Connection Matrix Register Settings

Register Code	Connection Point
000000	Ground
000001	LUT2_0 Output
000010	LUT2_1 Output
000011	LUT2_2 Output
000100	LUT2_3 Output
000101	LUT3_0 Output
000110	LUT3_1 Output
000111	LUT3_2 Output
001000	LUT3_3 Output
001001	LUT3_4 Output
001010	LUT3_5 Output
001011	LUT4 Output
001100	DFF0/LATCH0 Output
001101	DFF1/LATCH1 Output
001110	DFF2/LATCH2 Output
001111	DFF3/LATCH3 Output
010000	PIN2 Digital Output
010001	PIN3 Digital Output
010010	PIN4 Digital Output
010011	PIN5 Digital Output
010100	PIN6 Digital Output
010101	PIN8 Digital Output
010110	PIN9 Digital Output
010111	PIN10 Digital Output
011000	PIN11 Digital Output
011001	PIN12 Digital Output
011010	RC Oscillator Output
011011	RC Oscillator Divided By 4 Output
011100	RC Oscillator Divided By 12 Output
011101	DLY0/CNT0 Output
011110	DLY1/CNT1 Output

Table 11. Connection Matrix Register Settings

Register Code	Connection Point
011111	DLY2/CNT2 Output
100000	DLY3/CNT3 Output
100001	Edge Detect Output
100010	Analog Comparator0 Output
100011	Analog Comparator1 Output
100100	ADC Output
100101	Digital Comparator0 Equal Output
100110	Digital Comparator1 Equal Output
100111	Digital Comparator2 Equal Output
101000	PWM/DCMP0 OUT- Output
101001	PWM/DCMP0 OUT+Output
101010	PWM/DCMP1 OUT- Output
101011	PWM/DCMP1 OUT+Output
101100	PWM/DCMP2 OUT- Output
101101	PWM/DCMP2 OUT+Output
101110	Reserved
101111	Programmable Delay Output
110000	Pipe Delay OUT0
110001	Pipe Delay OUT1
110010	Power Detector Output (PWR DETECT)
110011	1 PIPE OUT
110100	DFF0 Negative Output (nQ)
110101	DFF1 Negative Output (nQ)
110110	DFF2 Negative Output (nQ)
110111	DFF3 Negative Output (nQ)
111000	Ground
111001	Ground
111010	Ground
111011	Ground
111100	Ground
111101	Ground
111110	Power On Reset (OUT)
111111	VDD

9.0 Analog-to-Digital Converter (ADC)

The Analog to Digital Converter in the SLG46400 is an 8-bit Successive Approximation Register Analog to Digital Converter (SAR ADC) which operates at a maximum sampling speed of 10 kHz. The ADC's DNL < ±1LSB and INL < ±1LSB and has a V_{BG} accuracy of ±50mV. User controlled inputs and outputs of the ADC are listed below:

Inputs:

- CH SELECTOR: Single-Ended Mode ADC Selection and Analog Input Mux Control Signal (PIN 12)
- IN+: Single-Ended Mode Input and Differential Mode Positive Input (PIN8)
- IN-: Differential Mode Negative Input (PIN 9)
- EXT. VREF: ADC External Voltage Reference Input (PIN 11)
- EXT. CLK: ADC External Clock Input (PIN 5)
- SHARED PD: ADC Power Down Signal

Outputs:

- Ext_refout: ADC External Voltage Reference Output (PIN 10)
- PGA_Out: Output of the PGA to ACMP0
- SER DATA: ADC serial output (PIN 6)
- PAR DATA: 8-bit ADC parallel data to either the PWM or DCMP0
- ADC Interrupt Output (INT. OUT)

9.1 ADC Functional Diagram

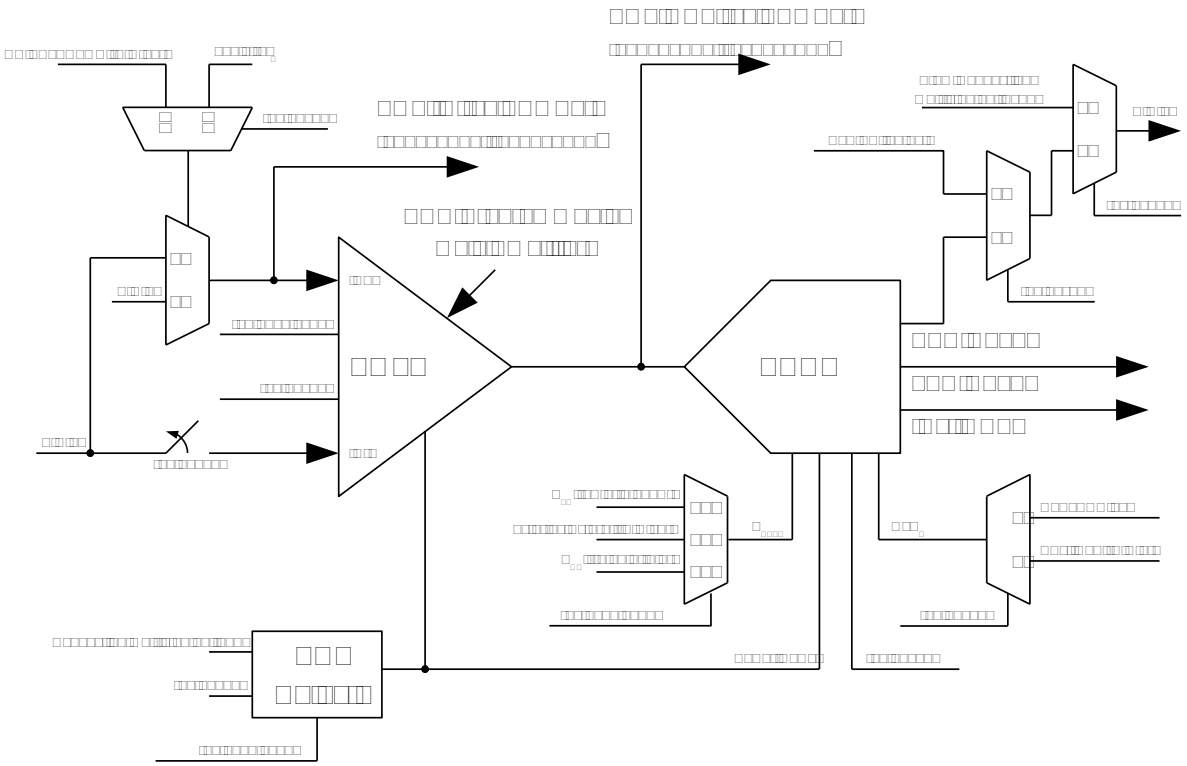

Figure 3. ADC Functional Diagram

9.2 ADC Operation Modes

The ADC has three operating modes:

- Single-Ended ADC operation using IN+ from PIN 8, when *ADC_sel* (reg <742>) is “0”
- Differential ADC operation using IN+ from PIN 8 and IN- from PIN 9, when *ADC_sel* (reg <742>) is “1”
- Pseudo-Differential ADC operation using IN+ from PIN 8 and IN- from PIN 9, when *ADC_sel* (reg <742>) and *ADC_pseudodiff_en* (reg <738>) bits are both set to “1”

9.3 ADC 3-bit Programmable Gain Amplifier

The front end of the ADC is a PGA with 3 bits for setting gain. The gain settings range from 0.5x to 16x. The PGA buffers the ADC in all cases except with the singled ended gain is 0.5x. Single-ended PGA operation has gain settings of 0.5, 1, 2, 4, and 8x, while Differential operation has gain settings of 1, 2, 4, 8, and 16x. The PGA gain is set by the ADC_gain_control (reg<718:716>). See ADC Register Settings Table

For Pseudo-Differential mode, the PGA gain can only be 1X.

9.4 ADC 2-Channel Selection

When *ADC_channel_sel* (reg <714>) is set to “1”, the PGA of the ADC will sample either PIN 8 or PIN 9 on the IN+ input, where the selection is controlled by PIN 12.

- When PIN 12 is set to “0”, the ADC will sample PIN 9
- When PIN 12 is set to “1”, the ADC will sample PIN 8

When *ADC_channel_sel* (reg <714>) is set to “0”, the PGA of the ADC will sample PIN 8 on the IN+ input.

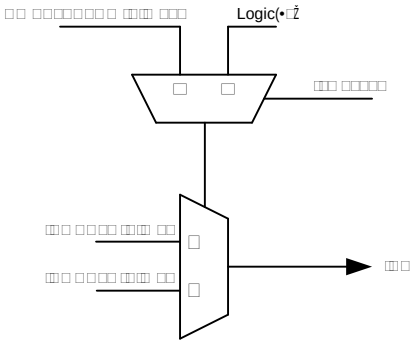

Figure 4. ADC 2-Channel Selection

9.5 ADC Input Voltage Definition

The ADC’s input voltage (V_{IN_ADC}) is calculated based on either the single-ended or differential operation modes the logic cell is set to. In single-ended mode V_{IN_ADC} is the positive input voltage multiplied by the gain of the PGA. While in differential mode the V_{IN_ADC} is the difference between the positive and negative input voltages multiplied by the gain of the PGA plus one half of the reference voltage.

$$V_{in\_adc} \quad \begin{matrix} V_{in} \quad G_{pga} \times gain \\ V_{in} \quad V_{in} \quad G_{pga} \times gain \quad V_{ref}/2 \end{matrix} \quad \begin{matrix} \text{Single-ended mode} \\ \text{Differential mode} \end{matrix}$$

Equation 1. ADC Input Voltage equation

9.6 ADC Reference Voltage

The ADC's reference voltage (V_{REF}) is controlled by ADC_Vref_sel (reg <720:719>) and the ADC_DAC_Vref (reg <713>). See the Table 12 for reference. For optimal ADC performance, the Ext_Vref value should not be greater than 1.0V. The three reference voltage inputs are chosen from the following:

- Bandgap voltage (V_{BG}) of 1V or 0.778V from Internal Source
- 1x or 2x External User Defined Voltage Source (PIN 11)
- Power Divider of (0.25 or 0.5) * V_{DD}

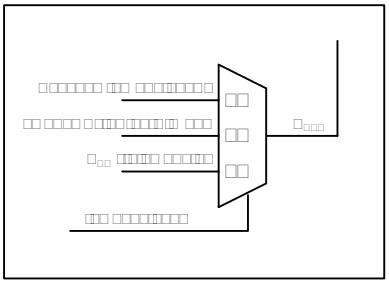

Figure 5. ADC Reference Voltage

Table 12. ADC Reference Voltage.

reg <720:719>	V_{REF}	
	reg <713> = 0	reg <713> = 1
00	V_{BG} (1V)	V_{BG} (0.778V)
01	2x Ext_Vref (PIN 11)	1x Ext_Vref (PIN 11)
10	Power Divider (0.5 * V_{DD})	Power Divider (0.25 * V_{DD})
11	N/A	N/A

9.7 ADC Power Down Select Mode

The ADC's power down source is selected by reg <815:814> (shared with the PWM and OSC). When reg <815:814> = '01', the ADC power down is controlled by reg <813>, where if reg <813> = '0', ADC is powered down, and if reg <813> = '1', ADC operates normally. Otherwise the ADC power down is controlled by the *connection matrix output 3* signal where a value of "1" will drive the ADC and the PGA to power down mode. The SLG46400 also has a slow/fast power on mode feature controlled by reg<715>. When reg<715> = 0, the ADC is in slow power on mode and the entire analog block is controlled by *connection matrix output 3*. When reg<715> = 1, ADC is in fast power on mode, where only the ADC will be controlled by *connection matrix output 3* and the analog block will remain on. With this feature, the first ADC power on (with the rest of the analog block) will be approximately 20∝s; the next power cycle the ADC power on (ADC only) time is <1ns.

9.8 ADC Clock Source

The ADC clock source comes from either the internal RC Oscillator (CLK4ADC/64) or an external clock from PIN 5. The selection is made from the *ADC_clk_sel* signal via reg <737> where:

- The RC Oscillator is used when the *ADC_clk_sel* is "0"
- An external clock from PIN 5 is used when the *ADC_clk_sel* is "1"

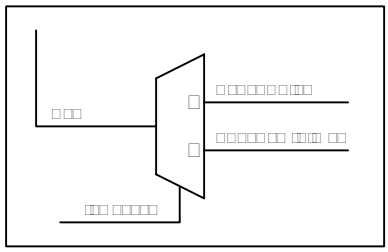

Figure 6. ADC Clock Source

The ADC requires 16 clock cycles to sample the analog voltage and output the sampled data.

When the internal RC Oscillator is used for providing timing to the ADC, a total of 1024 clock cycles are needed since the *CLK4ADC* signal is also divided by 64.

When an external clock is used on PIN5, the ADC will only need 16 clock cycles, as it bypasses the divide by 64 logic.

$$F_{ADC} = \frac{F_{OSC}}{64 \cdot 16 cycles} = \frac{F_{OSC}}{1024} cycles$$

$$F_{ADC} = \frac{F_{ext\ clk}}{16}$$

Equation 2. ADC Input Voltage equation

9.9 ADC Outputs

The ADC's output can be shifted out through the S2P logic cell. The *SER DATA* produces eight single data bits over eight individual clock cycles when activated, while the *PAR DATA* produces an 8-bit data string over 16 clock cycles.

9.9.1 ADC Serial Output

The 8-bit serial data can be outputted from the SLG46400 device on PIN 6. The individual 8 serial data bits can be read into an external device within the larger system design.

To initialize the *SER DATA* the ADC needs a Power Down signal, which can be configured through the connection matrix. After 3 ADC_CLK cycles the ADC will start to output the 8-Bit Serial Data. This PD signal needs to be held for at least 16 ADC_CLK cycles. The ADC_CLK is determined by either the SLG46400 clock, the RC Oscillator/64, or an external clock (from PIN 5) divided by 64.

9.9.2 ADC Parallel Output

The 16-bit parallel data can be outputted from the ADC logic cell to either the DCMP/PWM or FSM logic cells within the SLG46400 device.

To initialize the *PAR DATA* the ADC needs a Power Down signal, which can be configured through the connection matrix. After ten ADC_CLK cycles the ADC will start to output the 16-Bit Parallel Data. This PD signal needs to be held for at least 32 ADC_CLK cycles. The ADC_CLK is determined by either the SLG46400 clock, the RC Oscillator/64, or an external clock (from PIN 5) divided by 64.

9.10 ADC Interrupt Output Timing Diagram

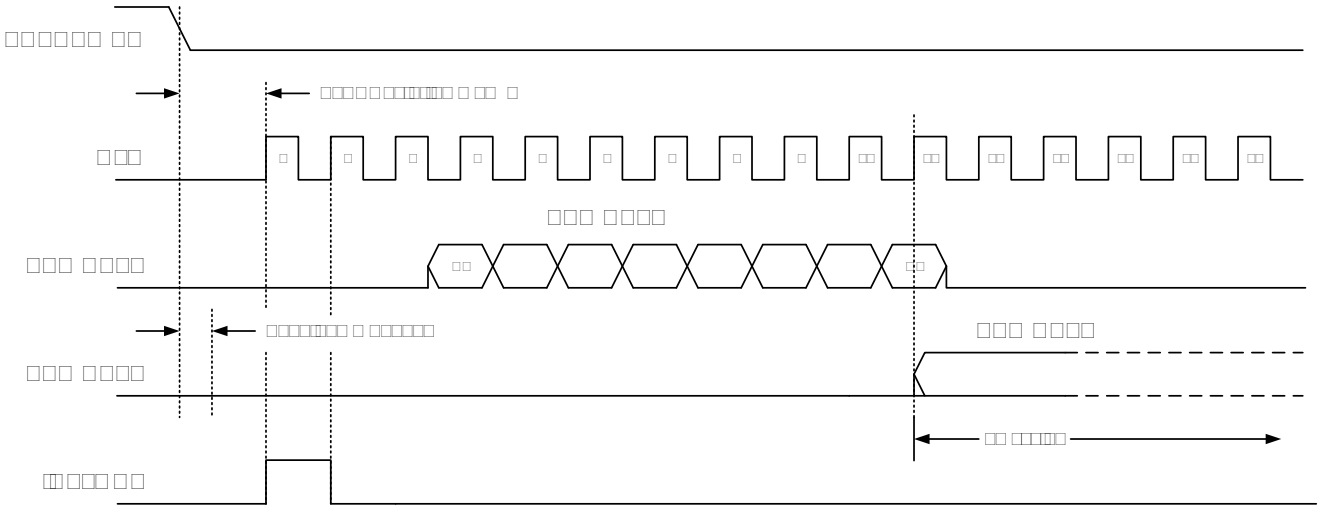

Figure 7. ADC Interrupt Output Timing Diagram

9.11 ADC Register Settings

Table 13. ADC Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
PIN6_dig_out	PIN 6 digital output source selection	<712:711>	00/01: from connection matrix 10: serial data from the S2P/SPI 11: serial data from the ADC
ADC_DAC_Vref	ADC reference DAC feedback select	<713>	0: normal 1: 0.5 gain
ADC_channel_sel	ADC mux channel selection	<714>	0: mux Disabled, ADC will sample PIN 8 for IN+ 1: mux Enabled, ADC will sample either PIN 8 or 9 for IN+
ADC_pdmode_sel	ADC power down mode selection	<715>	0: ADC slow power on 1: ADC fast power on
ADC_gain_control	ADC PGA gain control	<718:716>	000: single-ended (0.5X gain) or differential (N/A) 001: single-ended (1X gain) or differential (1x gain) 010: single-ended (2X gain) or differential (2X gain) 011: single-ended (4X gain) or differential (4X gain) 100: single-ended (8X gain) or differential (8X gain) 101: single-ended (N/A) or differential (16X gain)
ADC_Vref_sel	V_{REF} setting (depends on reg <713>)	<720:719>	00: V_{BG} (1V or 0.778V) 01: 1x or 2x external voltage source 10: Power Divider of V_{DD}* (0.25 or 0.5)
ADC_pg_en	ADC input pass gate charge pump enable	<735>	0: Passgate charge pump off 1: Passgate charge pump on
ADC_clk_sel	ADC clock selection	<737>	0: internal RC Oscillator 1: external clock from PIN 5
ADC_pseudodiff_en	ADC pseudo differential enable	<738>	0: Disable 1: Enable
ADC_sel	ADC mode select	<742>	0: single-end operation using PIN 8 1: differential mode using PINS 8 & 9
DAC_in_sel	DAC input data select	<746>	0: ADC normal operation 1: DAC data comes from FSM1
ADC_pd_control	ADC power down control	<813>	0: ADC power down 1: ADC normal operation
ADC_PWM_OSC_pd_src_sel	ADC/PWM/OSC power down source select	<815:814>	00: ADC pd from matrix out <3>, PWM pd from register 01: PWM pd from matrix out <3>, ADC pd from register 10: ADC & PWM pd from matrix out <3> 11: OSC pd from matrix out <3>, ADC & PWM pd from register

10.0 Analog Comparator (ACMP)

There are two Analog Comparator (ACMP) macro cells in the SLG46400. In order for the ACMP cells to be used in a GreenPAK design the power up signals (*PWR UP*) need to be active. These signals should be HIGH to turn on the ACMP and LOW to turn it off and each ACMP can be powered seperately.

When ACMP is powered down, output is low.

Each of the two ACMP cells has a negative input signal that is either created from an internal reference voltage (V_{REF}) or provided by way of the external sources.

10.1 ACMP0 Input Modes

ACMP0's positive input (IN+) can be connected to PIN3, PIN4, ADC/PGA OUT or IN by setting reg <735> and by the *ACMP0_PGA_en* signal, reg<739>. The negative input (IN-) of the ACMP0 cell can come from the internal V_{REF} macro cell which will generate a 50mV to 1.5V signal (only when V_{DD} > 3.0V), a 30mV to 1.0V signal, or from an external voltage source that is placed on PIN 11. Selection is made using a 4-bit value from NVM (reg<725:722>) and the V_{REF} band select (reg<736>).

10.2 ACMP0 Functional Diagram

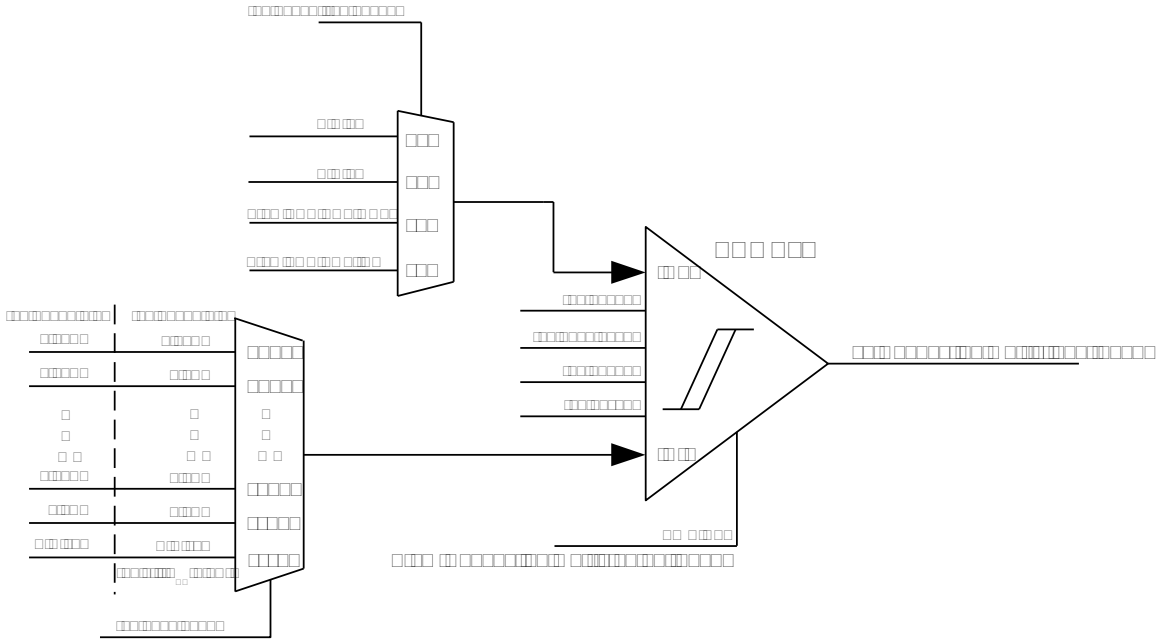

Figure 8. ACMP0 Functional Diagram

10.3 ACMP1 Functional Diagram

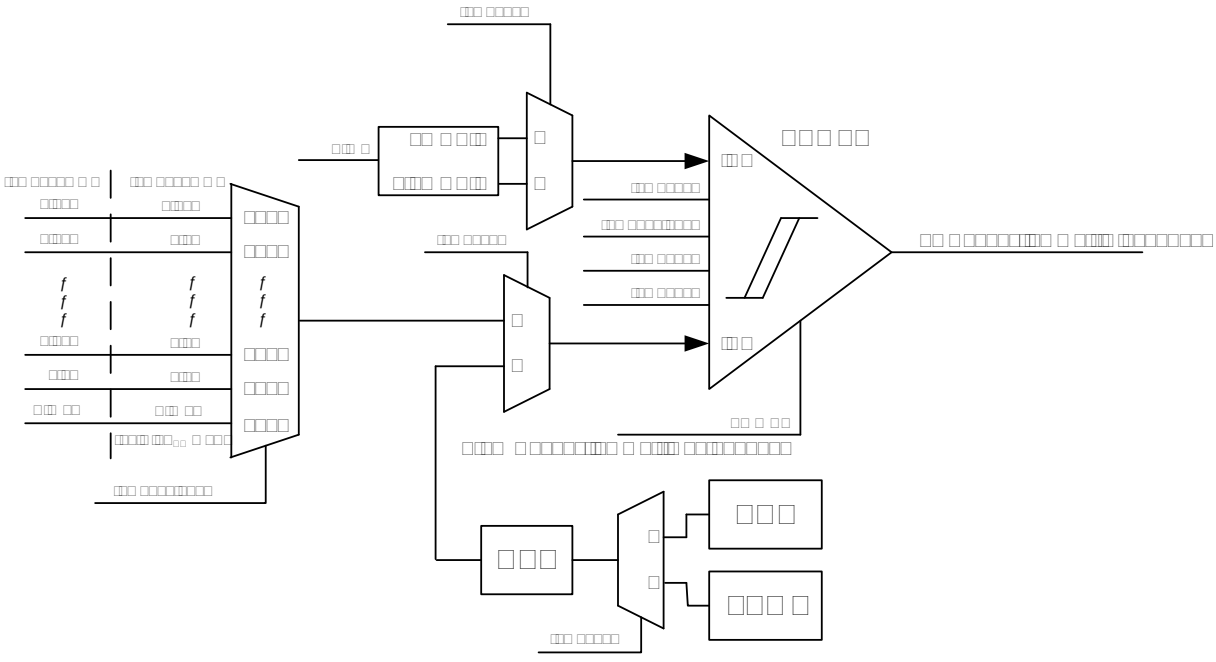

Figure 9. ACMP1 Functional Diagram

10.4 ACMP1 Input Modes

ACMP1's positive input (IN+) comes from PIN 4 with selection gain of 1X or 0.5X (two 50k resistor divider). The *ACMP1_0.5gain_en* signal (reg<747>) is used as a control signal into a MUX which has the 1X and 0.5X signals as inputs.

The negative input (IN-) of the ACMP1 cell can come from the DAC or the internal V_{REF} logic cell (selected by reg <745>) which will generate a 50mV to 1.5V signal (only when V_{DD} > 3.0V), a 30mV to 1.0V signal, or from a external voltage source that is placed on PIN 11 (but not more than V_{AIR} parameter for correct ACMP operation, see Section 5.0 Electrical Specifications) . Selection is made using a 4-bit value from NVM, reg<730:727> and the V_{REF} band select (reg<736>).

Reg <746> selects either the FSM1 or ADC as the source of the DAC.

The maximum ACMP output delay is 5∝s based on a minimum input difference of 2mV. The ACMP output is undefined for 100∝s after power up. When the power supply changes its value from higher to lower or vice versa (detect value is around 2.7V), then a special internal block (power regulator) starts up/down and influences V_{REF}. It means that ACMP with internal V_{REF} has output glitches if overvoltage is less than 50mV.

10.5 ACMP Output Modes

When IN+ has a greater voltage than IN-, the ACMP's output will be "1". Otherwise, that output will be a "0" signal. The ACMP of the SLG46400 has an offset voltage of ± 5mV.

10.6 ACMP 1uA Input Current Option

Both ACMP's can source 1∝A on their respected inputs. This feature is controlled by the following signals:

ACMP0_l1u_en, reg<721> for ACMP0

ACMP1_l1u_en, reg<726> for ACMP1

When either of these signals are equal to "1" the input will source a 1∝A current.

10.7 ACMP Low Bandwidth

Both ACMP's have a low bandwidth enable feature; this is controlled by the following signals:

ACMP0_low_bw, reg<811> for ACMP0

ACMP1_low_bw, reg<812> for ACMP1

When either of these signals are equal to "1" and the input frequency is more than 200kHz, the output retains its last value.

10.8 ACMP Frequency Bode Plot

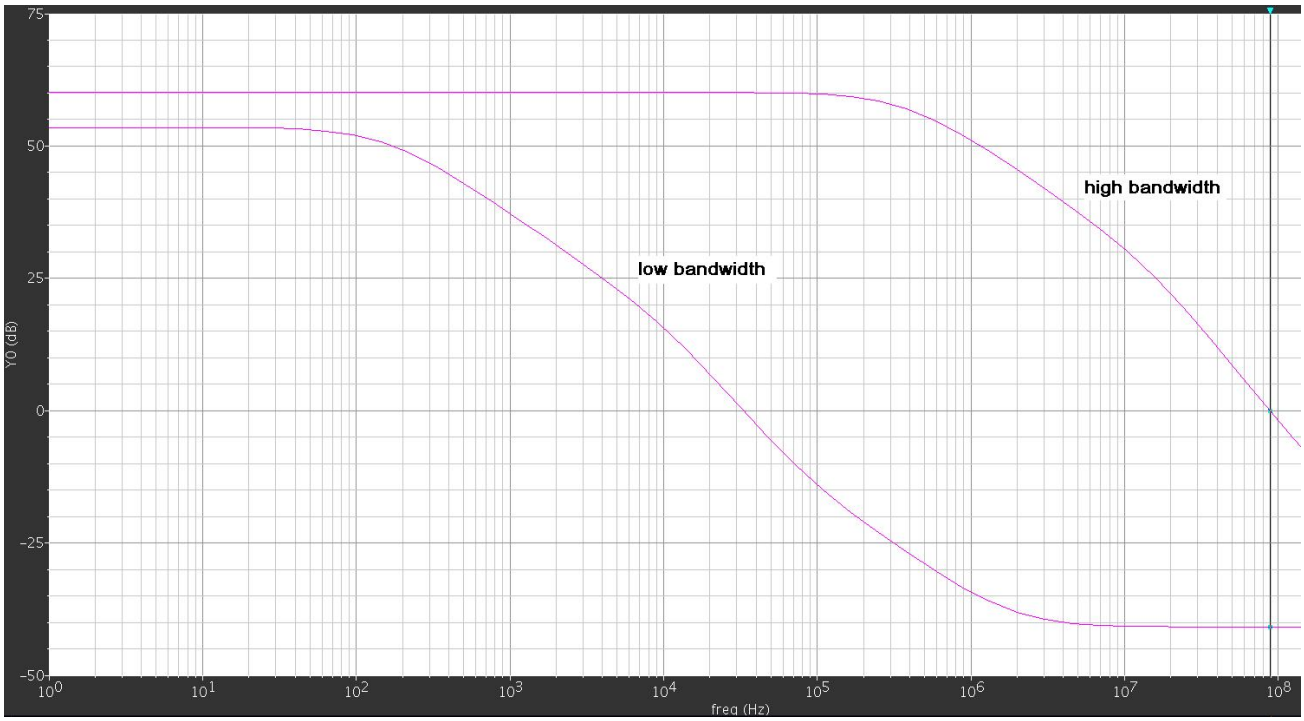

Figure 10. ACMP Frequency Bode Plot

10.9 ACMP Hysteresis

Both ACMP's have a hysteresis feature, where either the addition or subtraction of 12, 50, or 150 mV to the *IN-* signal will change the ACMP's output value. The amount of hysteresis is controlled as shown below:

ACMP0_hy_en, reg<732:731> when set to "01" will turn on the 12mV hysteresis,

- Output from "0" becomes "1" when IN+ IN- + 0.006V
- Output from "1" becomes "0" when IN+ IN- - 0.006V

ACMP0_hy_en, reg<732:731> when set to "10" will turn on the 50mV hysteresis,

- Output from "0" becomes "1" when IN+ IN- + 0.025V
- Output from "1" becomes "0" when IN+ IN- - 0.025V

ACMP0_hy_en, reg<732:731> when set to "11" will turn on the 150mV hysteresis,

- Output from "0" becomes "1" when IN+ IN- + 0.075V
- Output from "1" becomes "0" when IN+ IN- - 0.075V

ACMP1_hy_en, reg<734:733> when set to "01" will turn on the 12mV hysteresis,

- Output from "0" becomes "1" when IN+ IN- + 0.006V
- Output from "1" becomes "0" when IN+ IN- - 0.006V

ACMP1_hy_en, reg<734:733> when set to "10" will turn on the 50mV hysteresis,

- Output from "0" becomes "1" when IN+ IN- + 0.025V
- Output from "1" becomes "0" when IN+ IN- - 0.025V

ACMP1_hy_en, reg<734:733> when set to "11" will turn on the 150mV hysteresis,

- Output from "0" becomes "1" when IN+ IN- + 0.075V
- Output from "1" becomes "0" when IN+ IN- - 0.075V

10.10 ACMP0 & ACMP1 Register Settings

10.10.1 ACMP0 Register Settings

Table 14. ACMP0 Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
ACMP0_l1u_en	ACMP0 1∞A input current option	<721>	0: Disable 1: Enable
ACMP0_Vref_sel when reg<736> = 0	ACMP0 IN+ voltage select	<725:722>	0000: 50mV 0001: 100mV 0010: 150mV 0011: 200mV 0100: 250mV 0101: 300mV 0110: 400mV 0111: 500mV 1000: 600mV 1001: 700mV 1010: 800mV 1011: 900mV 1100: 1100mV 1101: 1300mV 1110: 1500mV 1111: Ext_Vref (PIN 11)
ACMP0_Vref_sel when reg<736> = 1	ACMP0 IN+ voltage select	<725:722>	0000: 30mV 0001: 70mV 0010: 100mV 0011: 130mV 0100: 170mV 0101: 200mV 0110: 270mV 0111: 330mV 1000: 400mV 1001: 470mV 1010: 530mV 1011: 600mV 1100: 730mV 1101: 870mV 1110: 1000mV 1111: Ext_Vref (PIN 11)
ACMP0_hy_en	ACMP0 hysteresis enable	<732:731>	00: Disabled (0mV) 01: Enabled (12mV) 10: Enabled (50mV) 11: Enabled (150mV)
ACMP_Vref_bd_sel	ACMP V_{REF} band select	<736>	0: 50mV to 1.5V range (only if V_{DD} > 3.0V) 1: 30mV to 1.0V range
ACMP0_analog_io_PGA_en	ACMP0 IN+ source selection	<739>, <735>	00: ACMP0 IN+ input from PIN3 01: ACMP0 IN+ input from PIN4 (PIN3 analog_io_en should be disabled) 10: ACMP0 IN+ input from PGA OUT 11: ACMP0 IN+ input from PGA IN
ACMP0_low_bw	ACMP0 low bandwidth enable	<811>	0: Disable 1: Enable

10.10.2 ACMP1 Register Settings

Table 15. ACMP1 Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
ACMP1_l1u_en	ACMP1 1∞A input current option	<726>	0: Disable 1: Enable
ACMP1_Vref_sel when reg<736> = 0	ACMP0 IN+ voltage select	<730:727>	0000: 50mV 0001: 100mV 0010: 150mV 0011: 200mV 0100: 250mV 0101: 300mV 0110: 400mV 0111: 500mV 1000: 600mV 1001: 700mV 1010: 800mV 1011: 900mV 1100: 1100mV 1101: 1300mV 1110: 1500mV 1111: Ext_Vref (PIN 11)
ACMP1_Vref_sel when reg<736> = 1	ACMP1 IN+ voltage select	<730:727>	0000: 30mV 0001: 70mV 0010: 100mV 0011: 130mV 0100: 170mV 0101: 200mV 0110: 270mV 0111: 330mV 1000: 400mV 1001: 470mV 1010: 530mV 1011: 600mV 1100: 730mV 1101: 870mV 1110: 1000mV 1111: Ext_Vref (PIN 11)
ACMP1_hy_en	ACMP1 hysteresis enable	<734:733>	00: Disable (0mV) 01: Enable (12mV) 10: Enable (50mV) 11: Enable (150mV)
ACMP_Vref_Bd_sel	ACMP V_{REF} band select	<736>	0: 50mV to 1.5V range (only if V_{DD} > 3.0V) 1: 30mV to 1.0V range
ACMP1_neg_src_sel	ACMP1 negative source select	<745>	0: From V_{REF} 1: From DAC output
ACMP1_DAC_src_sel	DAC input source select	<746>	0: from ADC 1: from FSM1
ACMP1_PGA_en	ACMP1's 0.5 gain enable	<747>	0: Disabled (IN+ input from PIN 4) 1: Enabled
ACMP1_low_bw	ACMP1 low bandwidth enable	<812>	0: Disable 1: Enable

11.0 Voltage Reference Out (V_{REF} Out)

The V_{REF} macro cell supplies an accurate reference voltage for the SLG46400.

11.1 V_{REF} Output

The output of the V_{REF} cell can be connected to PIN 10 as a buffered or non-buffered output. In order to use the V_{REF} cell within the SLG46400, the V_{REF} output enable signal (reg<741>) must be turned on.

When the op amp output buffer is enabled through the *Vrefo_buf_en* signal (reg<740>) the PIN 10 output voltage reference's impedance becomes 1k . With the op amp buffer switched out, the PIN 10 output voltage reference's impedance is 100k .

11.2 V_{REF} Sources

The value of V_{REF} can be set to either use $V_{DD}/3$ as a voltage source or by setting the ACMP0 to provide the desired voltage (50mV to 1.5V or 30mV to 1.0V is selectable). The V_{REF} macro cell uses ACMP0's negative input for the desired reference voltage.

11.3 V_{REF} Functional Diagram

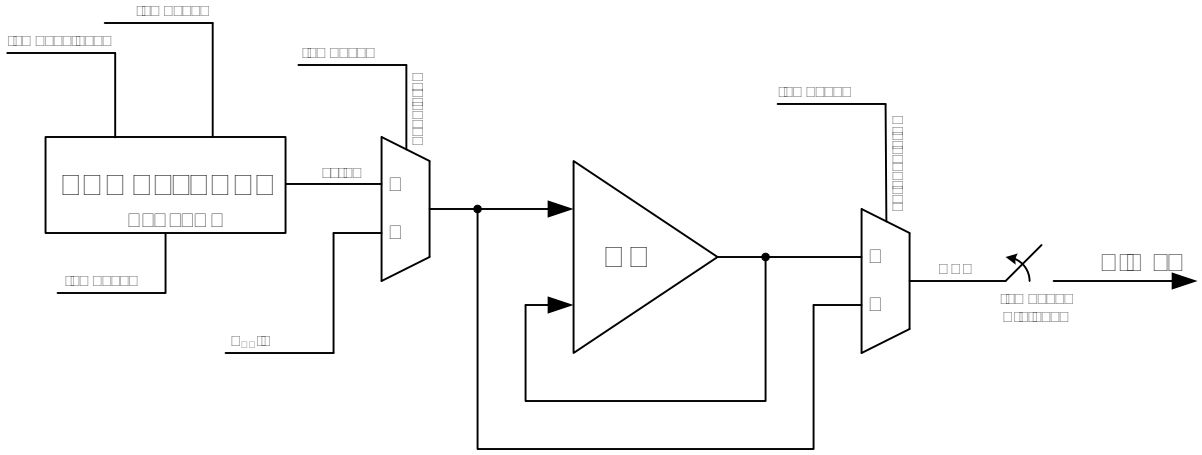

Figure 11. V_{REF} Functional Diagram

11.4 V_{REF} Register Settings

Table 16. V_{REF} Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
Vrefo_band_sel	V_{REF} band select for comparators	<736>	0: 50mV to 1.5V 1: 30mV to 1.0V
Vrefo_buf_en	V_{REF} output active buffer control	<740>	0: Enabled 1: Disabled
Vref_on	V_{REF} output enable	<741>	0: Disabled 1: Enabled
Vrefo_sel	V_{REF} output source select	<743>	0: ACMP0 reference voltage 1: $V_{DD}/3$

Refer to reg <725:722> for possible V_{REF} configurations.

12.0 Digital Comparator (DCMP) / Pulse Width Modulator (PWM)

The SLG46400 has three 8-bit digital comparator / pulse width modulator logic cells. Each of these three logic cells can be either a digital comparator (DCMP) or a pulse width modulator (PWM) independently of how the other two logic cells are defined.

Both the DCMP and PWM logic can operate at up to a frequency of 10MHz. The input power for the three logic cells is controlled independently by reg<760> for DCMP0/PWM0, reg<761> for DCMP1/PWM1 and reg<762> for DCMP2/PWM2.

PWM power down control is configured by reg <815:814> which is also shared with the ADC and OSC

12.1 DCMP Input Modes

The three DCMP logic cells have a positive (IN+) and a negative (IN-) input that are compared within the logic cell. The *inp* signal (connected to the IN+ input) takes the value from a 4:1 mux selection between the following signals:

- 8-bit signal from the ADC Parallel Output
- 8-bit signal from the S2P logic cell output (S2P<15:8> for DCMP0 and DCMP1 or S2P<7:0> for DCMP2)
- 8-bit signal from the FSM0<7:0>
- 8-bit user defined signal value.

The inn signal (connected to the IN- input) takes the value from an 8-bit user defined value for the DCMP operation.

12.2 DCMP Output Modes

The two 8-bit data inputs from IN+ and IN- are compared within the DCMP logic cells to produce the output and a *match* signal.

- If *inp* > *inn*, both *OUT*+ and *OUT* signals are equal to “1”, and *EQ* signal is equal to “0”
- If *inp* < *inn*, both *OUT*+ and *OUT* signals are equal to “0”, and *EQ* signal is equal to “0”
- If *inp* = *inn*, both *OUT*+ and *OUT* signals are equal to “0”, and *EQ* signal is equal to “1”

Both the *OUT*+ and *EQ* signals are triggered by the rising or falling edge of the *CKOSC* signal (defined by bit reg <759>).

12.3 PWM Input Modes

IN+ for the PWM is an 8-bit data string that can be selected from one of four sources;

- 8-bit signal from the ADC Parallel Output
- 8-bit signal from the S2P logic cell output (S2P<15:8> for DCMP0 and DCMP1 or S2P<7:0> for DCMP2)
- 8-bit signal from the FSM0<7:0>
- 8-bit user defined signal value.

IN-’s 8-bit data string for all PWMs is sourced from an 8-bit signal from CNT/DLY1.

12.4 PWM Output Modes

The output (*OUT+*) duty cycle can be set to either count down to 0% or count up to 100% and each PWM is independently controlled by the value of reg<758> (PWM0), reg<818> (PWM1), and reg<819> (PWM2). When both inputs are equal the output signal (*EQ*) will go high. The outputs (*OUT-* and *OUT+*) are non-overlapping.

When reg<758/818/819> = “0”

- PWM output duty cycle ranges from 0% to 99.61% and is determined by: Output Duty Cycle = IN+/256
- (IN+ = 0: output duty cycle = 0/256 = 0%; IN+ = 255: output duty cycle = 255/256 = 99.61%)
- Output signals are triggered by the rising or falling edge of the *CKOSC* signal (defined by bit reg <759>).

When reg<758/818/819> = “1”

- PWM output duty cycle ranges from 0.39% to 100% and is determined by Output Duty Cycle = (IN+ + 1)/256
- (IN+ = 0: output duty cycle = 1/256 = 0.39%; IN+ = 255: output duty cycle = 256/256 = 100%)
- Output signals are triggered by the rising or falling edge of the *CKOSC* signal (defined by bit reg <759>).

When IN+ = IN- then EQ = “1”

12.5 DCMP0/PWM0 Functional Diagram

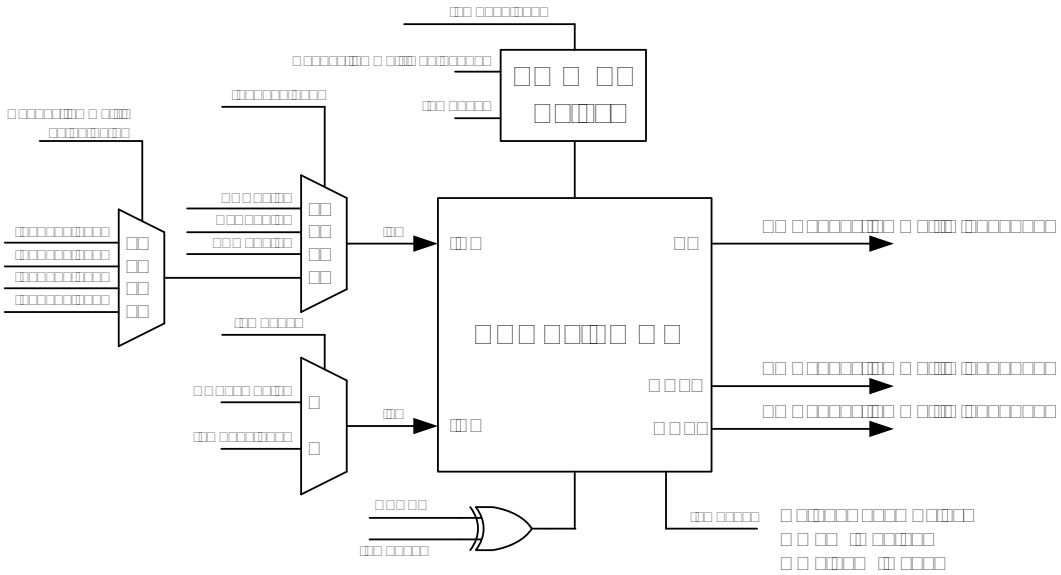

Figure 12. DCMP0/PWM0 Functional Diagram

12.6 DCMP1/PWM1 Functional Diagram

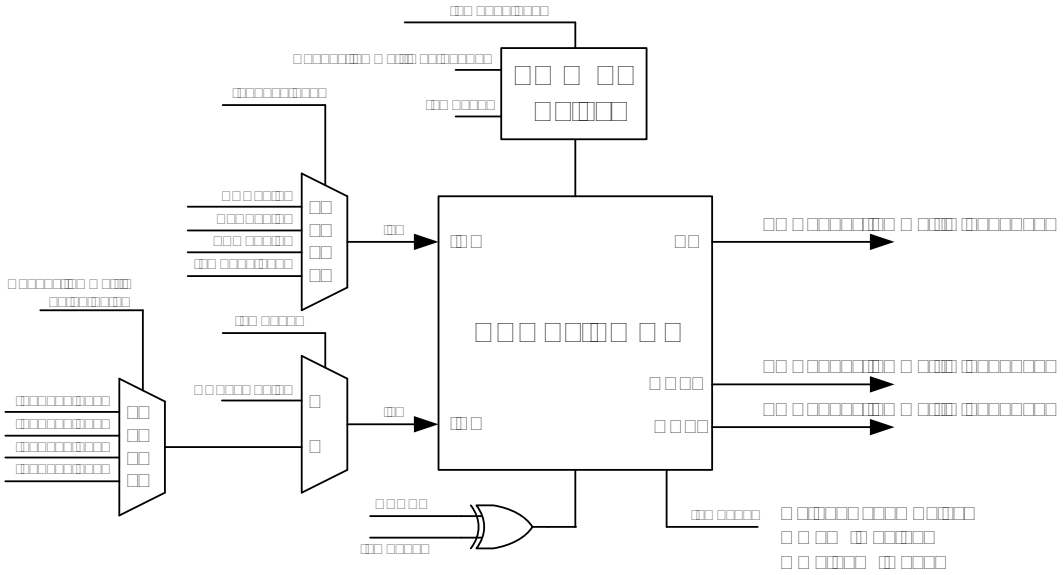

Figure 13. DCMP1/PWM1 Functional Diagram

12.7 DCMP2/PWM2 Functional Diagram

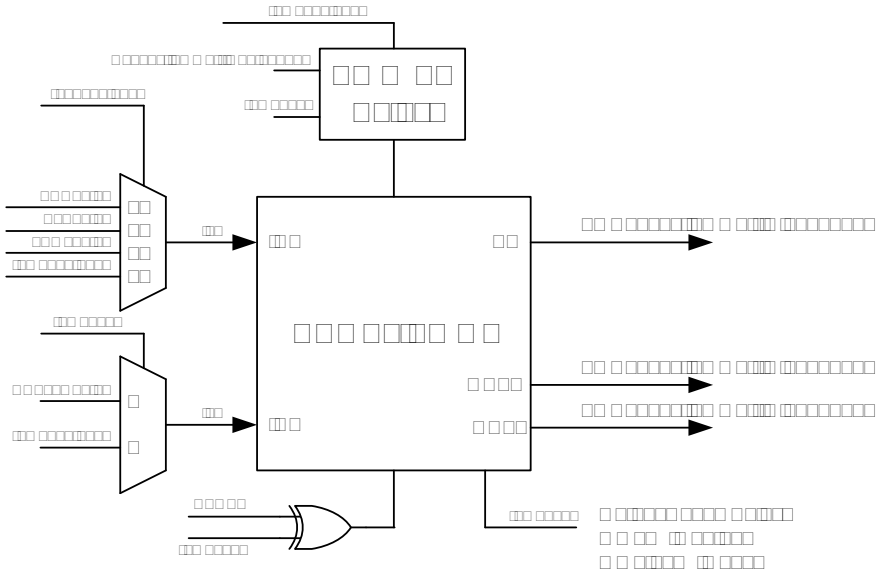

Figure 14. DCMP2/PWM2 Functional Diagram

12.8 PWM Dead Band Control

The dead band interval can be controlled with NVM bits (reg<757:755>). The typical dead band time starts at 8ns and can go to 64ns, increasing by 8ns intervals.

For the Delay dead band control, the dead time control range is:

$$T_D = (reg<757:755> + 1) \times 8ns$$

12.9 PWM Dead Band Control Timing Diagram

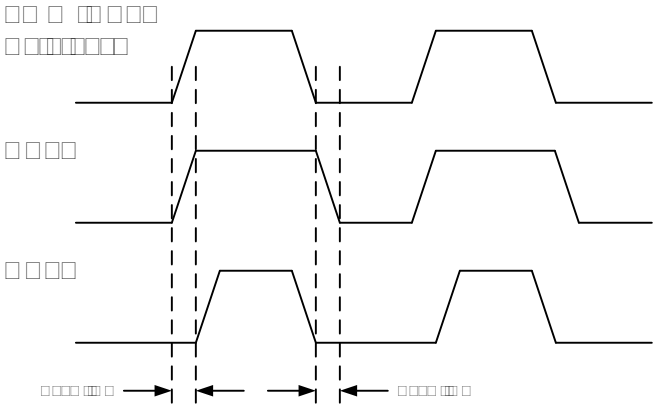

Figure 15. PWM Dead Band Control Timing Diagram

12.10 DCMP/PWM Power Down Control

The power down source for the DCMP/PWM logic cells is selected by reg <815:814> (shared with the ADC and PWM). When reg <815:814> = '00', the power down control DCMP/PWM logic cells comes from a register bit, otherwise it will come from connection matrix output 3 (in order for DCMP to turn on, this signal should be LOW). The DCMP/PWM logic cells can then be turned on or off individually with the appropriate register. The power down control of each logic cell is managed by the following register settings:

- When reg<760> = "0" DCMP0/PWM0 is powered down, when "1" logic cell is ON
- When reg<761> = "0" DCMP1/PWM1 is powered down, when "1" logic cell is ON
- When reg<762> = "0" DCMP2/PWM2 is powered down, when "1" logic cell is ON

12.11 DCMP/PWM Clock Invert Control

The three DCMP/PWM logic cells can invert the *CKOSC* input signal during the compare or PWM function. Reg<759> is used to control the three logic cells clock inversion.

12.12 DCMP/PWM Register Settings

Table 17. DCMP/PWM Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
PWM_db_sel	PWM Deadband Select	<757:755>	000:8ns 001:16ns 010:24ns 011:32ns 100:40ns 101:48ns 110:56ns 111:64ns
PWM0_mode_sel	PWM0 mode select	<758>	0: count down to 0% 1: count up to 100%
PWMDCMP_clk_in	PWM/DCMP clock invert	<759>	0: Disable 1: Enable
PWMDCMP0_pd	PWM0/DCMP0 power down control	<760>	0: power down 1: power on
PWMDCMP1_pd	PWM1/DCMP1 power down control	<761>	0: power down 1: power on
PWMDCMP2_pd	PWM2/DCMP2 power down control	<762>	0: power down 1: power on
PWMDCMP0_pos_in	PWM0/DCMP0 positive input source select	<764:763>	00: from ADC 01: from S2P 10: from FSM0 11: 8-bit user defined (selected through matrix)
PWMDCMP1_pos_in	PWM1/DCMP1 positive input source select	<766:765>	00: from ADC 01: from S2P 10: from FSM0 11: 8-bit user defined
PWMDCMP2_pos_in	PWM2/DCMP2 positive input source select	<768:767>	00: from ADC 01: from S2P 10: from FSM0 11: 8-bit user defined
PWMDCMP0_neg_in	PWM0/DCMP0 negative input source select	<769>	0: from CNT1 ramp (for PWM) 1: 8-bit user defined
PWMDCMP1_neg_in	PWM1/DCMP1 negative input source select	<770>	0: from CNT1 ramp (for PWM) 1: 8-bit user defined (selected through matrix)
PWMDCMP2_neg_in	PWM2/DCMP2 negative input source select	<771>	0: from CNT1 ramp (for PWM) 1: 8-bit user defined
ADC_PWM_OSC_pd_src_sel	ADC/PWM/OSC power down source select	<815:814>	00: ADC pd from matrix out <3>, PWM pd from register 01: PWM pd from matrix out <3>, ADC pd from register 10: ADC & PWM pd from matrix out <3> 11: OSC pd from matrix out <3>, ADC & PWM pd from register
PWM1_mode_sel	PWM1 mode select	<818>	0: count down to 0% 1: count up to 100%
PWM2_mode_sel	PWM2 mode select	<819>	0: count down to 0% 1: count up to 100%

13.0 Counters/Delay Generators (CNT/DLY)

There are four configurable counters/delay generators in the SLG46400. Three of these four logic cells can be either a 14-bit counter (CNT) or a delay generator (DLY) and one can be a 8-bit counter or delay generator independently of how the other three logic cells are defined.

13.1 Counter Functionality

CNT0, CNT1 and CNT2 each have a 14-bit input data source, while CNT3 has a 8-bit input data source.

CNT2 and CNT3's inputs can be sourced from the NVM, the ADC, or the S2P, while CNT0 and CNT1's inputs can be sourced from the connection matrix. The clock can be sourced from either the internal RC Oscillator (with data divider for CNT1) or from another connection matrix output.

The counters output their data to either the PWM or to the S2P. The supported counter functions include (FSM only): count UP, count DOWN, KEEP, and LOAD DATA (taken from ADC, S2P or Counter Data). The four counters can also function as frequency dividers, FSM (CNT2 and CNT3), or PWM ramp (CNT1), while captured data is outputted to S2P.

In counter mode, it is in DOWN mode. the count UP/DOWN, KEEP, and LOAD signals in CNT2 and CNT3 must be tied to ground and the RC OSC should be forced ON if the clock is sourced from the internal RC OSC for the counter to work.

For proper counter functionality, the force signals (CNT0_force reg<588>, CNT1_force reg<610>, CNT2_force reg<633>, CNT3_force reg<655>) should be configured as "1" (Force Power On) for any block configured as counter.

Example: for CNT3 to use the CNT/DLY block in Counter mode the following settings should be applied:

- CNT/DLY3 Output Source Select (*output_src_sel*) set to **Counter Mode** (reg <656> = "1")
- CNT3 Enable (*CNT3_force*) set to **Force Power On** (reg <655> = "1")
- Reset Source (*rst_src_sel*) should be set to **Edge Detect** mode (reg<654> = "1")
- Edge Select can be set to Both, Falling, or Rising (reg <669:668>)
- Additionally, make sure that RC Osc is in operating mode. The RC Osc may need to be set to Force On as well.

Since CNT1 and CNT2 can be used for a PWM ramp function, the PWM power down signal will control the force power to those macro cells.

13.2 CNT2 and CNT3 Reset Source Select

When reg <632> = "1" (for CNT2) or reg <654> = "1" (for CNT3), the reset signal for CNT2 or CNT3 is sourced from the falling and/or rising edge active signal from the connection matrix and only applies when used for counter function. When used in the counter function and reg <632> / reg <654> = "0" then the reset signal is sourced from the POR.

However when the counter cells are used for a delay function, reg <632> / reg <654> must be set to 0.

13.3 Counters Functional Diagram

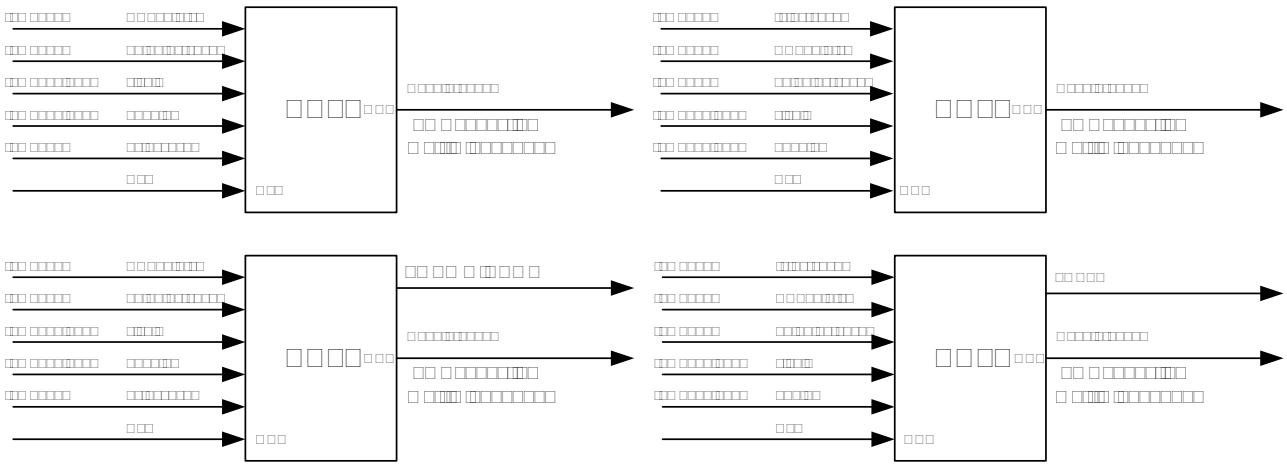

Figure 16. Counters Functional Diagram

13.4 Counter Timing

Each of the counters behave as a frequency divider, where the output clock (*Div_clk_out*) is result of the input clock (*CLK*) being divided by the value of the Counter Control Data (CNTx_d<13:0> + 1) for CNT0, CNT1 and CNT2. While CNT3 uses a Counter Control Data value of (CNTx_d<7:0> + 1). F_{CLK} comes from the RC Oscillator which has a /4, /8, and /12 function for all counter logic cells.

For CNT0:

$$div\_clk\_out0 = F_{CLK} / (reg<606:593> + 1)$$

For CNT1:

$$div\_clk\_out1 = F_{CLK} / (reg<628:615> + 1)$$

For CNT2:

$$div\_clk\_out2 = F_{CLK} / (reg<651:638> + 1)$$

For CNT3:

$$div\_clk\_out2 = F_{CLK\_IN} / (reg<667:660> + 1)$$

Note: For proper functionality of each Counter/Delay cell, each respective CNTx_d<13:0> or CNTx_d<7:0> must have a value of greater than '1'.

An example waveform is shown below (for either CNT0, CNT1 or CNT2) where the output clock goes high for only one of the input clock's cycles over a time period that is equal to the Counter Control Data (CNTx_d<13:0> +1). The waveform would be the same for CNT3, except the timing would be based on 8-bits of data rather than 14-bits.

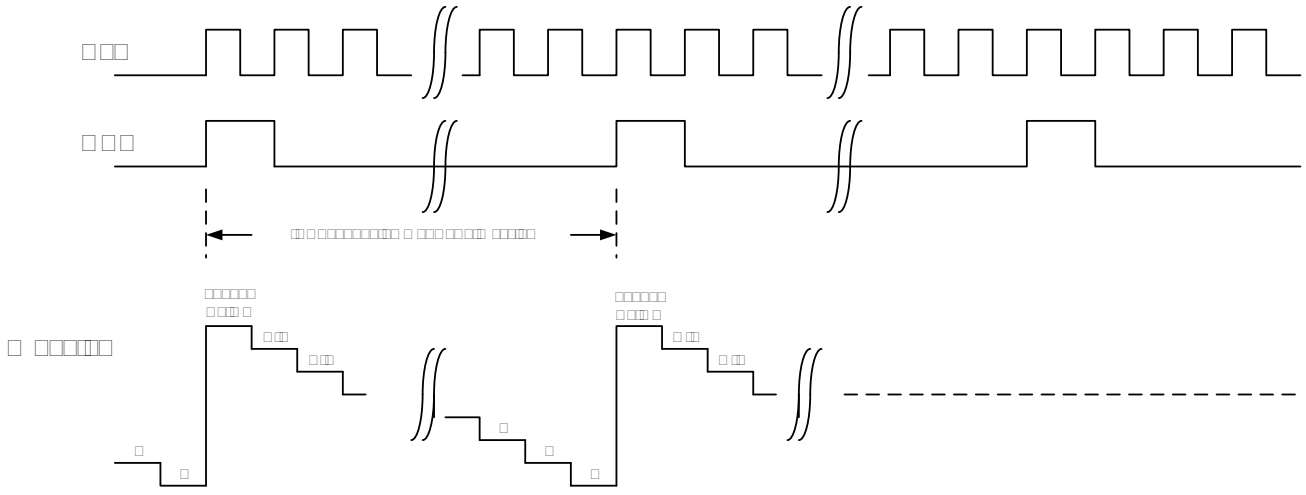

Figure 17. Counter Behavior

13.5 CNT0/DLY0 and CNT1/DLY1 Register Settings

Table 18. CNT0/DLY0 and CNT1/DLY1 Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
CNT0_en	CNT0 Enable (Force CNT0 power on)	<588>	0: Auto Power On (Power on as needed) 1: Force Power On (Power always on)
CNT_DLY0_out_src_sel	CNT/DLY0 Output Source Select	<589>	0: Delay Output 1: Counter Output
CNT0_CLK_sel	CNT/DLY0 Clock Source Select	<592:590>	000: Internal RC OSC Clock 001: CLOCK/4 010: CLOCK/12 011: CNT1 Overflow Output 1X0: CLOCK/8 1X1: External Clock
CNT0_d<13:0>	CNT0 Control Data/DLY0 Time Control	<606:593>	1-16384: (delay time = (counter control data + 1) / freq)
DLY0_d_mode_sel	DLY0 Mode Select	<608:607>	00: delay on both falling and rising edges 01: delay on falling edge only 10: delay on rising edge only 11: no delay on either falling or rising edges
DLY0_in_sel	DLY0 Input Function Select	<609>	0: for delay input signal 1: for counter0 external clock
CNT1_en	CNT1 Enable (Force CNT1 power on)	<610>	0: Auto Power On (Power on as needed) 1: Force Power On (Power always on)
CNT_DLY1_out_src_sel	CNT/DLY1 Output Source Select	<611>	0: Delay Output 1: Counter Output
CNT1_CLK_sel	CNT/DLY1 Clock Source Select	<614:612>	000: Internal RC OSC Clock 001: CLOCK/4 010: CLOCK/12 011: CNT2 Overflow Output 1X0: CLOCK/8 1X1: External Clock
CNT1_d<13:0>	CNT1 Control Data/DLY1 Time Control	<628:615>	1-16384: (delay time = (counter control data + 1) / freq)
DLY1_d_mode_sel	DLY1 Mode Select	<630:629>	00: delay on both falling and rising edges 01: delay on falling edge only 10: delay on rising edge only 11: no delay on either falling or rising edges
DLY1_in_sel	DLY1 Input Function Select	<631>	0: for delay input signal 1: for counter1 external clock

13.6 CNT2/DLY2 and CNT3/DLY3 Register Settings

Table 19. CNT2/DLY2 and CNT3/DLY3 Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
CNTDLY2_rst_sel	CNT/DLY2 Reset Source Select	<632>	0: From Delay Cell 1: From Edge Detect When reg <633> = 1, then reg <634> must be set to 1 and DLY2 input must be tied to ground
CNT2_en	CNT2 Enable (Force CNT2 power on)	<633>	0: Auto Power On (Power on as needed) 1: Force Power On (Power always on)
CNT_DLY2_out_src_sel	CNT/DLY2 Output Source Select	<634>	0: Delay Output 1: Counter Output
CNT2_CLK_sel	CNT/DLY2 Clock Source Select	<637:635>	000: Internal RC OSC Clock 001: CLOCK/4 010: CLOCK/12 011: CNT3 Overflow Output 1X0: CLOCK/8 1X1: External Clock
CNT2_d<13:0>	CNT2 Control Data/DLY2 Time Control	<651:638>	1-16384: (delay time = (counter control data + 1) / freq)
DLY2_d_mode_sel	DLY2 Mode Select	<653:652>	00: delay on both falling and rising edges 01: delay on falling edge only 10: delay on rising edge only 11: no delay on either falling or rising edges
CNTDLY3_rst_sel	CNT/DLY3 Reset Source Select	<654>	0: From Delay Cell 1: From Edge Detect When reg <655> = 1, then reg <656> must be set to 1 and DLY3 input must be tied to ground
CNT3_en	CNT3 Enable (Force CNT3 power on)	<655>	0: Auto Power On (Power on as needed) 1: Force Power On (Power always on)
CNT_DLY3_out_src_sel	CNT/DLY3 Output Source Select	<656>	0: Delay Output 1: Counter Output
CNT3_CLK_sel	CNT/DLY3 Clock Source Select	<659:657>	000: Internal RC OSC Clock 001: CLOCK/4 010: CLOCK/12 011: CNT0 Overflow Output 1X0: CLOCK/8 1X1: External Clock
CNT3_d<7:0>	CNT3 Control Data/DLY3 Time Control	<667:660>	1-256: (delay time = (counter control data + 1) / freq)
DLY3_d_mode_sel	DLY3 Mode Select	<669:668>	00: delay on both falling and rising edges 01: delay on falling edge only 10: delay on rising edge only 11: no delay on either falling or rising edges

13.7 CNT2 as a Finite State Machine (FSM0)

CNT2 can be used as a 14-bit Finite State Machine, which has features for UP/DOWN/KEEP control and loading data select.

- When UP/DOWN = “1“: CNT2 is in up-counting mode, after POR or reset, the Q value will count from 0 to 16383, then the N is loaded (d <13:0>) and the Q value count from loaded data N to 16383. When Q is equal to 16383, OUT generates a single clock cycle pulse as shown in Figure (FSM Behavior).
- When UP/DOWN = “0“: CNT2 is in down-counting mode, the Q value will count from the loaded data value of N (based on reg<651:638> + 1) to 0. When Q is equal to 0, OUT generates a single clock cycle pulse as shown in Figure (FSM Behavior).
- When KEEP = “1“: Q will stay at its current value.
- When DLY IN has a transition (edge mode is dependent on reg<653:652>), a narrow pulse signal will be generated which will reset the CNT2 state to “0“.
- For FSM operation, the Reset Source (*rst_src_sel*) should be set to Edge Detect in Counter Mode and user will be able to select rising, falling, or both edge (if resetting is needed), or tie reset input to ground (if resetting is not needed).
- LOAD function is synchronous to Counter’s clock signal. For LOAD event to happen there should be a rising edge on the clock input of the FSM and LOAD node should be HIGH.

13.8 FSM0 (CNT2) Functional Diagram

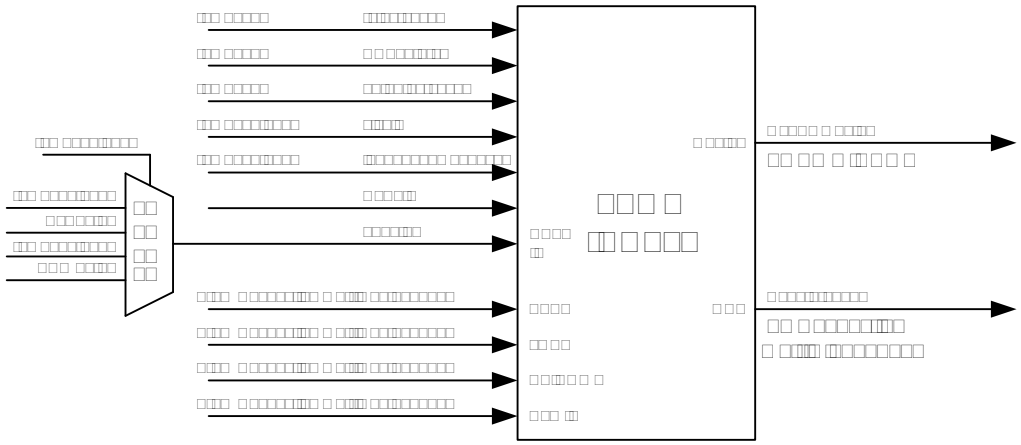

Figure 18. FSM0 (CNT2) Functional Diagram

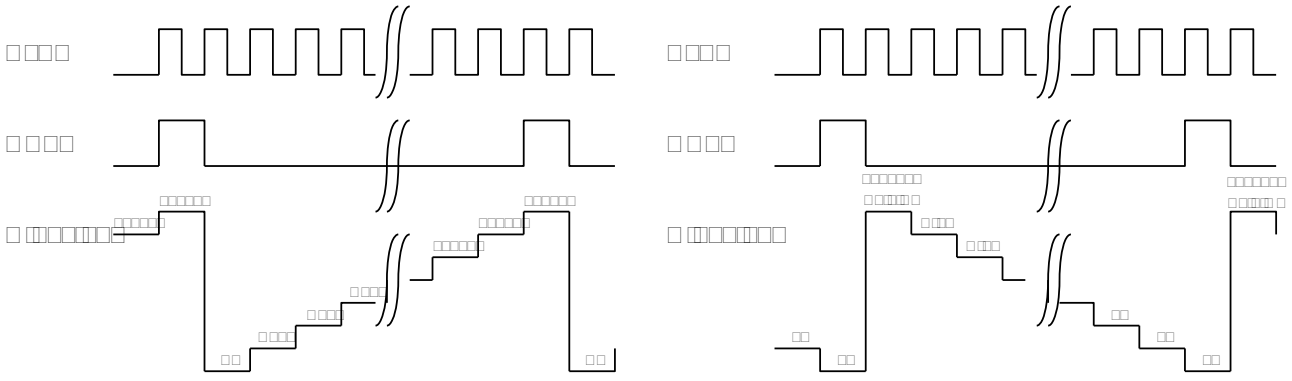

Figure 19. FSM0 Behavior

13.9 CNT3 as a Finite State Machine (FSM1)

CNT3 can be used as a 8-bit Finite State Machine, which has features for UP/DOWN/KEEP control and loading data select.

- When UP/DOWN = “1“: CNT3 is in up-counting mode, after POR or reset, the Q value will count from 0 to 255, then the N is loaded (d <13:0>) and the Q value count from loaded data N to 255. When Q is equal to 255, OUT generates a single clock cycle pulse as shown in Figure (FSM Behavior).
- When UP/DOWN = ”0”: CNT3 is in down-counting mode, the Q value will count from the loaded data value of N (based on reg<667:660> + 1) to ”0”. When Q is equal to 0, OUT generates a single clock cycle pulse as shown in Figure (FSM Behavior).
- When KEEP = ”1”: Q will stay at its current value.
- When DLY IN has a transition (edge mode is dependent on reg<669:668>), a narrow pulse signal will be generated which will reset the CNT3 state to “0”.
- For FSM operation, the Reset Source (*rst_src_sel*) should be set to Edge Detect in Counter Mode and user will be able to select rising, falling, or both edge (if resetting is needed), or tie reset input to ground (if resetting is not needed).
- LOAD function is synchronous to Counter’s clock signal. For LOAD event to happen there should be a rising edge on the clock input of the FSM and LOAD node should be HIGH.

13.10 FSM1 (CNT3) Functional Diagram

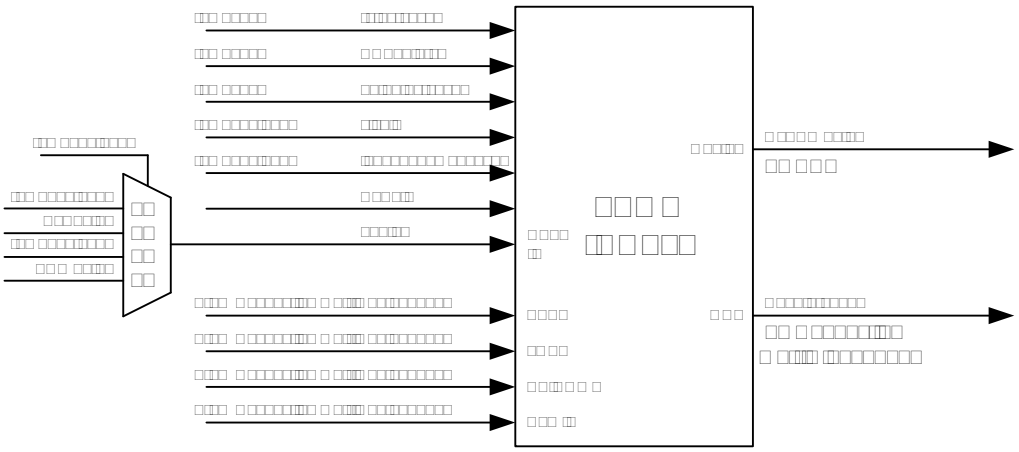

Figure 20. FSM1 (CNT3) Functional Diagram

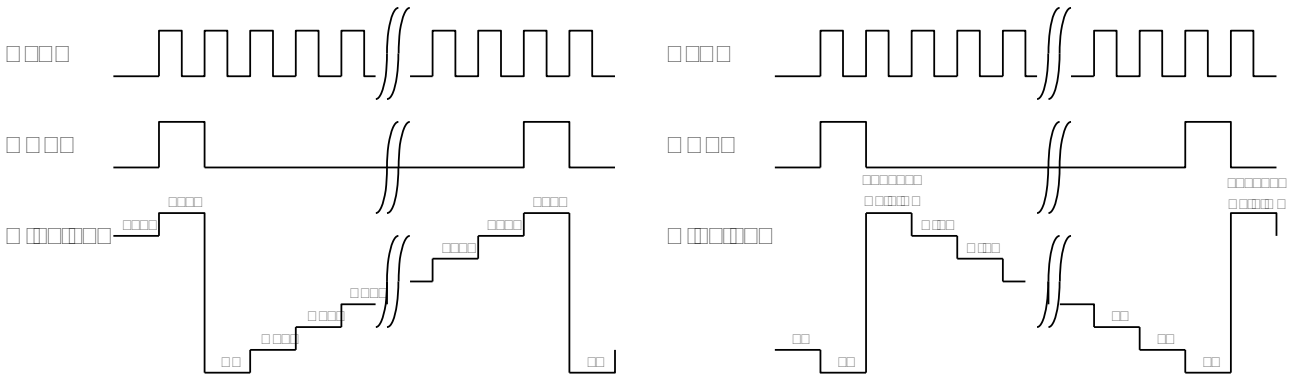

Figure 21. FSM1 Behavior

13.11 FSM Register Settings

Table 20. FSM Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
FSM0_In_sel	FSM0 Input Data Select	<752:751>	00: from NVM data 01: from S2P 10: Reserved 11: from ADC
FSM1_In_sel	FSM1 Input Data Select	<754:753>	00: from NVM data 01: from S2P 10: Reserved 11: from ADC

13.12 Delay Cell Functionality

The four Delay Cells in the SLG46400 can operate independently or they can be cascaded with one another to achieve longer time delays. DLY0, DLY1 and DLY2 use a 14-bit data source, while DLY3 uses a 8-bit data source. Each delay cell can be triggered from a rising edge transition, a falling edge transition, or a transition in either direction.

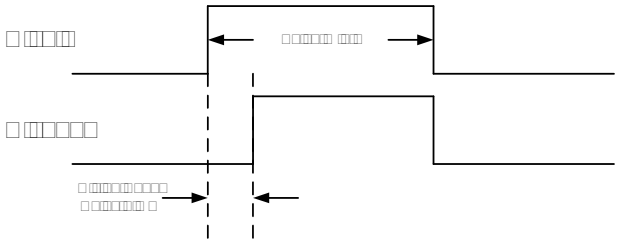

Figure 22. Delay Cells - Long Pulse, Rising Edge

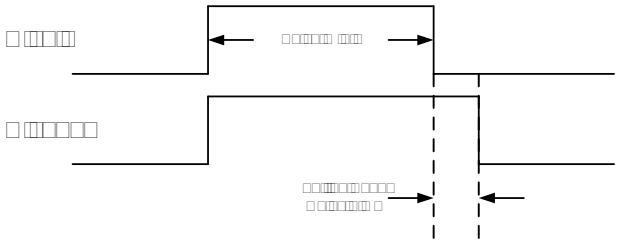

Figure 23. Delay Cells - Long Pulse, Falling Edge

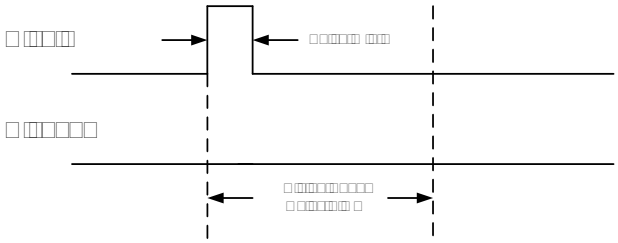

Figure 24. Delay Cells - Short Pulse, Rising Edge

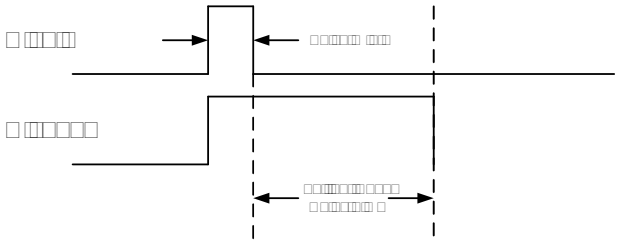

Figure 25. Delay Cells - Short Pulse, Falling Edge

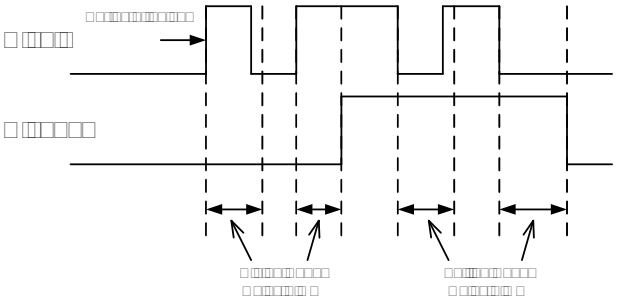

Figure 26. Delay Cells - Short Pulse, Rising and Falling Edge

The clock frequency and counter data are used to set the desired output delay. Each time delay cell's input and output can be sourced from any user defined signal in the SLG46400.

All Delay blocks have some of the registers shared with Counter mode block configuration. For correct Delay operation, Counters' force signals (CNT0_force reg<588>, CNT1_force reg<610>, CNT2_force reg<633>, CNT3_force reg<655>) should be set to "0" (Auto Power On (Power on as needed)).

13.13 Delay Cells Functional Diagram

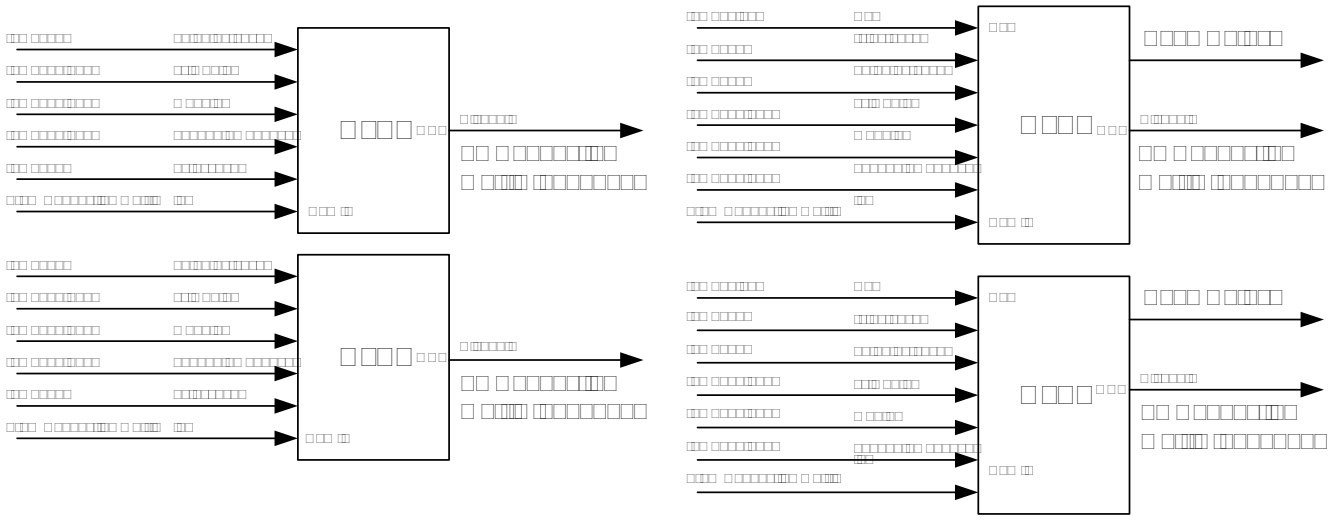

Figure 27. Delay Cells Functional Diagram

13.14 Delay Timing

The delay timing of each logic cell is determined by the frequency of the RC Oscillator and the Delay Time Control registers (reg<606:593> for DLY0, reg<628:615> for DLY1, reg<651:638> for DLY2, and reg<667:660> for DLY3). The formulas below list the timing delay equations for each logic cell. Clock source comes from the external clock (from matrix), CNT1/DLY1, or RC Oscillator which has a /4, /8, and /12 function.

For DLY0:

$$T_{DLY0} = (1/F_{OSC}) * (reg<606:593> + 1)$$

For DLY1:

$$T_{DLY1} = (1/F_{OSC}) * (reg<628:615> + 1)$$

For DLY2:

$$T_{DLY2} = (1/F_{OSC}) * (reg<651:638> + 1)$$

For DLY3:

$$T_{DLY2} = (1/F_{OSC}) * (reg<667:660> + 1)$$

Note: In order for these equations above to be valid the pulse width must be larger than the total rising and falling edge delay times.

14.0 Programmable Delay (PDLY)

The SLG46400 has a programmable time delay logic cell available that can generate a maximum delay of 200ns. The programmable time delay cell has four delay cells with a typical value of 20ns per cell (based on a V_{DD} of 3.3V). The delay cells are tied in series where the output of each delay cell goes to the next delay cell and to a 4-input mux that is controlled by reg<537:536>.

14.1 Programmable Delay Functional Diagram

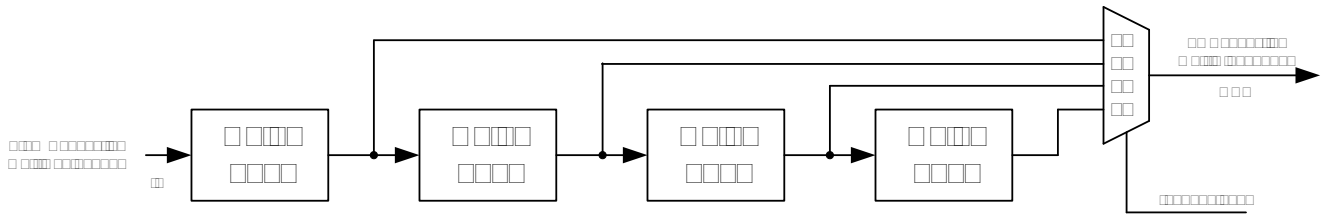

Figure 28. Programmable Delay Functional Diagram

14.2 VDD vs. Typical Time Delay

Table 21. V_{DD} vs. Typical Time Delay per 1 Cell.

V_{DD} (V)	Typical Time Delay (ns)
5.0V	10ns
3.3V	20ns
1.8V	50ns

14.3 Programmable Delay Register Settings

Table 22. Programmable Delay Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
PDLY_sel	PDLY value section	<537:536>	00: 1 delay cell active 01: 2 delay cells active 10: 3 delay cells active 11: 4 delay cells active

15.0 Pipe Delay (PD)

The SLG46400 has a pipe delay logic cell available that can generate up to three individual delays concurrently:

- a single delay stage on 1 PIPE OUT
- 3, 5, 7, or 11 stages of delay on OUT0
- 2, 4, 8, 12 stages of delay on OUT1

The pipe delay cell is built from 12 D Flip-Flop logic cells that provide the three delay options. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by reg <810:809> for OUT0 and reg <821:820> for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46400 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46400). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

15.1 Pipe Delay Functional Diagram

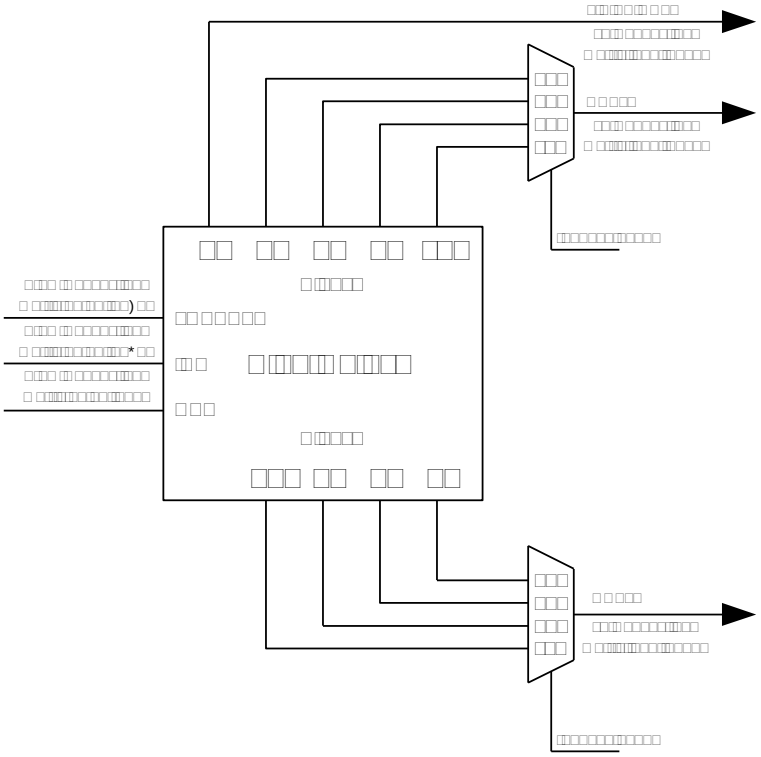

Figure 29. Pipe Delay Functional Diagram

15.2 Pipe Delay Register Settings

Table 23. Pipe Delay Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
PD_sela	Pipe Delay number select	<810:809>	00: 3 pipes 01: 5 pipes 10: 7 pipes 11: 11 pipes
PD_selb	Pipe Delay number select	<821:820>	00: 2 pipes 01: 4 pipes 10: 8 pipes 11: 12 pipes

16.0 Clock Management

The RC Oscillator (RC OSC) of the SLG46400 provides an internal clock to the ADC, PWM/DCMP, Delays and Counter logic cells. It has a frequency range of 27kHz – 10MHz which can be adjusted through the *RCO_freq_cont* registers <586:583>.

16.1 Clock Management Functional Diagram

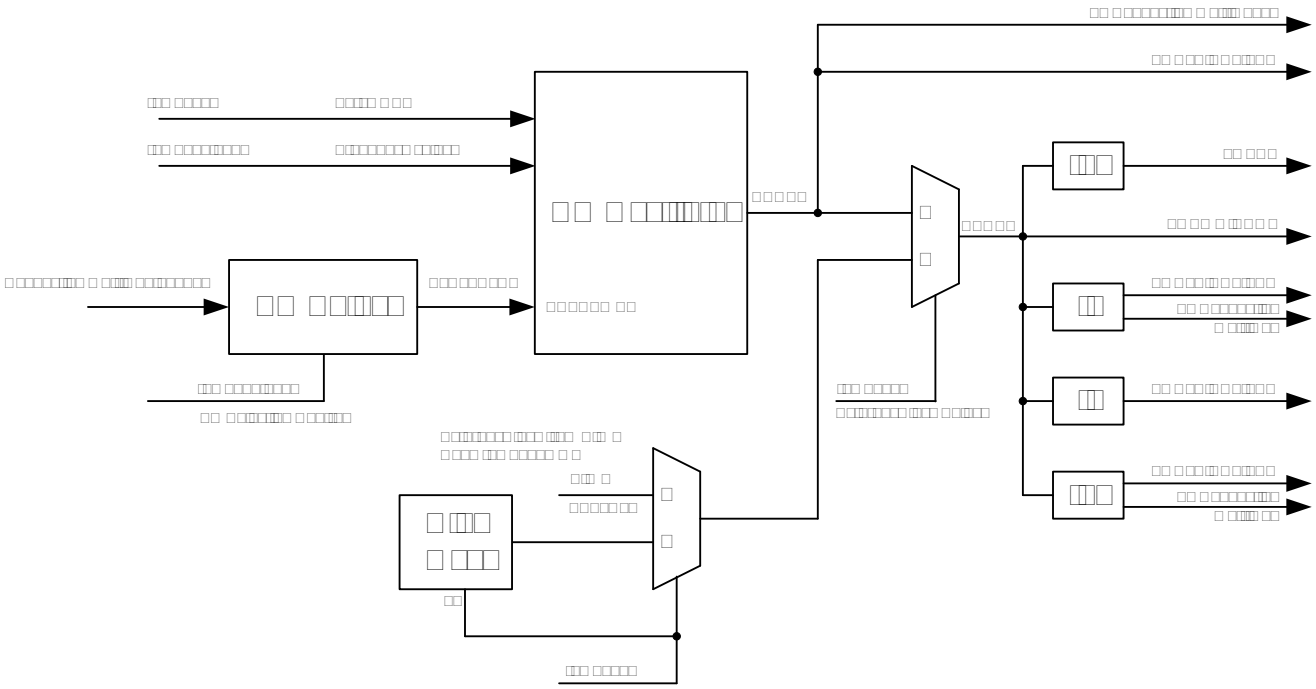

Figure 30. Clock Management Functional Diagram

16.2 RC OSC Power Down Control

The power down source for the RC OSC logic cell is selected by reg <815:814> (shared with the DCMP and ADC). When reg <815:814> = ‘11’, the power down control comes from the connection matrix. The SHARED PD signal should be LOW in order to turn on the RC OSC. This signal has the highest priority and if the RC OSC is off, no other blocks of registers will be available.

16.3 RC OSC Dividers Control

RC OSC dividers output to matrix can be controlled through setting the reg <816>. When the reg <816> = ‘0’ than the deviders output to matrix is allowed. When the reg <816> = ‘1’ than the deviders output to matrix will be disabled if no other blocks use them (CNT, DLY and so on).

16.4 Ring Oscillator and External Clock from PIN 5

In addition to the internal RC Oscillator, GreenPAK2 has an internal Ring Oscillator that operates on a single fixed frequency that ranges between 2 MHz and 27 MHz. This value varies from chip to chip and with VDD and temperature. To enable this function reg<587> and reg<670> should be set to ‘1’.

It is also possible to use the external clock signal from PIN5 as the source. To enable the external clock from PIN5, configure reg<587> = ’1’ and reg<670> = ’0’.

In either case, the Ring Oscillator or external clock signal will feed the ADC through an internal /64 divider, the PWM/DCMP blocks and CNT/DLY/FSM blocks through /4, /8, and /12 frequency dividers, and the matrix through /4 and /12 frequency dividers. Direct connection to matrix is not possible (CNT/DLY/FSM blocks and matrix will be fed from the internal RC Oscillator without dividers).

16.5 RC OSC Frequency Selection

Table 24. RC OSC Typical Frequency Selection

reg <586:583>	V_{DD} = 1.8V			V_{DD} = 3.3V			V_{DD} = 5.0V		
	Min (kHz)	Typ (kHz)	Max (kHz)	Min (kHz)	Typ (kHz)	Max (kHz)	Min (kHz)	Typ (kHz)	Max (kHz)
0000	25.72	28.77	31.83	25.47	28.49	31.52	25.84	28.73	31.63
0001	50.19	55.71	61.22	49.32	54.75	60.19	49.90	55.14	60.38
0010	72.12	79.92	87.73	70.30	78.06	85.82	71.08	78.55	86.02
0011	111.24	124.85	138.46	106.95	120.57	13.20	107.76	120.89	134.01
0100	129.01	142.81	156.61	126.81	140.46	154.11	128.28	141.46	154.64
0101	191.74	213.47	235.21	187.08	209.01	230.94	189.17	209.85	230.53
0110	204.31	228.1	251.89	199.13	223.17	247.21	201.40	223.92	246.45
0111	278.36	316.49	354.63	269.60	308.17	346.74	273.93	309.07	344.21
1000	422.46	481.35	540.23	425.66	486.70	547.74	432.35	493.01	553.67
1001	523.27	596.94	670.60	527.09	60.85	684.60	539.47	616.26	693.05
1010	571.54	654.32	737.10	576.15	665.78	755.41	591.66	678.24	764.81
1011	652.33	749.54	846.74	659.18	766.24	873.30	678.30	781.37	884.43
1100	1942.36	2205.05	2467.74	1980.05	2250.95	2521.85	2032.54	2296.34	2560.14
1101	2515.21	2866.21	3217.21	2567.59	2932.52	3297.44	2636.11	2990.74	3345.38
1110	592.77	6478.03	7363.28	5721.18	6708.73	7696.28	5837.26	6836.42	7835.58
1111	6866.55	8016.51	9166.46	7015.74	8337.72	9659.71	7149.45	8484.86	9820.27

16.6 RC OSC Register Settings

Table 25. RC OSC Register Settings

Signal Name	Signal Function	Register Bit Address	Register Definition
RCO_force	Force Oscillator Power On	<582>	0: Auto Power On (Power on as needed) 1: Force Power On (Power always on)
RCO_fs	Oscillator Frequency Control	<586:583>	See Frequency Selection Table
RCO_clk_sel	External Clock Source Select	<587>	0: Internal RC OSC Clock 1: External Clock
RCO_ring_en	Ring Oscilator Enable	<670>	0: Disable 1: Enable (ADC/PWM/DCMP/Clock/4, Clock/8, and Clock/12 clock source is selected from the ring oscillator)
ADC_PWM_OSC_pd_src_sel	ADC/PWM/OSC power down source select	<815:814>	00: ADC pd from matrix out <3>, PWM pd from register 01: PWM pd from matrix out <3>, ADC pd from register 10: ADC & PWM pd from matrix out <3> 11: OSC pd from matrix out <3>, ADC & PWM pd from register
RCO_div_ctrl	Oscillator Dividers Control	<816>	0:Oscillator Dividers Enabled 1: Oscillator Dividers Diasbled

17.0 Slave SPI - Serial to Parallel / Parallel to Serial Converter (S2P)

The Slave SPI data can be communicated between the SLG46400 and the larger system design through either the serial to parallel or parallel to serial interface. The S2P has two 16-bit registers (2 bytes) that are used for data transfer. The external clock signal comes from PIN 5 and the nCSB (Enable Control Signal) comes from the Connection Matrix Out.

S2P uses edge detection from the *DLY3* signal for capturing the input data.

17.1 S2P Functional Diagram

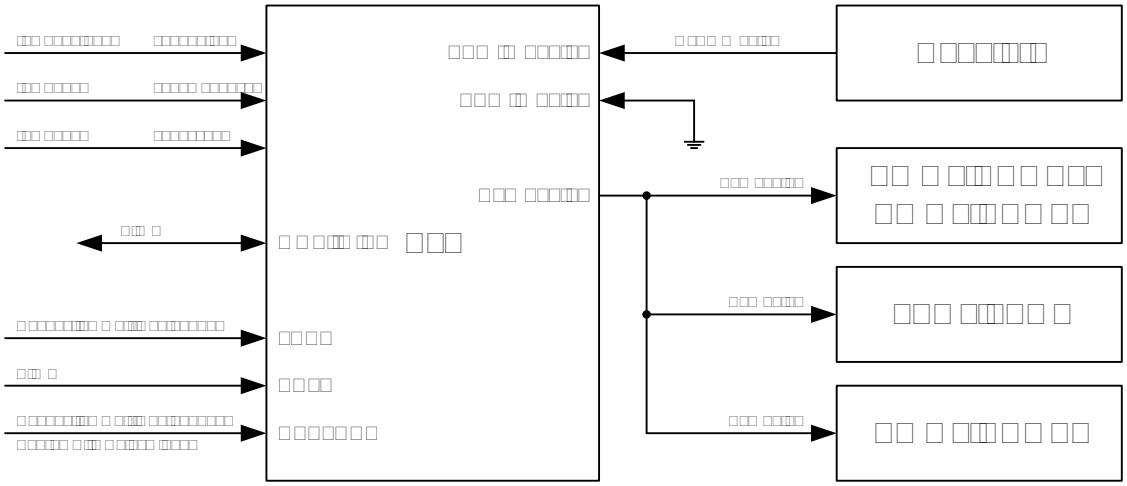

Figure 31. S2P Functional Diagram

17.2 Serial to Parallel Operation

For serial to parallel operation (S2P), the serial data in (MOSI) comes from PIN 6 of the SLG46400. The S2P will produce a 16-bit parallel data output (S2P<15:0>) where the MSB <15:8> can be used by the PWM/DCMP0 and PWM/DCMP1 logic cells, while the LSB <7:0> can be used by the PWM/DCMP2, FSM0, and FSM1 logic cells.

17.3 Serial to Parallel Timing Diagram

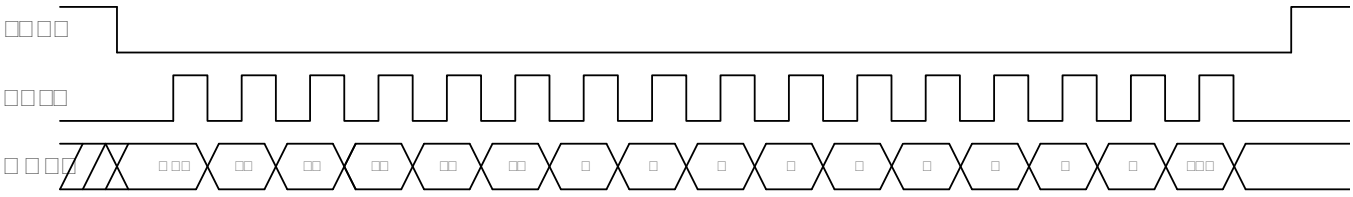

Figure 32. Serial to Parallel Timing Diagram

17.4 Parallel to Serial Operation

For parallel to serial operation (P2S), the 8-bit parallel data in (PAR IN<15:8>) comes from the CNT1 logic cell. PIN 6 is used to output the 8-bit serial data out (MISO) signal.

17.5 Parallel to Serial Timing Diagram

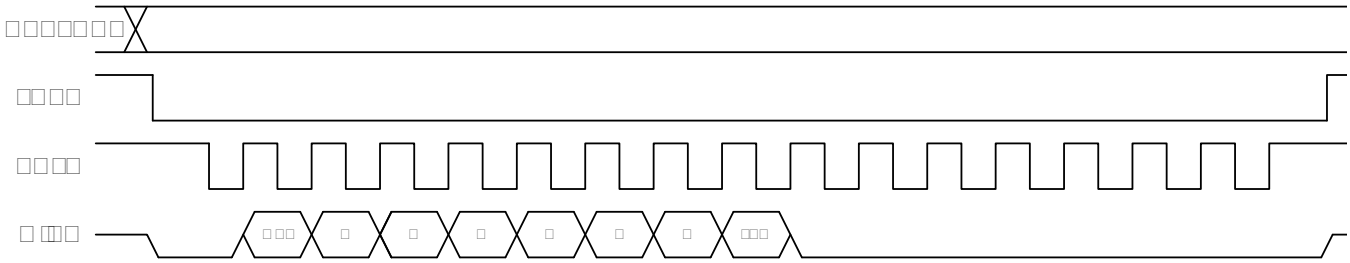

Figure 33. Parallel to Serial Timing Diagram

17.6 S2P Notes

Some functions of the S2P Converter share logic cells within the SLG46400, and as a result only one of these functions can be enabled at a time. The logic cells that are shared are:

- S2P serial to parallel mode or S2P parallel to serial out
- S2P parallel to serial mode or ADC serial output data on PIN 6
- S2P parallel to serial mode or DLY3 logic cell

17.7 S2P Register Settings

Table 26. S2P Register Settings

Signal Function	Register Bit Address	Register Definition
S2P Output Enable (PIN6)	<712:711>	00: Disable 01: Disable 10: Enable 11: Disable
S2P Mode Select	<804>	0: Serial Input (from PIN 6)/Parallel Output 1: Parallel Input (from CNT1)/Serial Output
S2P Clock Enable	<805>	0: Disable 1: Enable

18.0 Combinatorial Logic

Combinatorial logic is supported via eleven Lookup Tables (LUTs) within the SLG46400. There are four 2-bit LUTs, six 3-bit LUTs and one 4-bit LUT.

Inputs/Outputs for the eleven LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the eleven LUTs can be configured to user defined functions or the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

18.1 2-Bit LUT

The four 2-bit LUTs within the SLG46400 each take in two input signals from the connection matrix and produce a single output. LUT 2.0 inputs are shared with input and reset of the Pipe Delay logic cell.

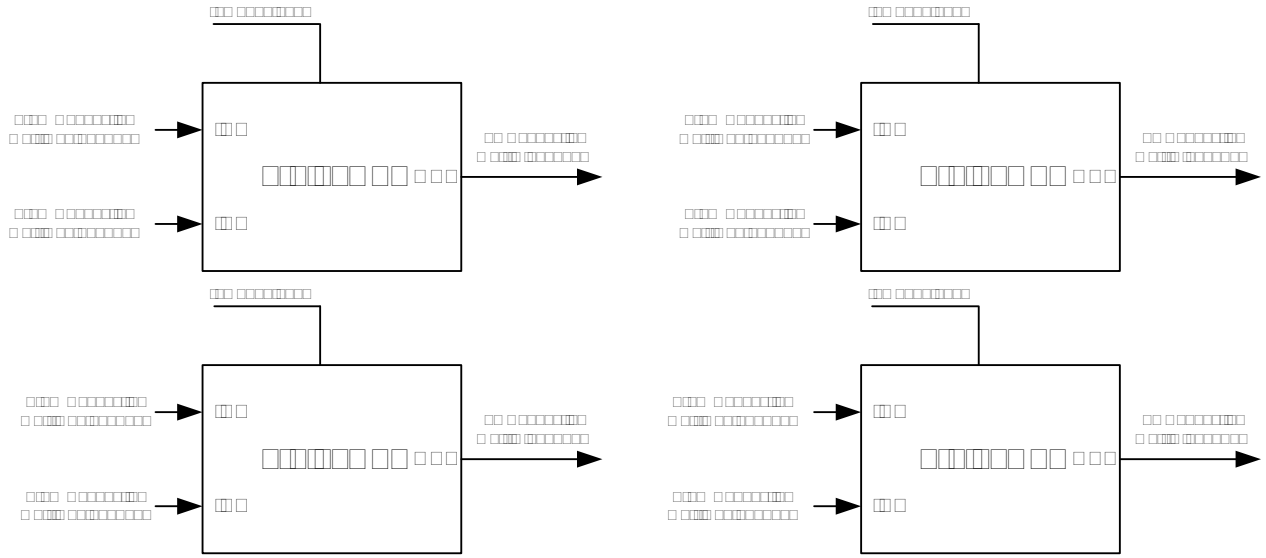

Figure 34. 2-bit LUTs

Table 27. 2-bit LUT0 Truth Table.

IN1	IN0	OUT
0	0	reg <450>
0	1	reg <451>
1	0	reg <452>
1	1	reg <453>

Table 28. 2-bit LUT1 Truth Table.

IN1	IN0	OUT
0	0	reg <454>
0	1	reg <455>
1	0	reg <456>
1	1	reg <457>

Table 29. 2-bit LUT2 Truth Table.

IN1	IN0	OUT
0	0	reg <458>
0	1	reg <459>
1	0	reg <460>
1	1	reg <461>

Table 30. 2-bit LUT3 Truth Table.

IN1	IN0	OUT
0	0	reg <462>
0	1	reg <463>
1	0	reg <464>
1	1	reg <465>

Each 2-bit LUT uses a 4-bit register signal to define their output functions;

2-Bit LUT0 is defined by reg<453:450>

2-Bit LUT1 is defined by reg<457:454>

2-Bit LUT2 is defined by reg<461:458>

2-Bit LUT3 is defined by reg<465:462>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 2-bit LUT logic cells.

Table 31. 2-bit LUT0/LUT1/LUT2/LUT3 Standard Digital Functions.

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

18.2 3-Bit LUT

The six 3-bit LUTs within the SLG46400 each take in three input signals from the connection matrix and produce a single output.

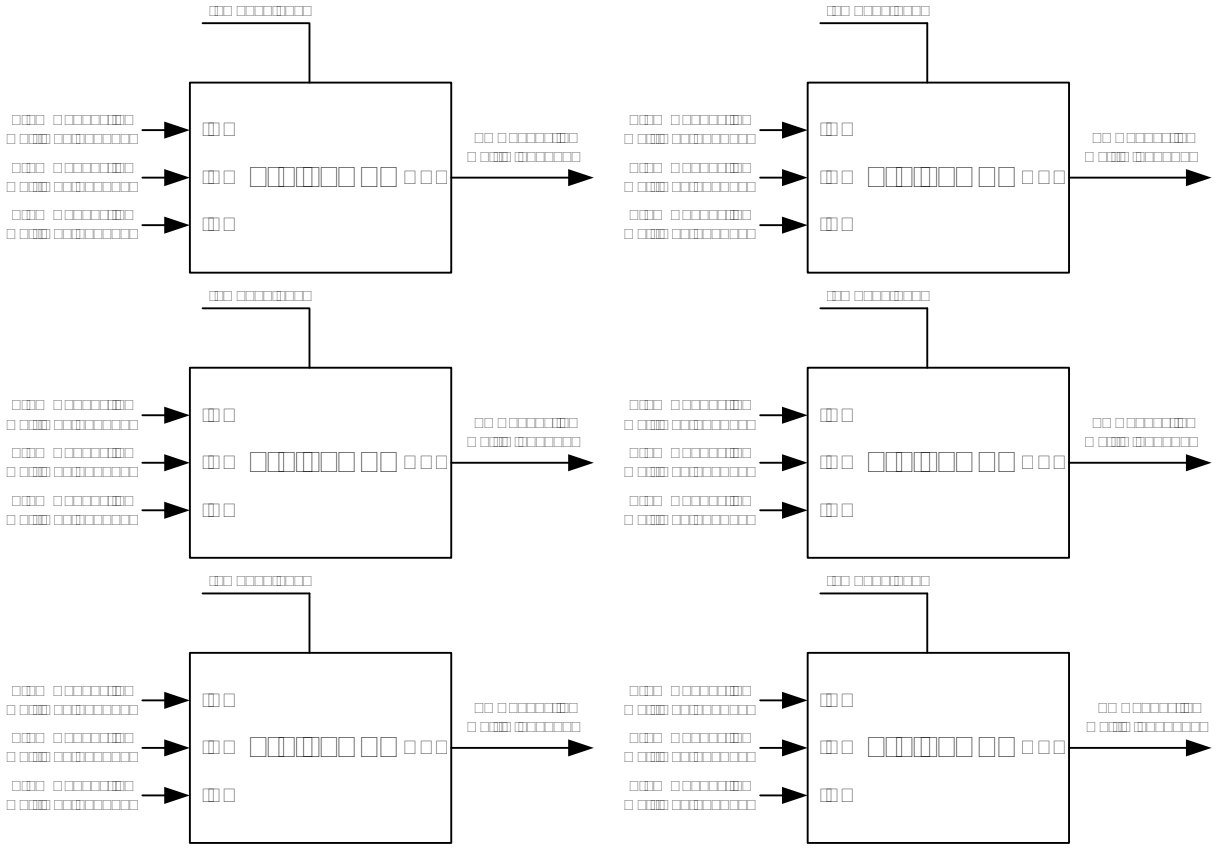

Figure 35. 3-bit LUTs

Table 32. 3-bit LUT0 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <466>
0	0	1	reg <467>
0	1	0	reg <468>
0	1	1	reg <469>
1	0	0	reg <470>
1	0	1	reg <471>
1	1	0	reg <472>
1	1	1	reg <473>

Table 33. 3-bit LUT1 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <474>
0	0	1	reg <475>
0	1	0	reg <476>
0	1	1	reg <477>
1	0	0	reg <478>
1	0	1	reg <479>
1	1	0	reg <480>
1	1	1	reg <481>

Table 34. 3-bit LUT2 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <482>
0	0	1	reg <483>
0	1	0	reg <484>
0	1	1	reg <485>
1	0	0	reg <486>
1	0	1	reg <487>
1	1	0	reg <488>
1	1	1	reg <489>

Table 35. 3-bit LUT3 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <490>
0	0	1	reg <491>
0	1	0	reg <492>
0	1	1	reg <493>
1	0	0	reg <494>
1	0	1	reg <495>
1	1	0	reg <496>
1	1	1	reg <497>

Table 36. 3-bit LUT4 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <498>
0	0	1	reg <499>
0	1	0	reg <500>
0	1	1	reg <501>
1	0	0	reg <502>
1	0	1	reg <503>
1	1	0	reg <504>
1	1	1	reg <505>

Table 37. 3-bit LUT5 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <506>
0	0	1	reg <507>
0	1	0	reg <508>
0	1	1	reg <509>
1	0	0	reg <510>
1	0	1	reg <511>
1	1	0	reg <512>
1	1	1	reg <513>

Each 3-bit LUT uses an 8-bit register signal to define their output functions;

3-Bit LUT0 is defined by reg<473:466>

3-Bit LUT1 is defined by reg<481:474>

3-Bit LUT2 is defined by reg<489:482>

3-Bit LUT3 is defined by reg<497:490>

3-Bit LUT4 is defined by reg<505:498>

3-Bit LUT5 is defined by reg<513:506>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six3-bit LUT logic cells.

Table 38. 3-bit LUT0/LUT1/LUT2/LUT3/LUT4/LUT5 Standard Digital Functions.

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

18.3 4-Bit LUT

The one 4-bit LUT within the SLG46400 takes in four input signals from the connection matrix and produces a single output.

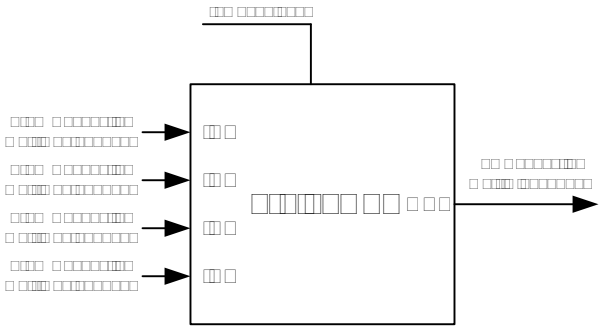

Figure 36. 4-bit LUT

Table 39. 4-bit LUT0 Truth Table.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <514>
0	0	0	1	reg <515>
0	0	1	0	reg <516>
0	0	1	1	reg <517>
0	1	0	0	reg <518>
0	1	0	1	reg <519>
0	1	1	0	reg <520>
0	1	1	1	reg <521>
1	0	0	0	reg <522>
1	0	0	1	reg <523>
1	0	1	0	reg <524>
1	0	1	1	reg <525>
1	1	0	0	reg <526>
1	1	0	1	reg <527>
1	1	1	0	reg <528>
1	1	1	1	reg <529>

The 4-bit LUT uses a 16-bit register signal to define the output function;

4-Bit LUT0 is defined by reg<529:514>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within the 4-bit LUT logic cell.

Table 40. 4-bit LUT0 Standard Digital Functions.

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

19.0 Digital Storage Elements (DFFs/LATCHes)

There are four DFF/LATCHes logic cells within the SLG46400 available for design. The source and destination of the inputs and outputs for the three DFF/LATCHes are configured from the connection matrix.

The operation of the D Flip-Flop and Latch will following the functional descriptions below:

DFF: CK is rising edge triggered, then Q = D; otherwise Q will not change

LATCH: if CK = 0, then Q = D

if CK = 1, then Q will not change

For DFF/LATCH 0, *matrix out1* will control the *Reset* and *Set* functions (Active Low) that are controlled from reg<531>. For DFF/LATCH 1, *matrix out18* will control the *Reset* and *Set* functions (Active Low) that are controlled from reg<533>.

19.1 DFF/LATCH Functional Diagram

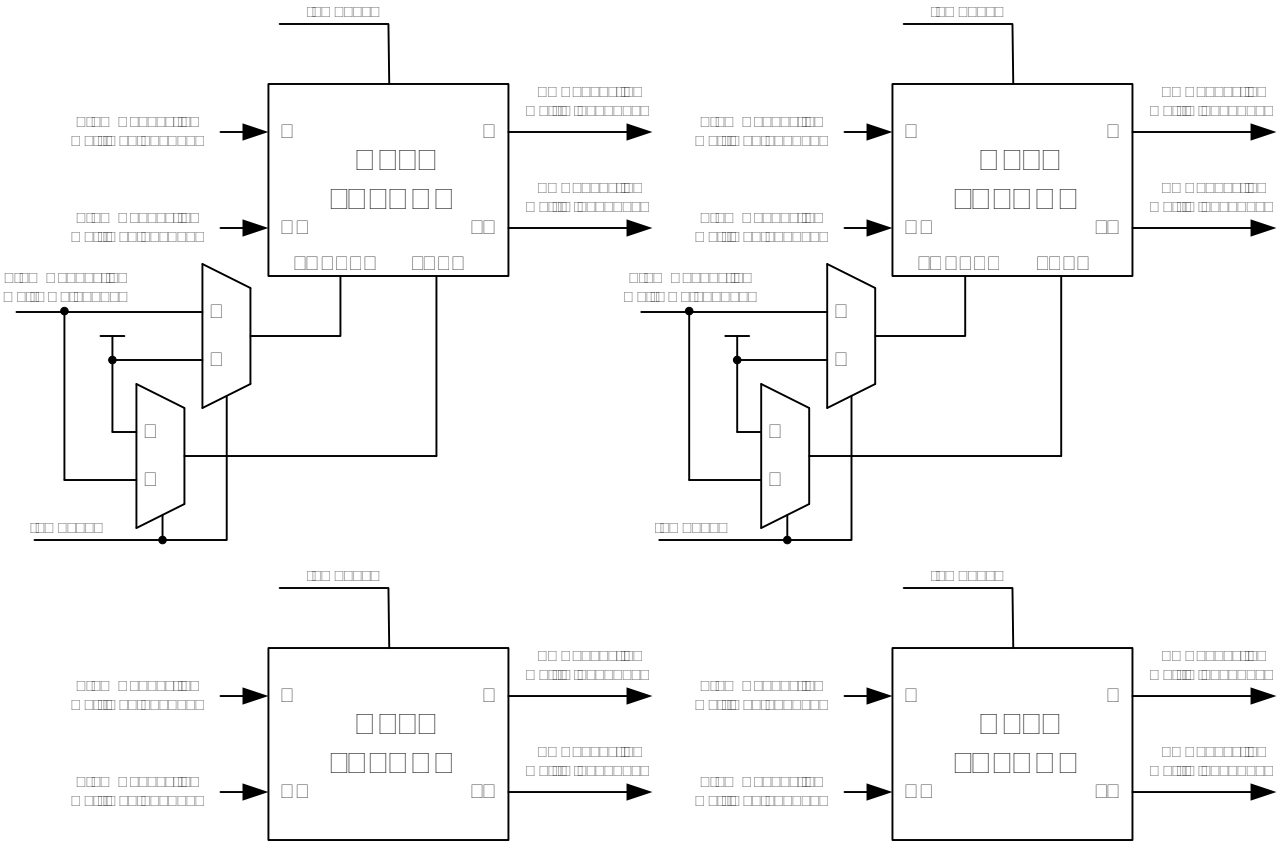

Figure 37. DFF/LATCH Functional Diagram

19.2 DFF/LATCH Selection

Each of the four DFF/LATCH logic cells have a selection bit that is used to define if the logic cell will be used as a D Flip-Flop or a Latch within the design. Those control bits are shown in the table below.

19.3 DFF/LATCH Register Settings

Table 41. DFF/LATCH Register Settings

Signal Function	Register Bit Address	Register Definition
DFF/LATCH0 Selection	<530>	0: DFF 1: Latch
DFF0 Reset or Set Select	<531>	0: Reset from Connection Matrix 1 1: Set from Connection Matrix 1
DFF/LATCH1 Selection	<532>	0: DFF 1: Latch
DFF1 Reset or Set Select	<533>	0: Reset from Connection Matrix 18 1: Set from Connection Matrix 18
DFF/LATCH2 Selection	<534>	0: DFF 1: Latch
DFF/LATCH3 Selection	<535>	0: DFF 1: Latch

20.0 Power On Reset (POR)

The Power On Reset (POR) macro cell will produce a “1” signal as an output when the power supply (V_{DD}) rises to around 1.4-1.6V.

The typical internal delay for POR from 1.4V to 1.6V is 6.8ms (min=4ms, max=10.47ms). The typical delay time for POR to NVM data out is 500∝s. For POR to work properly, the max power up ramp time for V_{DD}=1.8V is 34ms; for V_{DD}=5V, it is 100ms.

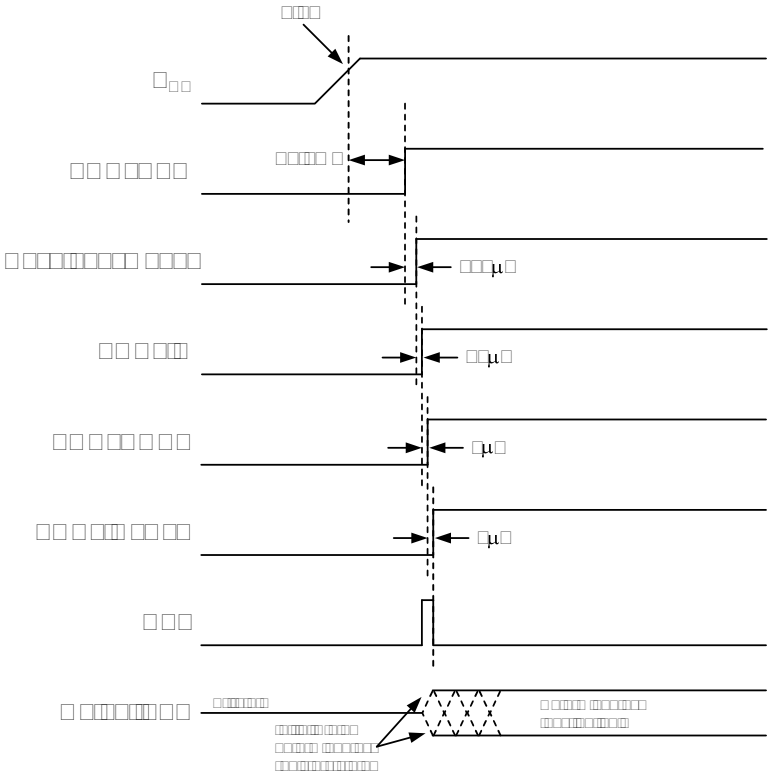

Figure 38. Power on Reset Timing Diagram

When NVM data is ready, the oscillator must be stable at the same time. If the oscillator power on is controlled by auto power on signals such as delay cells, ADC, or PWM, the oscillator will need a maximum of 5∝s to become stable.

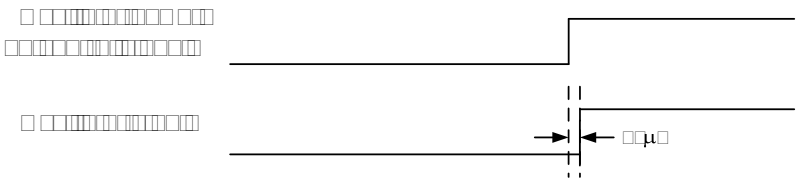

Figure 39. Stable Oscillator wait time

20.1 POR Register Settings Description

The POR logic cell is controlled by setting the registers <750:748>:

- When set to '010': Auto power detect function is on (both auto detection and the regulator for ADC and ACMP are on)
- When set to '101': V_{DD} bypass to ADC (when V_{DD} < 2.7V, no power consumption is used by either the ADC or ACMP logic cells)
- When set to '001': Regulator always on (when V_{DD} > 2.7V, there is no auto power detection, but regulator has power for the ADC & ACMP logic cells).

If the ADC or ACMP are not in use; reg <750:748> should be set to '000' and the ADC/ACMP logic cells should be set to power down mode.

If the ADC or ACMP are in use:

- if V_{DD} is fixed and 2.7V, reg <750:748> should be set to '101'.
- If V_{DD} varies from 1.8V to 5.0V, reg <750:748> should be set to '010'
- if V_{DD} varies from 2.6V to 5.0V, reg <750:748> should be set to '010' or '001'.

20.2 POR Register Settings

Table 42. POR Register Settings

Signal Function	Register Bit Address	Register Definition
POR Auto Power Detect	<748>	0: Enable 1: Disable
Power Divider Power On	<749>	0: Power Down 1: Power On
V_{DD} bypass to ADC (when V_{DD} 2.7V turn on)	<750>	0: Disable 1: Enable

21.0 Application Examples

21.1 System Reset

In the following application example, a system reset pulse can be generated from a command signal (from a microprocessor) or an external reset push button. The current reset state can be shown by adding a LED into the design. Implementing this function within the SLG46400 requires the use of an input buffer, an open drain LED output driver, a de-glitch filter, and a one-shot circuit. In this example the SLG46400 replaces up to four off-the-shelf components.

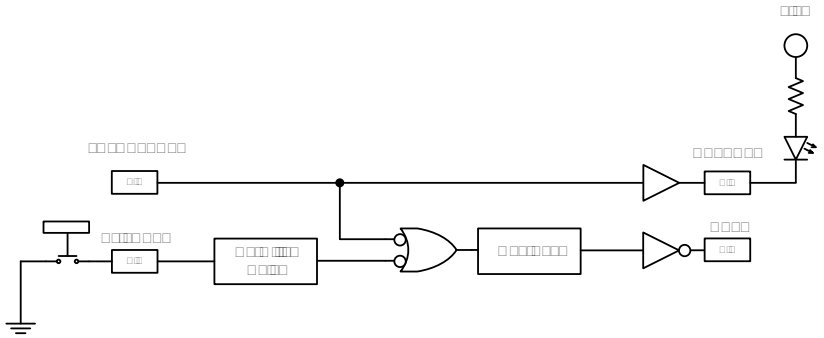

Figure 40. Example: System Reset

21.2 Combinatorial Logic

In this application example one SLG46400 is used to replace three discrete ‘1G’ SOT23-5 packaged logic components. The SLG46400’s 2.5mm X 2.5mm TDFN packaging of this function will result in significant space savings due to fewer components used in the final PCB design.

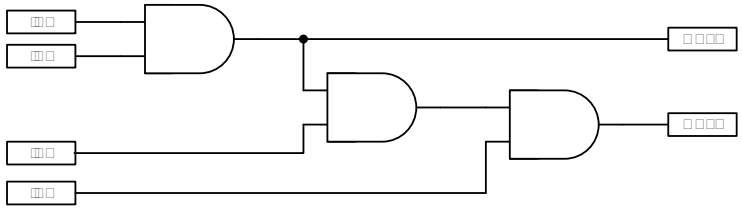

Figure 41. Example: Combinatorial Logic

21.3 Example: Bi-Directional Pin using an OE Signal

The example figure below shows how a Bi-Directional Pin can be set up in the GreenPAK 2 Designer tool by using an external signal for the Output Enable control signal.

The input to PIN 2 is controlled from an external signal, which is then used to control the Output Enable on PIN 3.

- When the signal on PIN 2 = “0”, then PIN 3 will act as a Digital Input. In this example, the signal from PIN 3 is going to the logic cell (LUT2.1 in this case).

- When the signal on PIN 2 = “1”, then PIN 4 will act as a Push Pull Output with 1x current drive. In this example, a signal from CNT1/DLY1 will be sent from the SLG46400 to the external board.

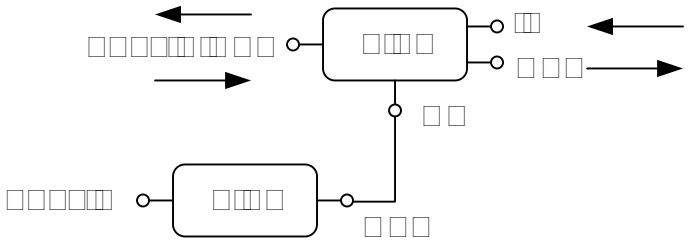

Figure 42. PIN 4 as a Bi-Directional Pin with PIN 2 as the OE Control

22.0 Development Tools

22.1 Software & Hardware

22.1.1 GreenPAK 2 Designer™

At the core of the GreenPAK 2 development software suite is GreenPAK 2 Designer, graphical schematic design tool used to create circuit designs within the GreenPAK 2 IC. GreenPAK 2 Designer requires no programming language or complier.

GreenPAK 2 Designer Software is available free of charge at http://www.silego.com/.

22.1.2 GreenPAK 2 Programmer

GreenPAK 2 Programmer is flexible enough and is used on the bench in development and also suitable for factory programming. GreenPAK 2 Programmer operates directly from GreenPAK 2 Designer.

22.1.3 Minimum System Requirements

- CPU: 800MHz
- RAM: 128MB
- Graphics RAM: 32MB
- Free Hard Disk Space: 50MB

Both of Silego's GreenPAK 2 Designer and Programmer software is supported in the following operating systems:

- 32-bit Microsoft Windows XP / Vista / 7
- 64-bit Microsoft Windows XP / Vista / 7
- Apple Mac OS X

Windows is a registered trademark of Microsoft Corporation in the United States and other countries.

Mac OS is a trademark of Apple Inc., registered in the U.S. and other countries.

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22.2 Development Kits

The GreenPAK 2 Development kit is sold directly at the Silego Online Store. Please visit at http://store.silego.com/

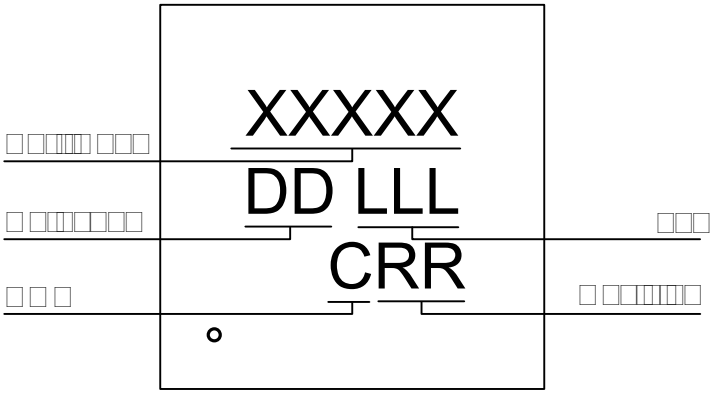
The GreenPAK 2 Development kit is for prototyping and development with GreenPAK 2 Designer. The kit contains a USB Programming stick, USB extension cable and 50 SLG46400 samples. Everything needed for a circuit designer to start prototyping designs with the GreenPAK 2 IC.

22.3 Project Examples

Additional GreenPAK 2 examples designs are available on the Silego website free of charge. These designs can be downloaded and reviewed in the GreenPAK 2 designer as a quick and efficient way to become familiar with the project development.

These examples can be found at http://support.silego.com/

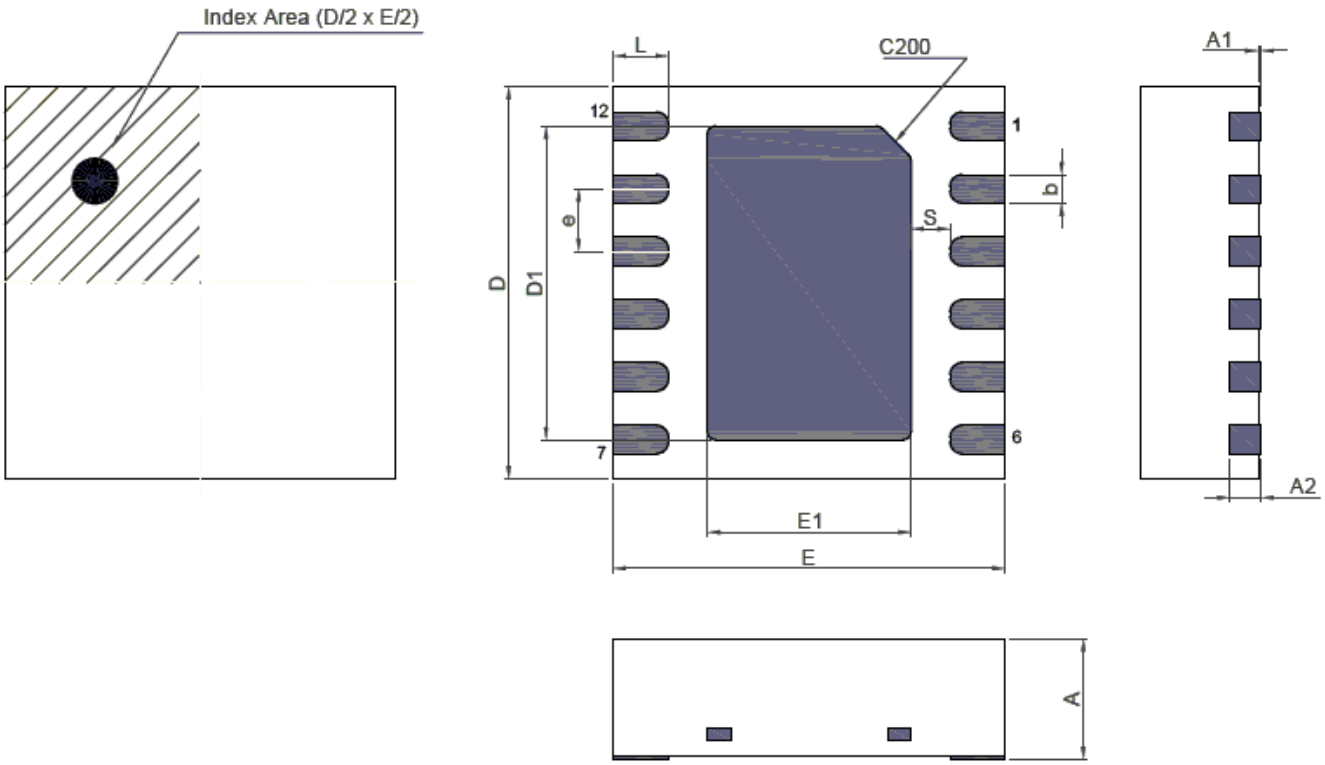
23.0 Package Top Marking System Definition



24.0 Package Drawing and Dimensions

24.1 12 Lead TDFN Package

JEDEC MO-252, Variation 2525E



Unit: mm

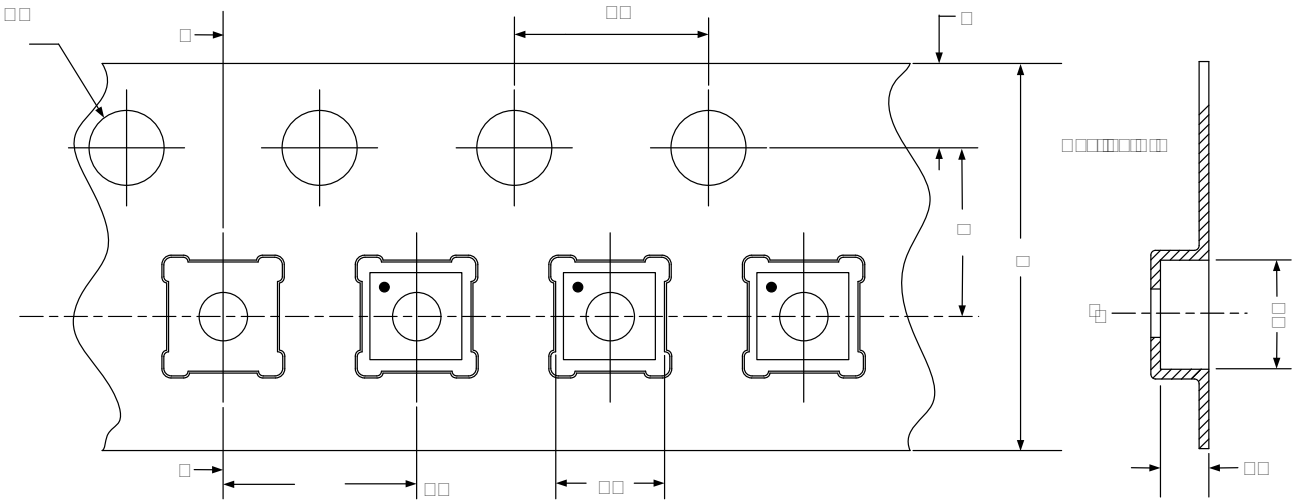
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	D1	1.95	2.00	2.05
A1	0.005	-	0.060	E1	1.25	1.30	1.35
A2	0.15	0.20	0.25	e	0.40 BSC		
b	0.13	0.18	0.23	L	0.30	0.35	0.40
D	2.45	2.50	2.55	S	0.18	-	-
E	2.45	2.50	2.55				

24.2 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 12L Green	12	2.5 x 2.5 x 0.75	3,000	3,000	178 / 60	42	168	42	168	8	4

24.3 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index hole to Pocket center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 12L Green	2.75	2.75	1	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

25.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 4.6875 mm^3 (nominal). More information can be found at www.jedec.org.

26.0 Appendix - SLG46400 Register Definition

Bit Address	Register Definition
reg<5:0>	Clock of Pipe Delay
reg<11:6>	Reset or set of DFF0
reg<17:12>	Reset or set of DFF1
reg<23:18>	Power down for ADC/PWM/RC OSC (reg<815:814> select power down block)
reg<29:24>	CNT2 external clock
reg<35:30>	CNT3 external clock
reg<41:36>	20ns/40ns/60ns/80ns Delay input
reg<47:42>	nCSB for SPI
reg<53:48>	PWM/DCMP0 ip3 and PWM/DCMP1 in1 input mux select bit0
reg<59:54>	PWM/DCMP0 ip3 and PWM/DCMP1 in1 input mux select bit1
reg<65:60>	PWR UP (power up) for ACMP0
reg<71:66>	PWR UP (power up) for ACMP0
reg<77:72>	KEEP for FSM0
reg<83:78>	LOAD for FSM0
reg<89:84>	UP/DOWN for FSM0
reg<95:90>	KEEP for FSM1
reg<101:96>	LOADfor FSM1
reg<107:102>	UP/DOWN for FSM1
reg<113:108>	Input for DLY0 or CNT0 external clock
reg<119:114>	Input for DLY1 or CNT1 external clock
reg<125:120>	Input for DLY2
reg<131:126>	Input for DLY3
reg<137:132>	PIN3 Digital Output Source
reg<143:138>	PIN4 Digital Output Source
reg<149:144>	PIN5 Digital Output Source
reg<155:150>	PIN6 Digital Output Source (reg<712:711>=00)
reg<161:156>	PIN8 Digital Output Source
reg<167:162>	PIN9 Digital Output Source
reg<173:168>	PIN10 Digital Output Source
reg<179:174>	PIN11 Digital Output Source
reg<185:180>	PIN12 Digital Output Source
reg<191:186>	Output Enable of PIN4
reg<197:192>	Output Enable of PIN5
reg<203:198>	Output Enable of PIN6
reg<209:204>	Output Enable of PIN10
reg<215:210>	Output Enable of PIN11
reg<221:216>	Output Enable of PIN12
reg<227:222>	Data Input of DFF0
reg<233:228>	Clock Input of DFF0
reg<239:234>	Data Input of DFF1
reg<245:240>	Clock Input of DFF1
reg<251:246>	Data Input of DFF2

Bit Address	Register Definition
reg<257:252>	Clock Input of DFF2
reg<263:258>	Data Input of DFF3
reg<269:264>	Clock Input of DFF3
reg<275:270>	IN0 of LUT2_0 /Input of Pipe Delay
reg<281:276>	IN1 of LUT2_0 /resetb of Pipe Delay
reg<287:282>	IN0 of LUT2_1
reg<293:288>	IN1 of LUT2_1
reg<299:294>	IN0 of LUT2_2
reg<305:300>	IN1 of LUT2_2
reg<311:306>	IN0 of LUT2_3
reg<317:312>	IN1 of LUT2_3
reg<323:318>	IN0 of LUT3_0
reg<329:324>	IN1 of LUT3_0
reg<335:330>	IN2 of LUT3_0
reg<341:336>	IN0 of LUT3_1
reg<347:342>	IN1 of LUT3_1
reg<353:348>	IN2 of LUT3_1
reg<359:354>	IN0 of LUT3_2
reg<365:360>	IN1 of LUT3_2
reg<371:366>	IN2 of LUT3_2
reg<377:372>	IN0 of LUT3_3
reg<383:378>	IN1 of LUT3_3
reg<389:384>	IN2 of LUT3_3
reg<395:390>	IN0 of LUT3_4
reg<401:396>	IN1 of LUT3_4
reg<407:402>	IN2 of LUT3_4
reg<413:408>	IN0 of LUT3_5
reg<419:414>	IN1 of LUT3_5
reg<425:420>	IN2 of LUT3_5
reg<431:426>	IN0 of LUT4_0
reg<437:432>	IN1 of LUT4_0
reg<443:438>	IN2 of LUT4_0
reg<449:444>	IN3 of LUT4_0
reg<453:450>	LUT2_0 data
reg<457:>454	LUT2_1 data
reg<461:458>	LUT2_2 data
reg<465:462>	LUT2_3 data
reg<473:466>	LUT3_0 data
reg<481:474>	LUT3_1 data
reg<489:482>	LUT3_2 data
reg<497:490>	LUT3_3 data
reg<505:498>	LUT3_4 data
reg<513:506>	LUT3_5 data

Bit Address	Register Definition
reg<529:514>	LUT4 data
reg<530>	DFF0 or Latch select 0: DFF function 1: Latch function
reg<531>	DFF0 nRST/nSET select 0: nRST from matrix out1 1: nSET from matrix out1
reg<532>	DFF1 or Latch select 0: DFF function 1: Latch function
reg<533>	DFF1 nRST/nSET select 0: nRST from matrix out18 1: nSET from matrix out18
reg<534>	DFF2 or Latch select 0: DFF function 1: Latch function
reg<535>	DFF3 or Latch select 0: DFF function 1: Latch function
reg<537:536>	Delay value select 00: 20ns 01: 40ns 10: 60ns 11: 80ns
reg<538>	Reserved
reg<540:539>	PIN8 initial state control 00: floating 01: ground 10: power 11: input
reg<543:541>	PIN8 mode control 000: digital in mode with Schmitt trigger 001: digital in mode without Schmitt trigger 010: low voltage digital in mode without Schmitt trigger 011: analog IO mode 100: push pull current x2 101: open drain mode 110: analog IO & open drain mode 111: push pull mode
reg<545:544>	PIN8 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<546>	PIN8 pull up/down resistor 0: pull down resistor 1: pull up resistor
reg<547>	PIN8 push pull output Enable 0: Disable 1: Enable
reg<549:548>	PIN9 Initial State Control 00: floating 01: ground 10: power 11: input

Bit Address	Register Definition
reg<552:550>	PIN9 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode without Schmitt trigger 010: Low voltage digital in mode without Schmitt trigger 011: Analog IO mode 100: Push pull current x2 101: Open drain mode 110: Analog IO & open drain mode 111: Push pull mode
reg<554:553>	PIN9 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<555>	PIN9 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<556>	PIN9 push pull output Enable 0: Disable 1: Enable
reg<558:557>	PIN10 initial state control 00: Floating 01: Ground 10: Power 11: Input
reg<561:559>	PIN10 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode without Schmitt trigger 010: Low voltage digital in mode without Schmitt trigger 011: Analog IO mode 100: Push pull current x2 101: Open drain mode 110: Analog IO & open drain mode 111: Push pull mode
reg<563:562>	PIN10 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<564>	PIN10 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<566:565>	PIN11 initial state control 00: Floating 01: Ground 10: Power 11: Input
reg<569:567>	PIN11 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode without Schmitt trigger 010: Low voltage digital in mode without Schmitt trigger 011: Analog IO mode 100: Push pull current x2 101: Open drain mode 110: Analog IO & open drain mode 111: Push pull mode

Bit Address	Register Definition
reg<571:570>	PIN11 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<572>	PIN11 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<574:573>	PIN11 initial state control 00: Floating 01: Ground 10: Power 11: Input
reg<577:575>	PIN12 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode without Schmitt trigger 010: Low voltage digital in mode without Schmitt trigger 011: Reserved 100: Push pull current x2 101: Open drain mode 110: Reserved 111: Push pull mode
reg<579:578>	PIN12 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<580>	PIN12 pull up/down resistor selection 0: Pull down resistor 1: Pull up resistor
reg<581>	PIN12 open drain double current 0: Normal current 1: Double current
reg<582>	Force RC Oscillator on 0: Auto Power On (Power on as needed) 1: Force Power On (Power always on)
reg<586:583>	RC Oscillator frequency control 0000: 28.66k 0001: 55.2k 0010: 78.84k 0011: 122.1k 0100: 141.58k 0101: 210.78k 0110: 225.06k 0111: 31‘.24k 1000: 487.02k 1010: 666.11k 1011: 765.72k 1100: 2.25M 1101: 2.93M 1110: 6.67M 1111: 8.28M
reg<587>	External Clock Source Select 0: Internal Oscillator Clock 1: External Clock

Bit Address	Register Definition
reg<588>	CNT0 Enable 0: Disable 1: Enable
reg<589>	CNT/DLY0 Output Source Select 0: Delay Output 1: Counter Output
reg<592:590>	CNT/DLY0 Clock Source Select 000: Internal RC OSC Clock 001: CLOCK/4 010: CLOCK/12 011: CNT1 Overflow Output 1X0: CLOCK/8 1X1: External Clock (reg<609> = 1)
reg<606:593>	CNT0 Control Data/DLY0 Time Control 1-16384: (delay time = (counter control data + 1) / freq)
reg<608:607>	DLY0 Mode Select 00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<609>	DLY0 Input Function Select 0: For Delay Input signal 1: For CNT0 External Clock
reg<610>	CNT1 Enable 0: Disable 1: Enable
reg<611>	CNT/DLY1 Output Source Select 0: Delay Output 1: Counter Output
reg<614:612>	CNT/DLY1 Clock Source Select 000: Internal RC OSC Clock 001: CLOCK/4 010: CLOCK/12 011: CNT1 Overflow Output 1X0: CLOCK/8 1X1: External Clock (reg<631> = 1)
reg<628:615>	CNT1 Control Data/DLY1 Time Control 1-16384: (delay time = (counter control data + 1) / freq)
reg<630:629>	DLY1 Mode Select 00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<631>	DLY1 Input Function Select 0: For Delay input signal 1: For CNT0 external clock
reg<632>	CNT/DLY2 Reset Source Select 0: From delay cell 1: From edge detect
reg<633>	CNT2 Enable 0: Disable 1: Enable
reg<634>	CNT/DLY2 Output Source Select 0: Delay Output 1: Counter Output

Bit Address	Register Definition
reg<637:635>	CNT/DLY2 Clock Source Select 000: Internal RC OSC Clock 001: CLOCK/4 010: CLOCK/12 011: CNT1 overflow output 1X0: CLOCK/8 1X1: External clock
reg<651:638>	CNT2 Control Data/DLY2 Time Control 1-16384: (delay time = (counter control data + 1) / freq)
reg<653:652>	DLY2 Mode Select 00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<654>	CNT/DLY3 Reset Source Select 0: From Delay Cell 1: From Edge Detect
reg<655>	CNT3 Enable 0: Disable 1: Enable
reg<656>	CNT/DLY3 Output Source Select 0: Delay Output 1: Counter Output
reg<659:657>	CNT/DLY3 Clock Source Select 000: Internal RC OSC Clock 001: CLOCK/4 010: CLOCK/12 011: CNT1 Overflow Output 1X0: CLOCK/8 1X1: External Clock
reg<667:660>	CNT3 Control Data/DLY3 Time Control 1-255: (delay time = (counter control data + 1) / freq)
reg<669:668>	DLY3 Mode Select 00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<670>	Ring Oscillator Enable 0: Disable 1: Enable (PWM/DCMP external clock source is selected from this ring osc)
reg<671>	Reserved
reg<673:672>	PIN2 Mode Control 00: Digital In Mode with Schmitt Trigger 01: Digital In Mode without Schmitt Trigger 10: Low Voltage Digital Input 11: Analog In
reg<675:674>	PIN2 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<676>	PIN2 pull up/down resistor 0: Pull down resistor 1: Pull up resistor

Bit Address	Register Definition
reg<678:677>	PIN3 initial state control 00: Floating 01: Ground 10: Power 11: Input
reg<681:679>	PIN3 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode without Schmitt trigger 010: Low voltage digital in mode without Schmitt trigger 011: Analog IO mode 100: Push pull current x2 101: Open drain mode 110: Analog IO & open drain mode 111: Push pull mode
reg<683:682>	PIN3 pull up/down resistor value selection. 00: Floating 01: 50K 10: 100K 11: 300K
reg<684>	PIN3 pull up/down resistor 0: Pull Down Resistor 1: Pull Up Resistor
reg<685>	PIN3 push pull output Enable 0: Push Pull Output Disable 1: Push Pull Output Enable
reg<687:686>	PIN4 initial state control 00: Floating 01: Ground 10: Power 11: Input
reg<690:688>	PIN4 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode without Schmitt trigger 010: Low voltage digital in mode without Schmitt trigger 011: Analog IO mode 100: Push pull current x2 101: Open drain mode 110: Analog IO & open drain mode 111: Push pull mode
reg<692:691>	PIN4 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<693>	PIN4 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<695:694>	PIN5 initial state control 00: Floating 01: Ground 10: Power 11: Input

Bit Address	Register Definition
reg<698:696>	PIN5 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode without Schmitt trigger 010: Low voltage digital in mode without Schmitt trigger 011: Reserved 100: Push pull current x2 101: Open drain mode 110: Reserved 111: Push pull mode
reg<700:699>	PIN5 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<701>	PIN5 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<703:702>	PIN6 initial state control 00: Floating 01: Ground 10: Power 11: Input
reg<706:704>	PIN6 mode control 000: Digital in mode with Schmitt trigger 001: Digital in mode without Schmitt trigger 010: ;ow voltage digital in mode without Schmitt trigger 011: Reserved 100: Push pull current x2 101: Open drain mode 110: Reserved 111: Push pull mode
reg<708:707>	PIN6 pull up/down resistor value selection 00: Floating 01: 50K 10: 100K 11: 300K
reg<709>	PIN6 pull up/down resistor 0: Pull down resistor 1: Pull up resistor
reg<710>	PIN6 open drain double 0: Normal current 1: Double current
reg<712:711>	PIN6 digital output source selection 0x: From Connection Matrix (out25) 10: From S2P (MISO) 11: From ADC Serial Output
reg<713>	ADC Input Gain Range 0: 0 ~ 1V 1: 0 ~ 0.78V
reg<714>	ADC Mux Channel Selection 0: MUX Disabled, ADC will sample PIN 8 for IN+ 1: MUX Enabled, ADC will sample either PIN 8 or 9 for IN+
reg<715>	ADC power down mode select 0: ADC slow power on mode 1: ADC fast power on mode

Bit Address	Register Definition
reg<718:716>	ADC PGA Gain Control 000: Single-ended (0.5X gain) or differential (N/A) 001: Single-ended (1X gain) or differential (1x gain) 010: Single-ended (2X gain) or differential (2X gain) 011: Single-ended (4X gain) or differential (4X gain) 100: Single-ended (8X gain) or differential (8X gain) 101: Single-ended (N/A) or differential (16X gain)
reg<720:719>	ADC V_{REF} source select (depends on reg <713>) 00: Bandgap voltage V_{BG} (1V or 0.778) 01: 1x or 2x external voltage source 10: V_{DD}* (0.25 or 0.5) 11: None
reg<721>	ACMP0 1uA input current option 0: Disable 1: Enable
reg<725:722>	ACMP0 IN- voltage select (when reg<736> = 0) 0000: 50mV 0001: 100mV 0010: 150mV 0011: 200mV 0100: 250mV 0101: 300mV 0110: 400mV 0111: 500mV 1000: 600mV 1001: 700mV 1010: 800mV 1011: 900mV 1100: 1100mV 1101: 1300mV 1110: 1500mV 1111: External (PIN 11)
reg<725:722>	ACMP0 IN- voltage select (when reg<736> = 1) 0000: 30mV 0001: 70mV 0010: 100mV 0011: 130mV 0100: 170mV 0101: 200mV 0110: 270mV 0111: 330mV 1000: 400mV 1001: 470mV 1010: 530mV 1011: 600mV 1100: 730mV 1101: 870mV 1110: 1000mV 1111: External (PIN 11)
reg<726>	ACMP1 1∞A input current option 0: Disable 1: Enable
reg<730:727>	ACMP1 IN- voltage select (when reg<736> = 0) 0000: 50mV 0001: 100mV 0010: 150mV 0011: 200mV 0100: 250mV 0101: 300mV 0110: 400mV 0111: 500mV 1000: 600mV 1001: 700mV 1010: 800mV 1011: 900mV 1100: 1100mV 1101: 1300mV 1110: 1500mV 1111: External (PIN 11)
reg<730:727>	ACMP1 IN- voltage select (when reg<736> = 1) 0000: 30mV 0001: 70mV 0010: 100mV 0011: 130mV 0100: 170mV 0101: 200mV 0110: 270mV 0111: 330mV 1000: 400mV 1001: 470mV 1010: 530mV 1011: 600mV 1100: 730mV 1101: 870mV 1110: 1000mV 1111: External (PIN 11)
reg<732:731>	ACMP0 hysteresis Enable 00: Disabled (0mV) 01: Enabled (12mV) 10: Enabled (50mV) 11: Enabled (150mV)
reg<734:733>	ACMP1 hysteresis Enable 00: Disabled (0mV) 01: Enabled (12mV) 10: Enabled (50mV) 11: Enabled (150mV)
reg<736>	ACMP V_{REF} band select 0: 50mV to 1.5V range 1: 30mV to 1V range
reg<737>	ADC clock selection 0: Internal RC Oscillator 1: External clock from PIN 5

Bit Address	Register Definition
reg<738>	ADC pseudo diff input Enable under ADC diff mode 0: Disabled 1: Enabled
reg<739>, reg<735>	ACMP0 IN+ source selection 00: ACMP0 IN+ input from PIN3 01: ACMP0 IN+ input from PIN4 (PIN3 analog_io_en should be disabled) 10: ACMP0 IN+ input from PGA OUT 11: ACMP0 IN+ input from PGA IN
reg<740>	V_{REF} Output Active Buffer Control 0: Enabled 1: Disabled
reg<741>	V_{REF} Output Enable 0: ACMP0 = V_{REF} Input 1: Enabled
reg<742>	ADC Input Mode Select 0: Single-end operation using PIN 8 1: Differential mode using PINS 8 & 9
reg<743>	V_{REF} Output Source Select 0: ACMP0 reference voltage 1: V_{DD}/3
reg<744>	Force bandgap on 0: Disabled 1: Enable
reg<745>	ACMP1 negative input source select 0: from V_{REF} 1: from DAC output
reg<746>	DAC input data select 0: ADC normal work 1: DAC data comes from FSM
reg<747>	ACMP1 positive input divided by 2 resistor(100K) 0: Disabled (IP input from PIN 4) 1: Enabled (IP input from ADC - PGA Out)
reg<748>	POR Auto Power Detection Control 0: Enable 1: Disable
reg<749>	POR Power Divider Power On (only required when using power divider output for external source) 0: Disable 1: Enable
reg<750>	POR V_{DD} bypass to ADC (only required when V_{DD} <=2.7V) 0: Disable 1: Enable
reg<752:751>	FSM0 Input Data Select x0: From NVM (connection matrix) 01: From S2P 11: From ADC
reg<754:753>	FSM1 Input Data Select x0: From NVM (connection matrix) 01: From S2P 11: From ADC
reg<757:755>	PWM deadband Select 000:8ns 001:16ns 010:24ns 011:32ns 100:40ns 101:48ns 110:56ns 111:64ns

Bit Address	Register Definition
reg<758>	PWM0 Mode Select 0: Down to 0% 1: Up to 100%
reg<759>	PWM/DCMP Clock Invert 0: Disable 1: Enable
reg<760>	PWM0/DCMP0 Power Down Control 0: Power down 1: Power on
reg<761>	PWM1/DCMP1 Power Down Control 0: Power down 1: Power on
reg<762>	PWM2/DCMP2 Power Down Control 0: Power down 1: Power on
reg<764:763>	PWM0/DCMP0 Positive Input Source Select 00: From ADC 01: From S2P 10: From FSM0 11: 8-bit user defined (selected through matrix)
reg<766:765>	PWM1/DCMP1 Positive Input Source Select 00: From ADC 01: From S2P 10: From FSM0 11: 8-bit user defined (selected through matrix)
reg<768:767>	PWM2/DCMP2 Positive Input Source Select 00: From ADC 01: From S2P 10: From FSM0 11: 8-bit user defined (selected through matrix)
reg<769>	PWM0/DCMP0 Negative Input Source Select 0: From CNT1 ramp (for PWM) 1: 8-bit user defined (selected through matrix)
reg<770>	PWM1/DCMP1 Negative Input Source Select 0: From CNT1 ramp (for PWM) 1: 8-bit user defined (selected through matrix)
reg<771>	PWM2/DCMP2 Negative Input Source Select 0: From CNT1 ramp (for PWM) 1: 8-bit user defined (selected through matrix)
reg<779:772>	PWM/DCMP NVM data pwm_reg0
reg<787:780>	PWM/DCMP NVM data pwm_reg1
reg<795:788>	PWM/DCMP NVM data pwm_reg2
reg<803:796>	PWM/DCMP NVM data pwm_reg3
reg<804>	S2P or P2S Mode Select 0: Serial in parallel output to chip internal 1: Parallel in from chip serial out
reg<805>	SPI clock /Osc external clock Enable 0: Disable 1: Enable
reg<806>	Bypass the PIN2 0: PIN2 edge active 1: PIN2 high active

Bit Address	Register Definition
reg<807>	PIN2 edge detect mode 0: Rising edge 1: Falling edge
reg<808>	PIN2 reset Enable 0: Disable 1: Enable
reg<810:809>	Pipe number select from connection matrix out <48> 00: 3 pipes 01: 5 pipes 10: 7 pipes 11: 11 pipes
reg<811>	ACMP0 Low Bandwidth Enable 0: Disable 1: Enable
reg<812>	ACMP1 Low Bandwidth Enable 0: Disable 1: Enable
reg<813>	ADC power down control register when reg<815:814>="01". ADC power power is controlled by reg<813>, otherwise, ADC power down is controlled by connection matrix out<3>. When reg <814> = "1": 0: ADC power on 1: ADC power down
<815:814>	ADC/PWM/OSC power down source selection 00: ADC power down from matrix out <3>, PWM power down from register 01: PWM power down from matrix out <3>, ADC power down from reg <813> 10: ADC & PWM power down from matrix out <3> 11: OSC power down from matrix out <3>, PWM & ADC power down from register
reg<816>	Oscillator Dividers control 0:Oscillator Dividers Enabled 1: Oscillator Dividers Diasbled
reg<817>	DFF0/LATCH0 output polarity control 0: Do not invert output polarity 1: Invert output polarity
reg<818>	PWM1 Mode Select 0: Down to 0% 1: Up to 100%
reg<819>	PWM2 Mode Select 0: Down to 0% 1: Up to 100%
reg<821:820>	Pipe number select from connection matrix out <49> 00: 2 pipes 01: 4 pipes 10: 8 pipes 11: 12 pipes
reg<829:822>	8-bit pattern id
reg<830>	NVM data read Disable 0: Disable 1: Enable
reg<831>	NVM power down 0: None 1: Power Down

27.0 Revision History

Date	Version	Change
6/3/2015	1.09	Fixed package name Tape and Reel Spec
10/8/2014	1.08	Fixed typo in Tape and Reel Spec
8/6/2014	1.07	Fixed ESD information
11/21/2013	1.06	Added ESD Ratings and MSL to Absolute Maximum Conditions
9/24/2013	1.05	Updated conditions for V_{AIR} in Electriical Characteristics for clarity. Updated Section 13 to clarify Counter functionality.
7/16/2013	1.04	Fixed Typo in Section 15.1 Diagram
06/04/2013	1.03	Updated 3bit LUT and 4bit LUT Standard Digital Functions tables
02/05/2013	1.02	SLG46400 Rev. B: Updated ADC Functional Diagram (Figure 3) Updated ACMP0 IN+ source selection information and ACMP0 Functional Diagram (Section 10.1 and Figure 8) Updated ACMP0 Register Settings (reg<735> and reg<739>) Corrected FSM0 and FSM1 UP/DOWN operation descriptions (Sections 13.7 and 13.9, Figures 19 and 21) Added Frequency Dividers Control function description (Section 16.3) Updated RC OSC Register Settings Updated RC OSC Typical Frequency Selection, Table 24 Updated Register Definition (RC OSC Frequency Control, reg<586:583>) Updated Register Definition (ACMP0 IN+ Source Selection, reg<739, 735>) Updated Register Definition (RC OSC Dividers Control, reg<816>)
11/19/2012	1.01	Updated Electrical Characteristics Table (VIL values) Fixed typo in Section 10.9 (less than or equal sign)
9/19/2012	1.0	Fixed typo in Section 10.9 Description
7/27/2012	0.92	Fixed typo in Electrical Characteristics table Updated Section 12.2 for clarification
7/16/2012	0.91	Editorial changes for clarification and typo fixes throughout Renamed Signal names to match GreenPAK Designer Software Moved Bi-Directional Pin example to Section 21.0
6/27/2012	0.9	Updated Electrical Characteristics Table Corrected Section 9.4 regarding 2-Channel Selection (Pin 12 instead of Pin 2) Updated Section10.0 to clarify ACMP power down operation and fixed ACMP hysteresis values in Sections 6.4, 10.9, and 10.10.1 Updated Section 12.10 regarding poiwer down control Renamed Section 16.0 RC Oscillator to Clock Management and clarified operation and updated block diagram. Updated Section 13.12 to include short pulse delay time diagrams. Removed Application Example regarding time delay Updated register map
6/8/2012	0.85	Updated Section 13.4 Added note regarding minimum value of the register setting for the CNT/DLY cells
3/20/2012	0.84	Editorial changes for clarification and typo fixes throughout
1/27/2012	0.83	Editorial changes for clarification and typo fixes throughout Updated Section 9.9 ADC Outputs Updated Section 13.1 Counter Functionality Updated Section 13.7 and 13.9 regarding FSM Operation Updated Recommended Soldering Profile information
12/5/2011	0.82	Added Recommended Soldering Profile information
11/3/2011	0.81	Added Bi-Directional Pin Information
9/19/2011	0.8	Production release
9/18/2011	0.53	General updates

Date	Version	Change
10/20/2010	0.1	Preliminary datasheet

28.0 Silego Website & Support

28.1 Silego Technology Website

Silego Technology provides online support via our website at http://www.silego.com/.This web site is used as a means to make files and information easily available to customers.

For more information regarding Silego GreenPAK and other Silego Green products, please visit:

http://greenpak.silego.com/
http://greenfet.silego.com/
http://greenpak2.silego.com/
http://greenfet2.silego.com/
http://greenclk.silego.com/

Products are also available for purchase directly from Silego at the Silego Online Store at http://store.silego.com/.

28.2 Silego Technical Support

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send email requests to GreenPAK@silego.com

Users of Silego products can receive assistance through several channels:

28.2.1 Contact Your Local Sales Representative

Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to info@silego.com

28.2.2 Contact Silego Directly

Silego can be contacted directly via e-mail at info@silego.com or user submission form, located at the following weblink:

http://support.silego.com/

28.3 Other Information

The latest Silego Technology press releases, listing of seminars and events, listings of world wide Silego Technology offices and representatives are all available at http://www.silego.com/