AN-1006
Proper PCB Layout with GreenCLK

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Introduction

GreenCLK printed circuit board (PCB) layouts can be sensitive to nearby RF. It is important to follow good controlled impedance PCB design techniques.

GreenCLK Background

Good radio frequency (RF) PCB practices should be employed when adding a GreenCLK to a PCB layout. GreenCLK by its very nature generates several different frequencies from its various outputs. Improper PCB layout techniques and methods can degrade the GreenCLK performance.

PCB Grounding

It should be noted that the thermal pad on the bottom of the GreenCLK package is not specifically used for dedicated grounding purposes. Each pin that is designated as being connected to ground should be specifically and solidly connected to the PCB ground. If possible, each ground pin should connect through its own via to a ground plane (preferred method). If this is not possible, traces connecting to common vias that reach the ground plane should be as short as possible (acceptable method). Vias should be of sufficient diameter so as to reduce via inductance as much as possible. The ground that GreenCLK connects to should be as large and continuous as possible.

VDD/V3.3A/VRTC Connections

GreenCLK power supply connections should be routed away from RF traces such as the outputs that carry signals in the MHz frequency range. PCB crosstalk from RF sources can cause coupling to power supply traces that can degrade performance.

External Passive Components

When passive components are required for external connections to a GreenCLK IC, they should be of a "0402" or similar type. This will help keep self-resonant frequencies higher and reduce their impact on performance.

In some cases an external series resistor or loading capacitor may be required to reduce EMI.

VDD/V3.3A/VRTC Bypass Capacitors

Power supply bypass capacitors should be used as per the recommendations in the specific GreenCLK datasheet being used. In general, however, bypass capacitors should be chosen for their low impedance as well as their self-resonant frequency. Multi-layered ceramic types are better for higher self-resonance. Bypass capacitors should be placed between the GreenCLK IC and their corresponding ground plane vias. This will result better overall bypassing of noise.

If space allows, several bypass capacitors of different values and self-resonant frequencies should be used in parallel to achieve better noise reduction.

RCAP Choice

Proper selection of the RCAP value and type is also critical to correct GreenCLK operation. The value recommended in the datasheet should be strictly adhered to. This value is chosen based on the application, power supply scheme, and required operation modes for the GreenCLK.

Crystal, Oscillator, or TCXO Reference

GreenCLK has been developed for use with a variety of crystal based frequency sources. In each case, the frequency source should be placed as close as possible to the GreenCLK input pin(s). Proper PCB trace design should minimize stray capacitance that can affect the circuit load capacitance of a crystal, for example. When a crystal is used as the frequency source, route traces to the crystal such that they minimize adding capacitance to the crystal Co. This can be done by avoiding routing the X1 and X2 traces in parallel.

VIO/VIOE/VDDIO Connections

When output drivers require a VIO, VIOE, or VDDIO power supply connection, proper bypassing of noise should be considered. Generally, 0.1 µF or larger should be used. The bypass capacitor should be placed as close as possible to the GreenCLK pin.

Reference Voltage Outputs

Some GreenCLK configurations have an internally controlled power supply that is required for proper biasing of external components. Specified bypass capacitors should be strictly adhered to.

Placement and Shielding from High Speed Lines

In noise sensitive applications, extra care must be taken with the layout of nearby high-speed signal lines. In such cases, the following guidelines* are advised:

1. Keep any HSIO line or via at least 70 mils away from X1, X2 line and associated components (crystal and load capacitors).

2. Add a GND shield between any high-speed I/O (HSIO) and any components or routing connected to X1 and X2 is advised. See below figure 1. for an example layout. The surrounding GND shield trace shown is 10 mils wide.

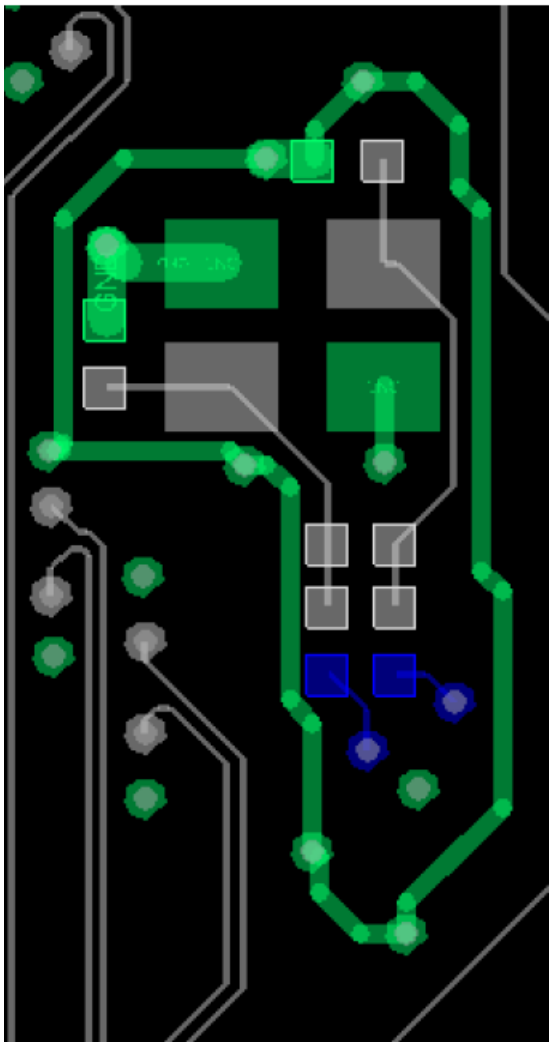

Figure 1. Crystal Components with GND Shield Trace

Figure 1 shows the layout top layer, but the same principal applies any other layer. Routing X1, X2 on inner layers with solid GND fills on outer layers would provide the greatest protection from external noise coupling. Of course, be aware that the GND planes over the traces are a source of parasitic capacitance, so size the crystal load caps accordingly.

**These guidelines are taken from an Intel advisory regarding crystal layout for their Skylake platform, known to have noise sensitivity issues.*

Sharing Of Power Supplies

Another noise source is coupling via power supplies. To prevent problems in sensitive applications, each of the supplies connected GCLK (eg. VDD, V3.3A, VDDIO, VIO, VIOE) should be isolated as much as possible from each other. If a supply must be shared, each pin should have its own bypass cap. Figure 2 shows an example that caused boot problems in a computer host controller application, along with a fix which resulted in acceptable performance.

In the problematic connection, VDD and VIO_25M were tied together, with only a 0.1uF bypass cap near the VIO_25M pin. To fix the boot problem, the VDD and VIO_25M lines were separated and bypass caps were put close to their respective pins. A series resistor (between 4.7 and 10 ohms recommended) also helps to provide isolation. A ferrite bead may be used in place of the resistor if greater isolation is needed.

This diagram shows the basic power scheme that was causing the boot problem. Noise was feeding into VDD and the Skylake platform is sensitive to excess noise

The circuit diagram shows how to resolve the boot problem by isolating VDD with a resistor and an additional 0.1uF cap

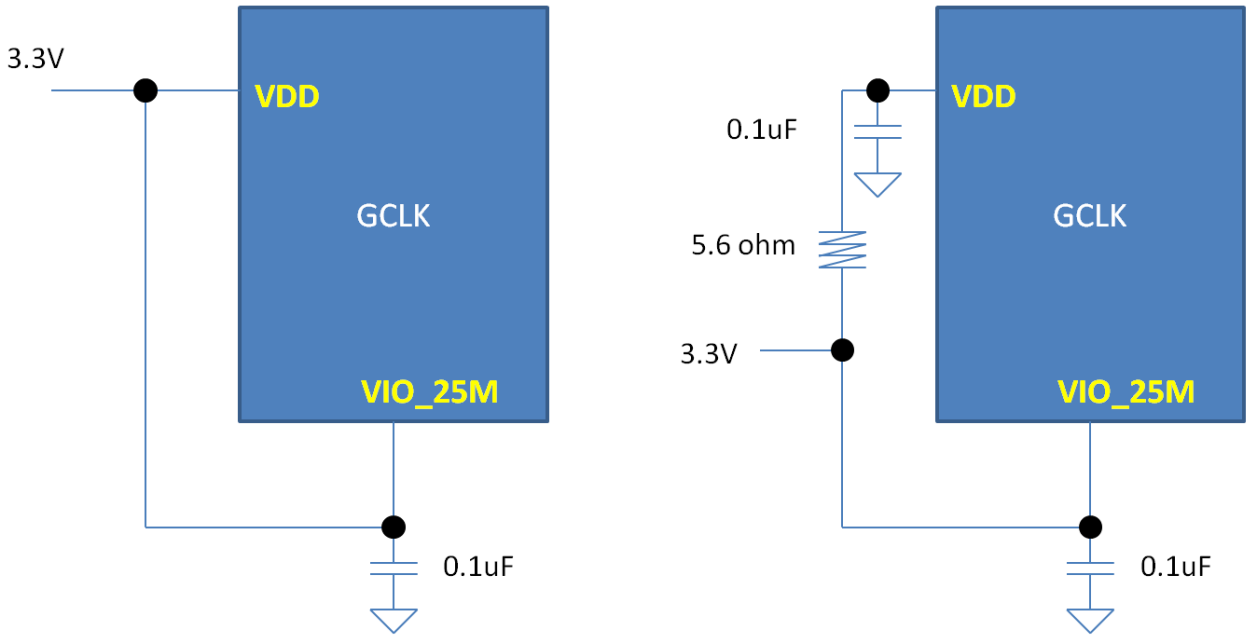

Figure 2. Problematic vs. Acceptable Power Schemes

Related Files

GreenCLK PCB layout libraries in OrCad, Eagle, and Altium, available from the **Silego website**.

References

Marks, L. & Caterina, J., Printed Circuit Assembly Design, 2000, McGraw-Hill.

About the Author

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Background: Chuck earned his BSEE from Northern Illinois University with specialization in RF. He has worked for over 20 years in the frequency control field designing many types of quartz crystal based oscillators (XO's, VCXO's, TCXO's, and OCXO's) using discrete analog and RF circuitry. Chuck has also managed engineering teams around the globe. He recently earned his MBA.

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Document History

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Revision	Orig. of Change	Submission Date	Description of Change
A	Chuck Husted	02/05/2013	New application note
B	David Chow	09/28/2015	Additional text and figures

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