GreenPAK Macro Circuit Design: Configurable Generators

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Introduction

GreenPAK2 chip has internal components that make creating different systems and circuits with configurable generators included possible. These circuits can be used for triggering other circuits or creating LED periodical blinking.

Generator Circuit Design

The simplest square waveforms generator consists of the inverter with a feedback from its output to input. The output signal will have a period equal to double of inverter's propagation time. If the propagation time can be controlled by the output signal period then the frequency can be controlled as well. Fortunately GreenPAK2 chips have configurable delay cells. The delay time of each cell depends on the Counter Data setting and the clocking frequency.

If the generated signal is a square waveform with 50% duty cycle but the generator itself has another duty cycle one can use a frequency divider by 2, constructed using a DFF with a feedback from its inverting output to data input, clocked from the generator. DFFs are available inside GreenPAK2 chip as well.

The design shown below is created in GreenPAK2 Designer software. Its task is to generate 500ms period 50% duty cycle square waveforms when ENABLE input is set HIGH. The timing diagram shown on Figure 1 explains the device operation.

The inverter can be created using a LUT. In this design a 3-bit LUT0 is used for this purpose because it combines POR initialization and button enable inverter logic. The 3-bit input LUT truth table is shown on Figure 2.

DLY0, configured as rising edge delay for 250ms, is used as a configurable element that sets the output period. The delay time is defined by the equation:

$$T_{DLY} = \frac{Counter\ Data + 1}{F_{CLK}}$$

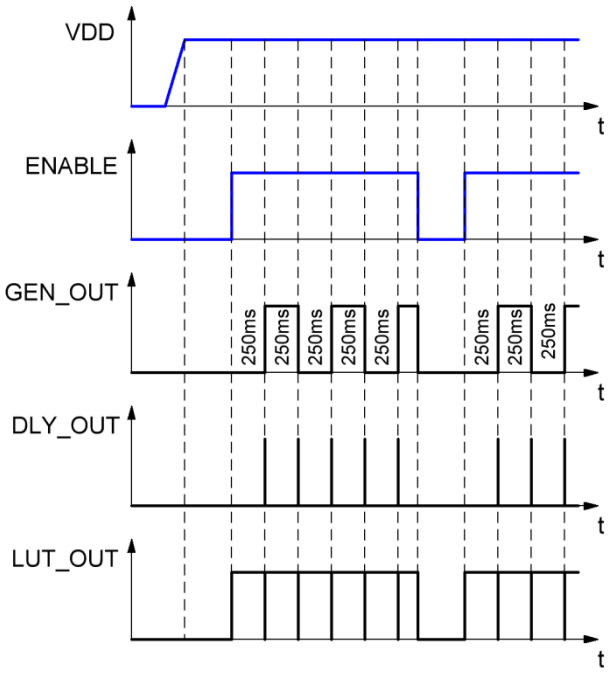


Figure 1. Generator Timing Diagrams

As a clocking source the RC OSC is chosen by default. Also there are options of the RC OSC divided by 4, 8, 12, from another CNT/DLY block or from matrix (please refer to the datasheet for more information). In its turn RC OSC has a configurable frequency that can be chosen from the set of 16 frequency options in the range from 29.11kHz to 8428.44kHz.

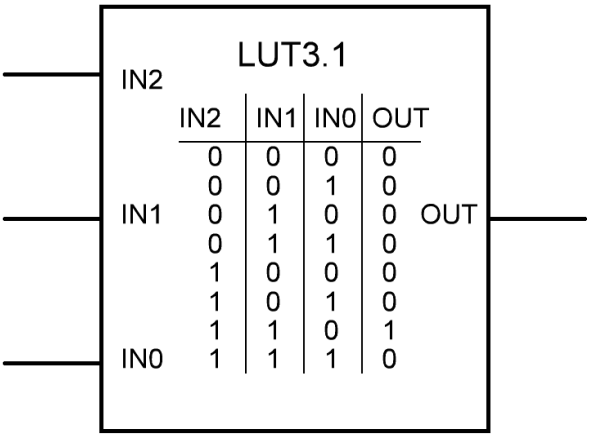
The 3-bit LUT has IN2 connected to POR output, IN1 connected to ENABLE (PIN2), IN0 is connected to DLY0 output which has an input connected to 3-bit LUT0 output.

Such a circuit will produce short pulses (equal to propagation time through LUT and DLY cell without delay) every 250ms. To make this signal a 50% duty cycle square waveform the DFF0 with a feedback from its nQ output to D input is used. The DFF clocked by the signal from the DLY0 output will start the output generation with 250ms LOW signal (see

Figure 1). The DFF0 is configured to have an active LOW nRESET input, which allows resetting the DFF0 output when ENABLE signal is LOW. For this purpose as well as for POR initialization a 2-bit LUT1 is used. This LUT is configured as AND gate.

So, considering all said above, the output signal will be a 50% duty cycle square waveform with the frequency defined by the next equation:

$$T_{OUT} = \frac{2(Counter\ Data + 1)}{F_{CLK}}$$



IN2	IN1	IN0	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Figure 2. 3-bit LUT1 Truth Table

The input of this design is configured as digital input without Schmitt trigger, out – push pull.

A functionality waveform of circuit created in GreenPAK2 Designer is shown on Figure 3 where Channel1 (yellow/top line) – PIN3 (ENABLE), Channel2 (light blue/bottom line) – PIN12 (GEN_OUT), Channel3 (magenta/3rd line) – PIN11 (DLY_OUT), Channel4 (blue/bottom line) – PIN10 (LUT_OUT) As can be seen from Figure 3 the real waveform coincides with the theoretical one shown on Figure 1.

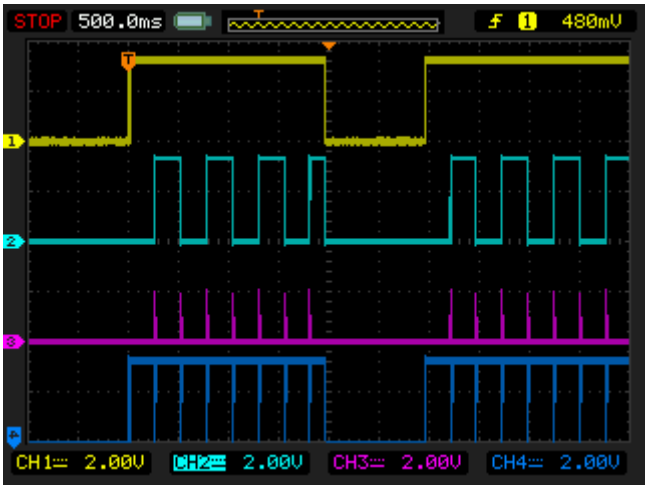


Figure 3. Configurable Generator Functionality Waveforms

Conclusion

Using the GreenPAK2 chips to create generators is very simple. The design itself is straightforward and flexible, that allows creating generators with user specific frequencies, enabled by the LOW or HIGH signals and outputs set LOW or HIGH when inactive. Also the output initial state after being enabled can be defined.

Note: For proper output PINs operation, if they are configured as push pull, their OE node should be connected to HIGH signal source, for example to VDD.

Related Files

Programming code for **GreenPAK Designer.**

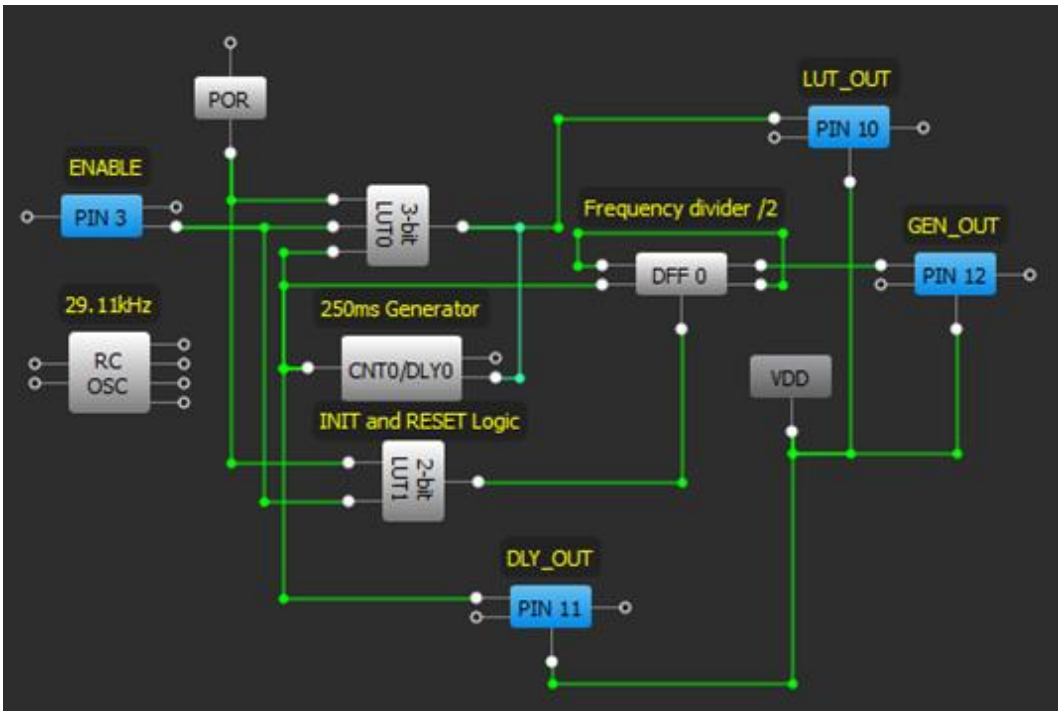


Figure 4.Configurable Generator Circuit in GreenPAK2 Designer

About the Author

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Background: Roman Yankevych graduated from Lviv Polytechnic National University in 2009, studying at the Department of Radioelectronic Devices and Systems. For the time being he's working with Configurable Mixed Signal ICs (CMICs) and their application notes. Moreover, for more than 5 years his particular sphere of interest has included signals processing in radar and communication systems.

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A	Roman Yankevych	08/01/2013	New application note

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