GreenPAK Macro Circuit Design: Digital Deglitch Filter

Author: Volodymyr Batig
Date: August 2013

Introduction

Digital deglitch filter are functions the main purpose of which is filtering signals according to their temporal parameters. This simple unit has one input and output, main part of which is delay cell that “decides” to pass through input signal or not, see figure 1.

Digital Deglitch circuit design

As can be seen on Figure 4, Digital Deglitch is implemented using 2-bit LUT1 (look-up table) connected to data input of CNT/DLY0, output of which is connected to Deglitch_OUT (PIN12) with Output Enable connected to VDD as it is configured as push-pull.

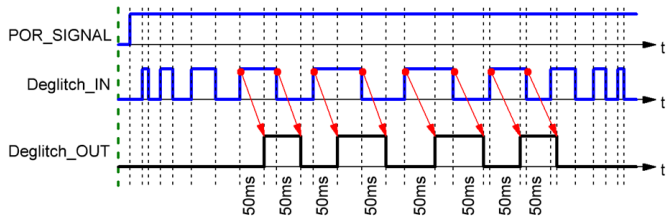

Figure 1. Digital Deglitch Filter Timing Diagrams

Digital Deglitch circuit analysis

POR and input PIN are connected to 2-bit LUT1 input (see on Figure 4) which is not involved in the formation of the delay, it serves for correct startup of the delay cell, see on Figure 2. If HIGH period of input signal is equal or bigger of the delay time of CNT0/DLY0 cell (counter data + 1 divided by the frequency of the oscillator, in this case T≥(1454+1)/29.11kHz ≈ 50ms). CNT0/DLY0 is sourced from RC OSC and has enough time to count down from 1454 to 0 and signal will be passed through circuit to Deglitch_OUT (PIN12). In the opposite case CNT0/DLY0 will rerun at each HIGH period of input signal and will not pass any signal on the output of CNT0/DLY0 cell.

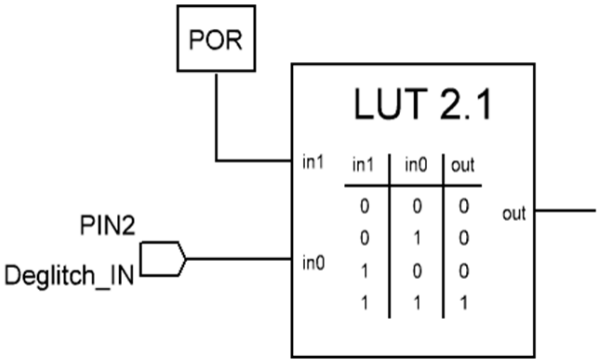

Figure 2. Input LUT Truth Table

Functionality waveform of real Digital Deglitch Filter circuit created in GreenPAK2 Designer is shown on Figure 3 where Channel1 (yellow/top line) – PIN2 (Deglitch_IN), Channel2 (light blue/bottom line) – PIN12 (Deglitch_OUT). As can be seen from Figure 3 the real waveform coincides with the theoretical shown in Figure 1.

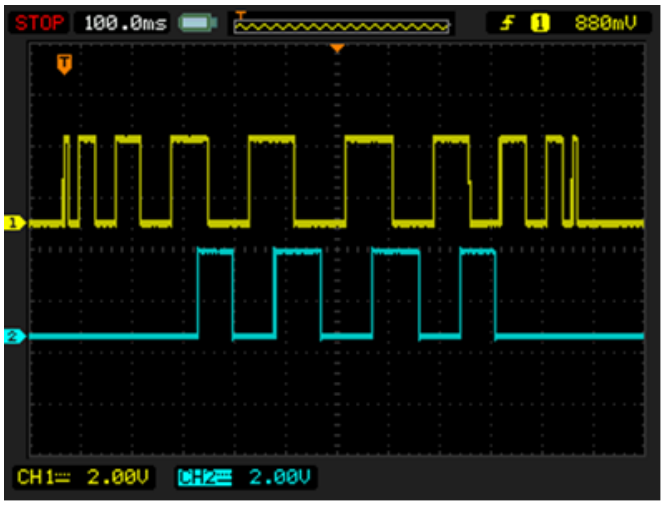

Figure 3. Digital Deglitch functionality waveforms

Related Files

Programming code for **GreenPAK Designer.**

Conclusion

Digital Deglitch is a simple and very useful function which helps to solve problems when it comes about input of noisy and signals with glitches, for instance from physical switches or push buttons.

Note: for proper operation of circuit don't forget to correctly configure input and output pins. In case of the schematic you see on Figure 4 input is configured as digital input with Schmitt trigger, and output as push-pull.

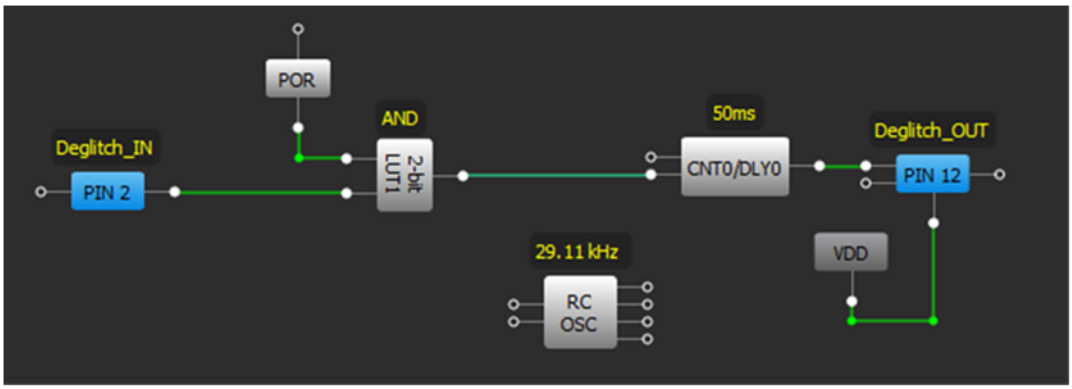

Figure 4.Digital Deglitch Filter Circuit in GreenPAK2 Designer

About the Author

Name: Volodymyr Batig

Background: Volodymyr Batig graduated from Ivan Franko Lviv National University in 2012, studying at the Department of Medical and Biomedical Electronics. Presently he's working with Configurable Mixed Signal ICs (CMICs) and their application notes. Moreover, for more than 10 years his particular sphere of interest has included design, modernization and repair of everything related to electronics.

Contact: volodymyrb@silego.com

Document History

Document Title: GreenPAK Macro Circuit Design: Digital Deglitch Filter

Document Number: AN-1012

Revision	Orig. of Change	Submission Date	Description of Change
A	Volodymyr Batig	08/19/2013	New application note

Worldwide Sales and Design Support

Silego Technology maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at **Silego Locations**.

About Silego Technology

Silego Technology, Inc. is a fabless CMIC company headquartered in Santa Clara, California, with operations in Taiwan, and additional design/technology centers in China, Korea and Ukraine.

SILEGO TECHNOLOGY

Silego Technology Inc.
1715 Wyatt Drive
Santa Clara, CA 95054

Phone : 408-327-8800
Fax : 408-988-3800
Website : www.silego.com