GreenPAK Macro Circuit Design: Active HIGH Latch

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Introduction

Digital Latches are functions with deep feedback for holding its state after switching by input signal from one state to another until Reset signal comes. This simple unit has one input and output, main part of which is 4-bit LUT0 (look-up table) with feedback to “memorize” input signal and hold it, see Figure 1.

Generator Circuit Design

As you can see on Figure 4, latch is implemented using 4-bit LUT0 (look-up table) with POR connected to its IN3, LATCH_IN (PIN2) to IN2, LATCH_RESET_IN (PIN3) to IN1, feedback from 4-bit LUT0 output to IN0, and output connected to LATCH_OUT (PIN12) with Output Enable connected to VDD as it is configured as push-pull.

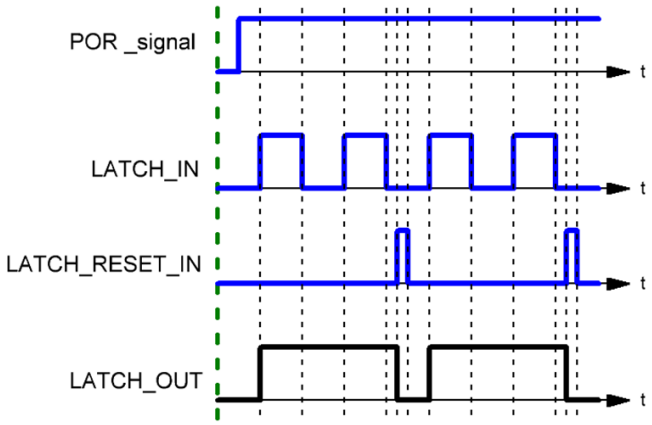

Figure 1. Latch Timing Diagram

Digital Latch circuit analysis

When POR signal goes HIGH, it allows to set latch by HIGH signal level on LATCH_IN (PIN2) input, due to feedback, this state will be hold even if input signal will go LOW. If LATCH_RESET_IN is HIGH, LATCH_OUT (PIN12) will go LOW (see on Figure 2) and due to specific truth table configuration it will stay LOW until next HIGH level appears on LATCH_IN.

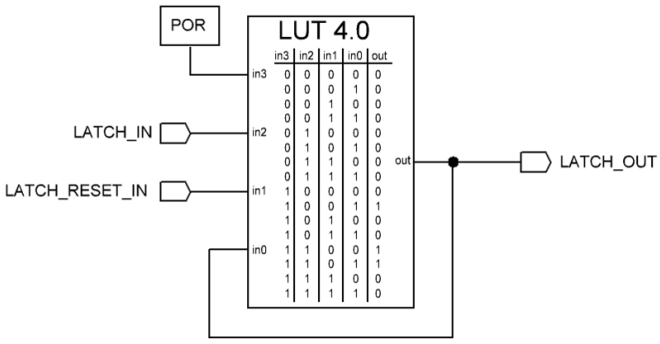

Figure 2. Latch Truth Table

Functionality waveform of real latch circuit created in GreenPAK2 Designer is shown on Figure 3 where Channel1 (yellow/top line) – PIN2 (LATCH_IN), Channel2 (light blue/2nd line) – PIN3 (LATCH_RESET_IN), Channel3 (magenta/bottom line) – PIN12 (LATCH_OUT). As can be seen from Figure 3 the real waveforms coincide with the theoretical shown on Figure 1.

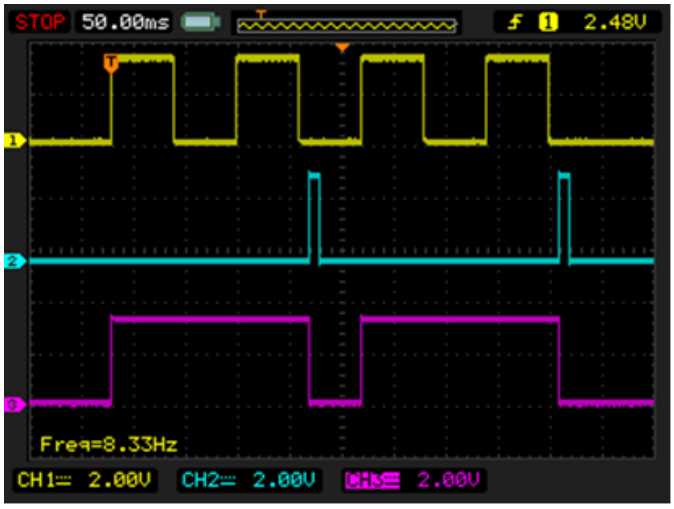

Figure 3. Digital Deglitch functionality waveforms

Related Files

Programming code for **GreenPAK Designer**.

Conclusion

Latch is a simple but useful function which helps to solve problems when it comes about holding the state of signals or detecting short peaks. It could be easily reconfigured to sense LOW level or to latch LOW.

Note: for proper operation of circuit don't forget to correctly configure input and output pins. In case of schematic you see on Figure 4 inputs are configured as digital input with Schmitt trigger, and output as push-pull.

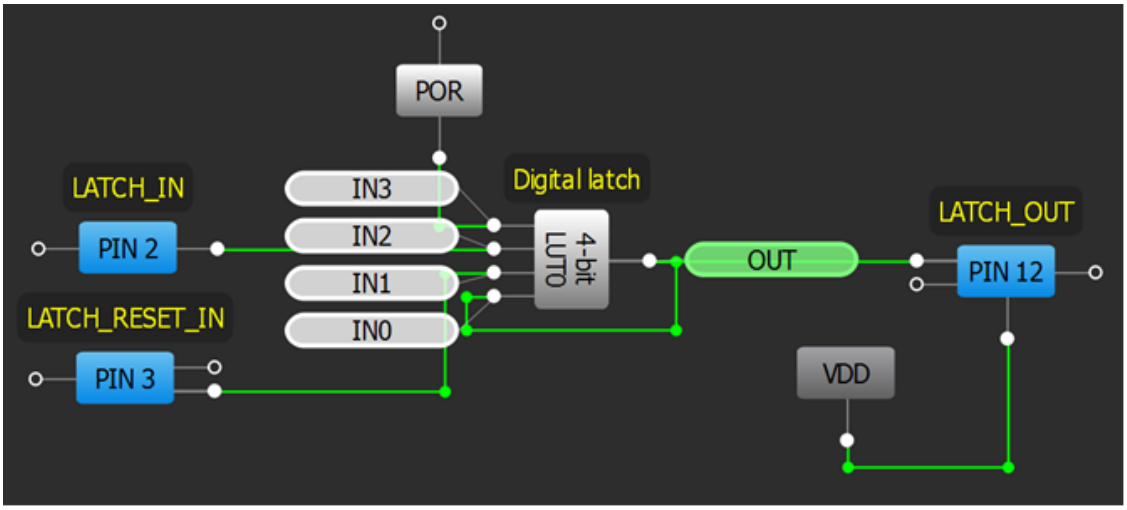

Figure 4.Digital Deglitch circuit in GreenPAK2 Designer

About the Author

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Background: Volodymyr Batig graduated from Ivan Franko Lviv National University in 2012, studying at the Department of Medical and Biomedical Electronics. Presently he's working with Configurable Mixed Signal ICs (CMICs) and their application notes. Moreover, for more than 10 years his particular sphere of interest has included design, modernization and repair of everything related to electronics.

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Document History

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Revision	Orig. of Change	Submission Date	Description of Change
A	Volodymyr Batig	08/19/2013	New application note

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