GreenPAK Macro Circuit Design: Serial to Parallel/Parallel to Serial (S2P)

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Introduction

The Serial to Parallel / Parallel to Serial block (S2P) has two 16-bit registers (2 bytes) that are used for data transfer. External clock signal comes from PIN5 and nCSB (active LOW Enable Control Signal) comes from the Connection Matrix Out. For serial to parallel operation (S2P) serial data input (MOSI) comes from PIN6. S2P will produce a 16-bit parallel data output (S2P<15:0>) where the MSB <15:8> can be used by PWM/DCMP0 and PWM/DCMP1 logic cells, while LSB <7:0> can be used by PWM/DCMP2, FSM0, and FSM1 logic cells. For parallel to serial operation (P2S), the 8-bit parallel data in (PAR IN<15:8>) comes from CNT1 logic cell. PIN 6 is used to output the 8-bit serial data output (MISO) signal.

Serial to Parallel Operation

S2P mode is the default option of S2P cell block. Its purpose is to convert serial data that comes on its input into internal parallel data that can be used by other blocks, such as DCMPs, and FSMs. The process of conversion is synchronous to external clock (rising edges). As S2P is a 16 bit cell, it takes 16 clock's rising edges (clocks) to read the data and convert it into parallel data. During serial data readout nCSB input should be set LOW until the readout is finished.

The screen capture of S2P and DCMP can be seen on Figure 2. S2P is connected to PIN4, PIN5, PIN6, which are configured as digital inputs without Schmitt trigger and without any pull up/down resistors. Output OUT+ of DCMP will switch HIGH after the first rising edge of RS OSC that comes after 16th falling-edge of CLK input signal, when IN+ > 15 (data written into DCMP register). Output EQ of DCMP will be HIGH when IN+ = 15. All outputs are configured to be push pull.

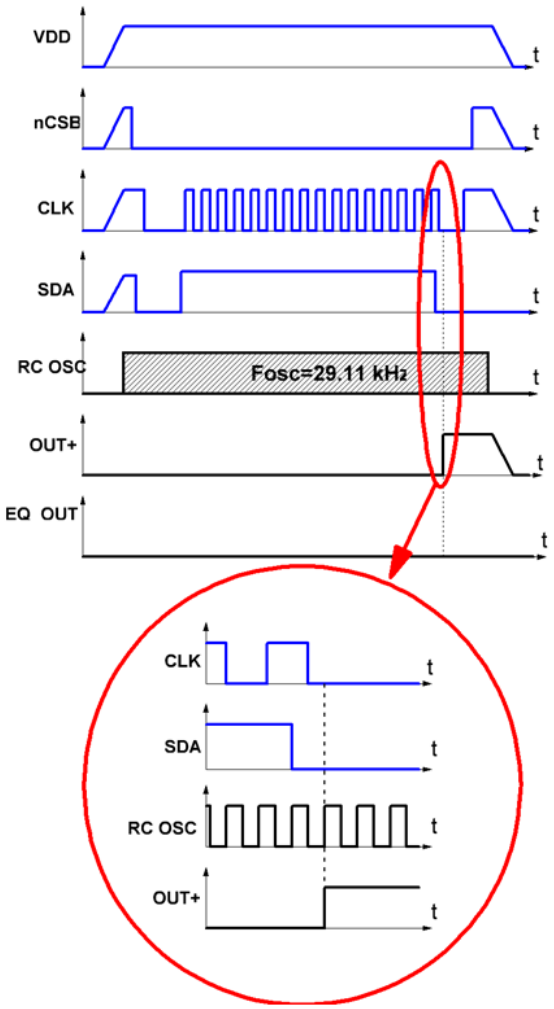

Figure 1. Serial to Parallel timing diagram. Blue lines are inputs, black are outputs

Serial to Parallel Circuit Analysis

Figure 3 shows the waveform of the project. If serial data is $11111111_2=255_{10}$ output OUT+ will be HIGH. When serial data is $00001111_2=15_{10}$ output OUT+ will be LOW, and output EQ_OUT will be HIGH.

Serial data, clock and nCSB input signals where generated by the GreenPAK2 Emulation Tool. The designer software has a possibility to connect logic, signal and clock generators to input pins.

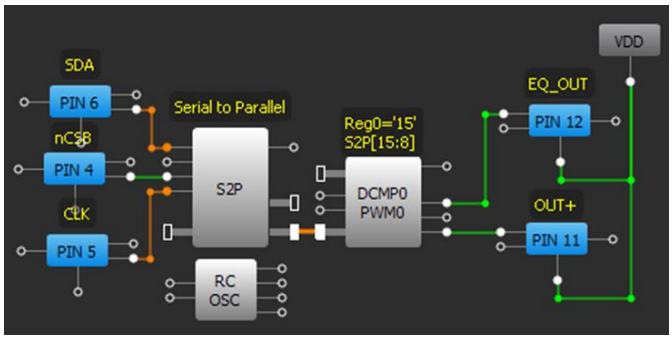

Figure 2. Serial to Parallel block diagram

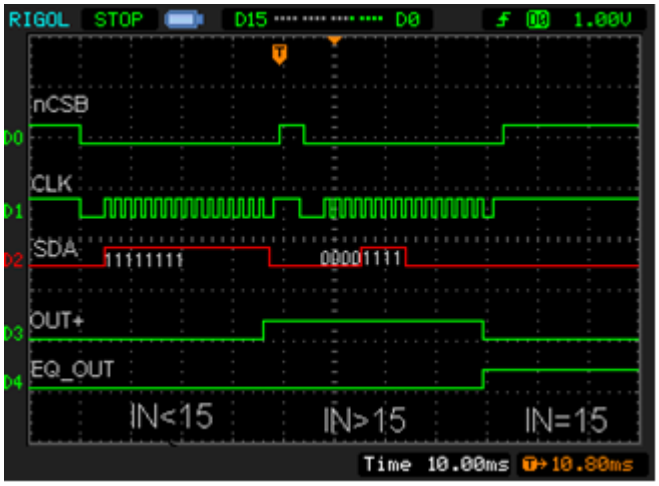

Figure 3. Serial to Parallel output waveform. Top line is S2P nCSB input, 2nd line is S2P CLK input, 3rd line – S2P MOSI input, 4th line – DCMP OUT+ output, bottom line – DCMP EQ output

Parallel to Serial Operation

P2S is a mode of S2P block that can be selected from the Mode options in the GreenPAK 2 Designer software. In this mode, the S2P block will convert the captured data from the connected to it CNT1 block. CNT1 is configured to have Counter Data = 255 or 28. This block sources its clock from internal RC OSC. The capture event happens on the rising, falling or both edges of CAPTURE signal. This can be selected by configuring DLY3 edge select option.

The data on CNT1 output changes with every RC OSC clock, so to make the change controllable, CNT/DLY3 is configured to be a both edge delay with a counter data 15. When the CAPTURE input signal goes HIGH (rising edge appears) S2P block will capture the data from CNT1 and output it. If the CAPTURE signal is long enough (more than 15+1 RC OSC clock) CNT1 will count down 16 clocks and stop because RC OSC is configured to be ON only during delay cell operation. So, if the CAPTURE signal goes LOW (falling edge) the second capture event happens that will convert CNT1 output parallel data in to serial.

Also to make S2P block operational external clocking signal is required. In this example, the RC OSC clocking signal is applied to PIN5 IN. The pin must be configured to be bi-directional, by setting its mode as digital input and connecting OE node to HIGH level signal (VDD). With such configurations PIN5 will be output and input at the same time that allows transferring signal from RC OSC to S2P blocks. S2P serial data will output with every rising edge of the CLK signal that comes from PIN5.

The screen capture of P2S (S2P block in P2S mode) circuit can be seen on Figure 6. PIN 6 is used to output the 8-bit serial data out (MISO) signal. PiN6 is configured as push pull.

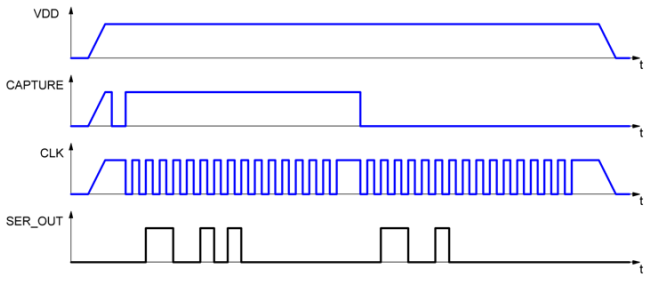

Figure 4. Parallel to serial timing diagram

Parallel to Serial Circuit Analysis

Figure 6 shows the scope shot of the design. If parallel data P2S PAR IN is 96_{10} MISO output will be 01100000_2. When parallel data P2S PAR IN is 80_{10} output MISO will be 01010000_2.

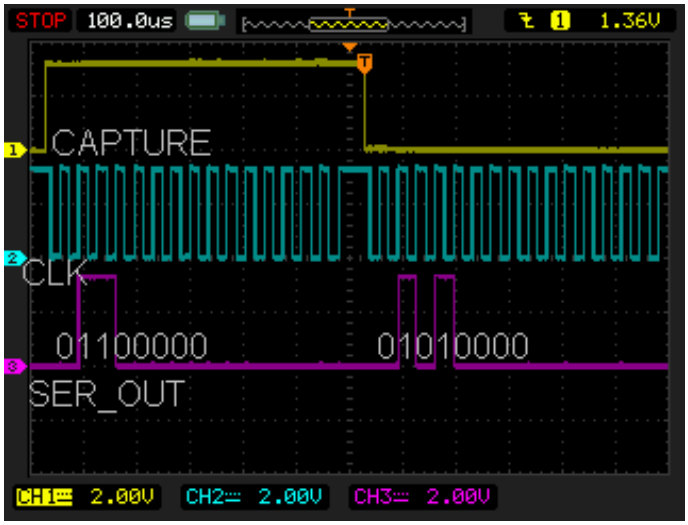

Figure 5. Parallel to serial output waveform. Top line is P2S CAPTURE input, 2nd line is P2S CLK input, bottom line – P2S MISO output

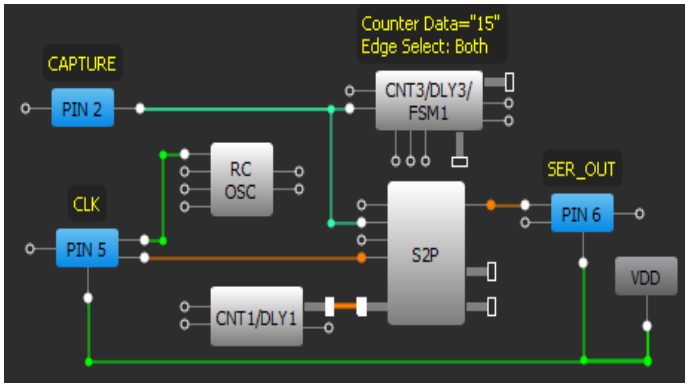

Figure 6. Parallel to Serial block diagram

Related Files

Programming code for **GreenPAK Designer**.

Conclusion

The S2P block is a standard communication block used in many devices and systems. The ease of use and configurability of this block in GreenPAK2 devices makes it a perfect candidate to replace bigger and more expensive microcontrollers. The S2P block can be configured in one of two modes: S2P or P2S, but the switching between these modes during device operation is impossible.

About the Author

Name: Bogdan Holod

Background: Bogdan Holod graduated from Lviv Polytechnic National University in 2011 and received a Master's Degree in Radio engineering devices, systems and complexes. Since 2012 he has been working as a design engineer and has got experience in designing low power analog systems, developing designing guidelines of digital and analog electronic circuits.

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Revision	Orig. of Change	Submission Date	Description of Change
A	Bogdan Holod	08/22/2013	New application note

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