Author: Olexander Reshotka
Date: September 3, 2013

H-bridge Application

An H-bridge is an electronic circuit that enables a voltage to be applied across a load in either direction. These circuits are often used in robotics and other applications to allow DC motors to run forwards and backwards.

H-bridges are available as integrated circuits, or can be built from discrete components: SWITCHES, RELAYS, TRANSISTORS or MOSFETS.

The term H-bridge is derived from the typical graphical representation of such a circuit. An H-bridge is built with four switches (solid-state or mechanical). When the switches S1 and S4 (according to the Figure 1) are closed (and S2 and S3 are open) a positive voltage will be applied across the motor. By opening switches S1 and S4 and closing switches S2 and S3, this voltage is reversed, allowing reverse operation of the motor.

Using the nomenclature above, switches S1 and S3 should never be closed at the same time, as this would cause a short circuit on the input voltage source. The same applies to the switches S2 and S4. This condition is known as “shoot-through”.

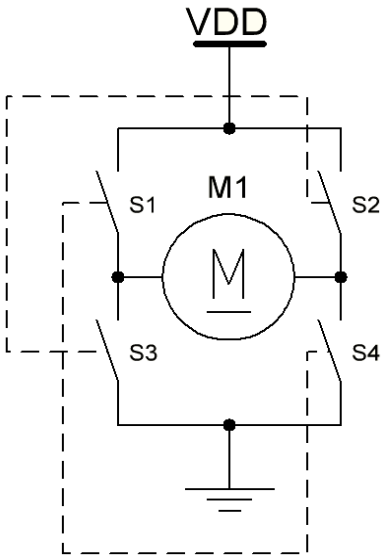

Figure 1. Structure of an H-bridge

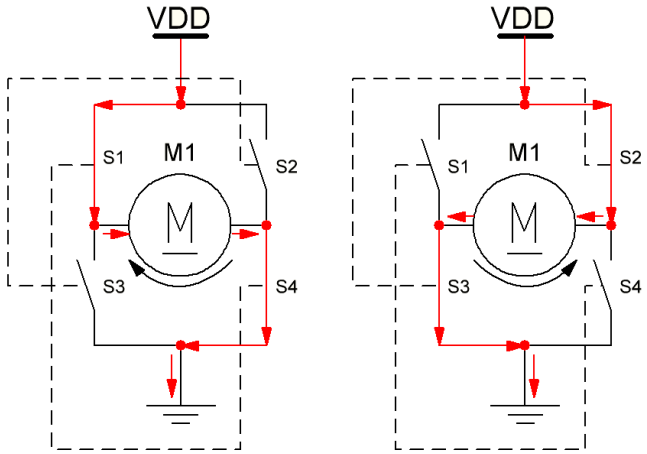

Figure 2. The two basic states of an H bridge

The type of motor can be a 3-pole (or 5-pole) with two brushes, similar to the following image.

To drive a motor forward and reverse, the circuit must deliver a voltage in one direction, then in the opposite direction.

It must also be able to deliver a "running current" (operating current, say up to 1 amp) and a "starting current" (up to 5 amps), and a "loaded current" (up to 5 amps). The transistors or other control elements must be capable of passing a "stalled current" (when the motor is powered but not turning) without being damaged.

Figure 3. Motor for H-bridge

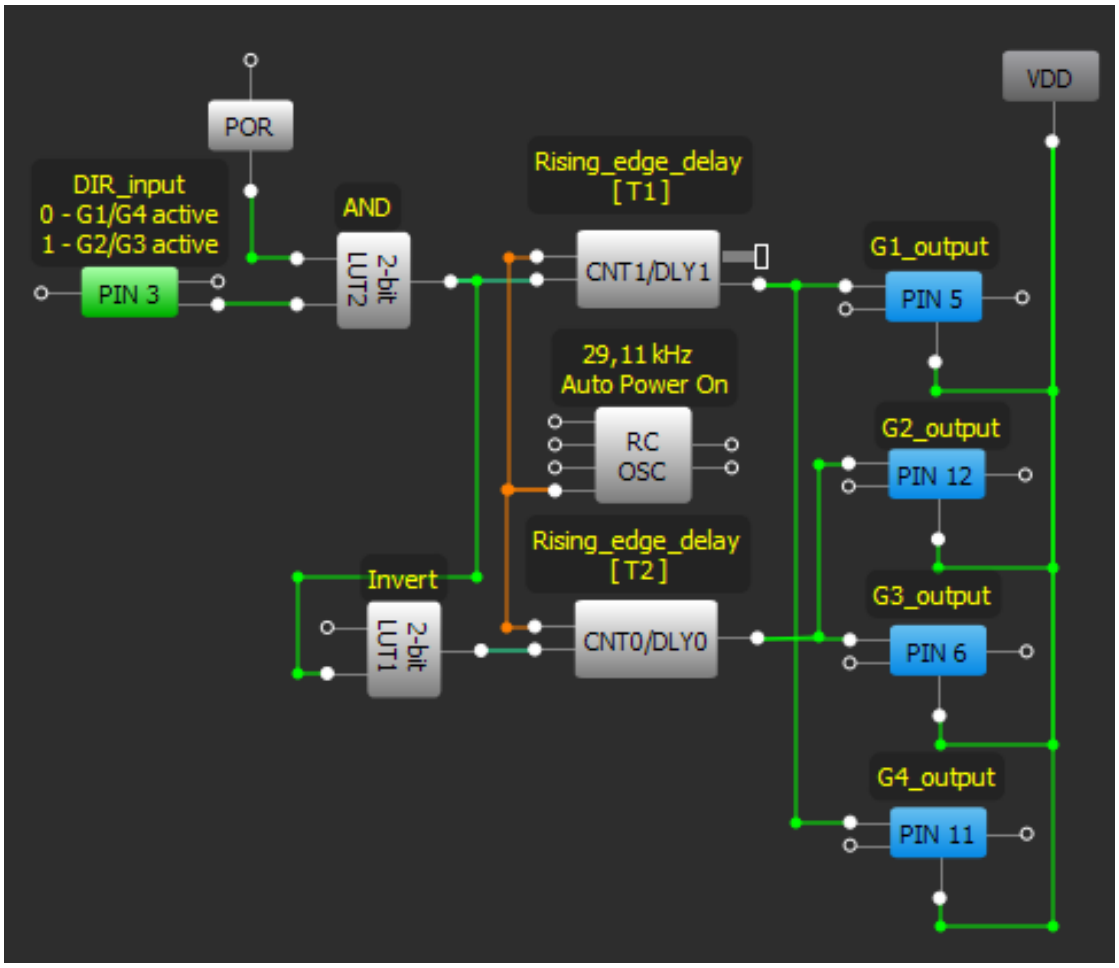

Figure 4. The internal structure of GreenPAK2 for driving the H-bridge with 6 MOSFETs

The power supply must be capable of delivering a high current so the motor will START-UP under load.

Design 1

The SLG46400 chip will be an H-bridge driver in our scheme. The input pins can be set in any startup combination. PINs 5, 6, 11 and 12 are selected as the outputs. The circuit will use two delay lines to form a "dead time". The dead time is critical to insure that shoot-through does not happen. It's a rising edge delay DLY1 (T1), and a falling edge delay DLY0 (T2). You can control the time of T1 and T2 by changing the value of Counter Data in the respective delay cells. The internal oscillator in the chip operates only during the delay cells operation, i.e. T1 and T2, so the chip will consume little current. AND logic gate and POR is used in the input circuit. This allows the chip to change its output states only when it is turned on. This design uses 6 transistors: 4 N-channel and 2 P-channel. Schottky diodes are installed in parallel to drain-source to eliminate inductive kicks. The resistors on the gates are used to close the MOSFETs by the default.

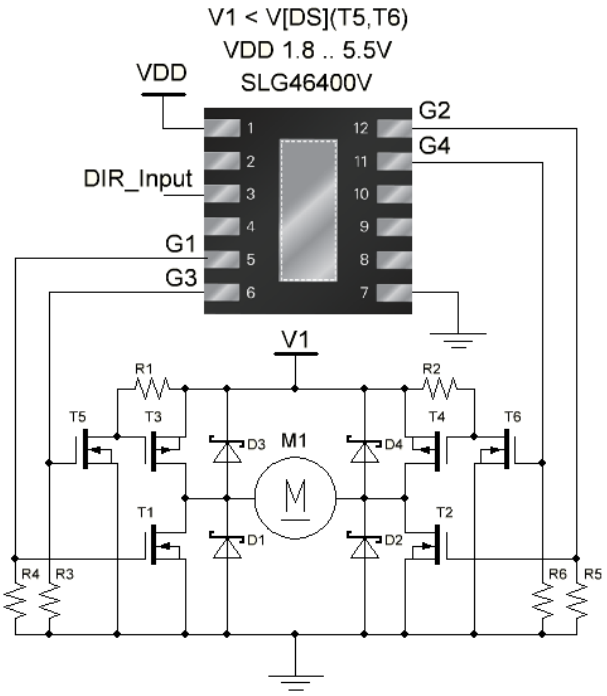

Figure 5. H-bridge with GreenPAK2 as a driver

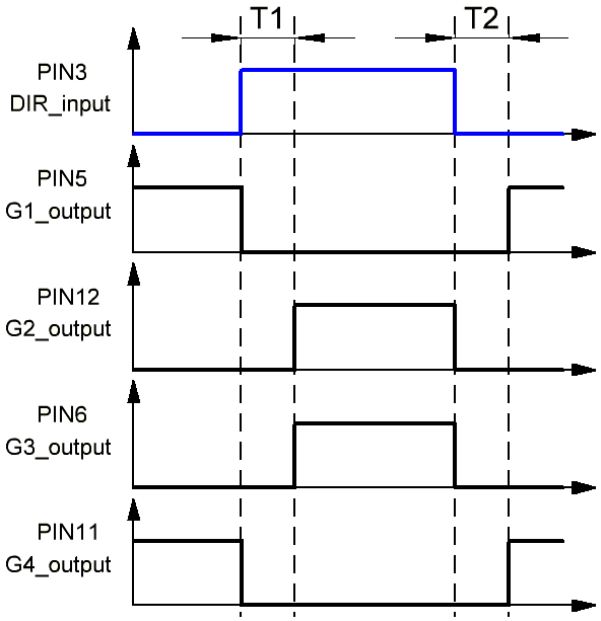

Figure 6. Design 1 timing diagram

When the chip is powered off, the motor is not running. After connecting the chip to power source, the motor starts whirling. The G1/G4 outputs will be active, when a logic LOW is present at PIN3. The G1/G4 outputs will be active, when logic HIGH is present at PIN3.

Design 2

This scheme is used when the power supply voltage of motor corresponds to the chip voltage. The supply voltage for this circuit is 1.8 V to 5.5 V. The advantage of this circuit is the use of only four mosfets.

When the chip is powered off, the motor is not running. After connecting the chip to power source, the motor starts whirling. The G1/G4 outputs will be active, when a logic LOW level is present at PIN3.

The G1/G4 outputs will be active, when logic HIGH level is present at PIN3.

As can be seen from Figure 9, T1 and T2 are a "dead time" - when the motor switches to the opposite side, chip switches all MOSFETs to the closed state. T1 and T2 are set by the DLY1 and DLY0 respectively.

- Minimal time of T1, T2 - 0.1us.
- Maximal time of T1, T2 - 6.75 seconds.

Design 3

The advantage of this scheme is the use of motor ON/OFF option. When a logical HIGH level is present at PIN4 the motor will rotate. When a logical LOW level is present at PIN4 the motor will stop immediately (MOSFETs will be closed). The rotation

will depend on the state of PIN3. The G1/G4 outputs will be active, when a logic LOW level is present at PIN3. The G1/G4 outputs will be active, when a logic HIGH level is present at PIN3.

The scheme is very flexible and can be performed in several ways.

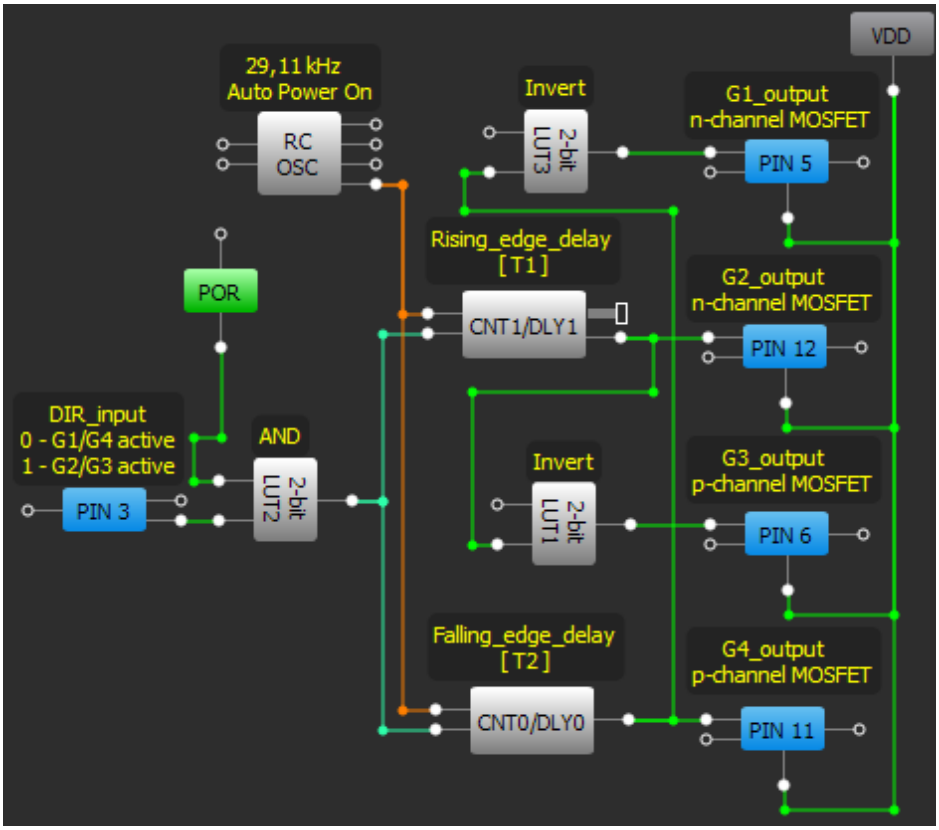

Figure 7. The internal structure of GreenPAK2 for driving the H-bridge with 4 MOSFETs

Design 4

This circuit is similar to the previous one. The feature of this scheme is using of additional delay between ON/OFF input and output state.

When a logical HIGH level is present at PIN4 the motor will rotate. When a logical LOW level is present at PIN4 the motor will stop immediately (MOSFETs will be closed). After applying the logical level HIGH to the PIN4 motor will start with some time delay of T1 or T2, depending on the direction selected. The G1/G4 outputs will be active, when a logic level LOW is present at PIN3. The G2/G3 outputs will be active, when logic level HIGH is present at PIN3.

When logic level LOW is present at PIN4, MOSFETs will be closed.

T1 and T2 are a "dead time" - when the motor switches to the opposite side, chip switches all MOSFETs to the closed state. T1 and T2 are set by the DLY1 and DLY0 respectively.

- Minimal time of T1, T2 - 0.1us.
- Maximal time of T1, T2 - 6.75 seconds.

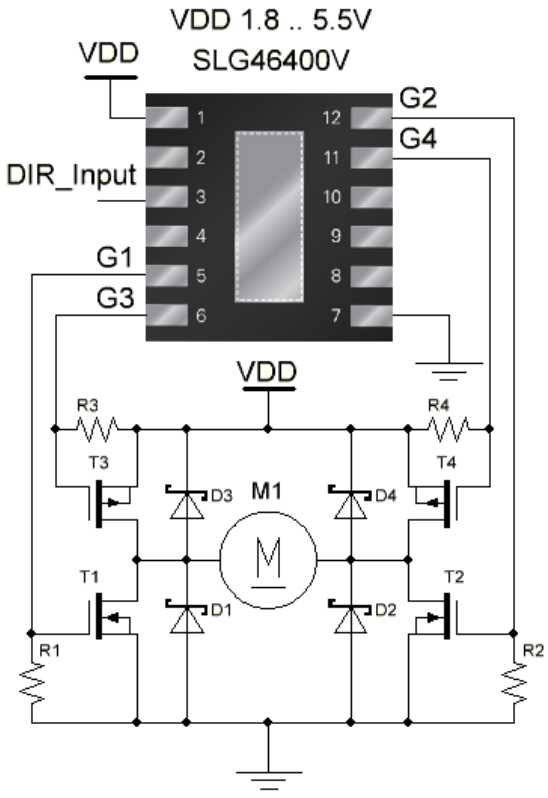

Figure 8. H-bridge with GreenPAK2 as driver controller

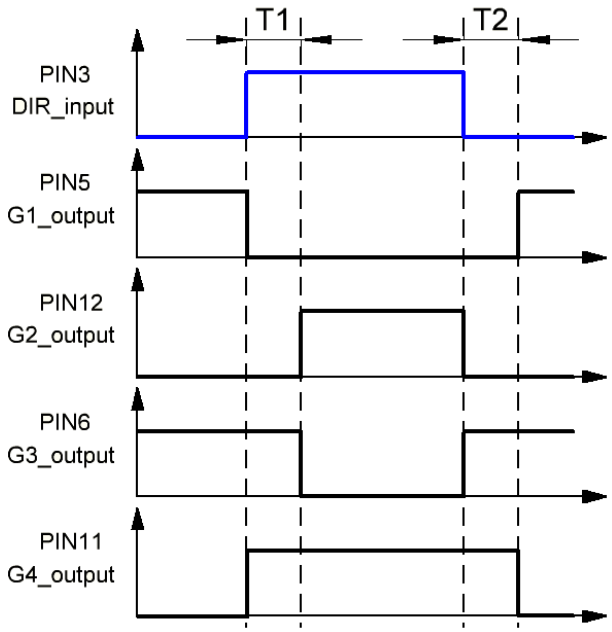

Figure 9. Design 2 timing diagram

Design 5

The advantage of the scheme is the use of motor over current protection (OCP). If more current will flow through the resistor R5, the more voltage will be dropped on this resistor. When the voltage on the resistor R5 exceeds the threshold of the comparator ACMP0, protection circuit will work and MOSFETs will switch to the closed state. Increasing of the current can be caused by overloading the motor pr breakdown of the switching circuits.

DLY2 and 2-bit LUT2 cells are used to successfully initialize the comparator at the start of the chip. Initialization time – 100 µs. PIN4 must be set to “Analog in”. The hysteresis in comparator is used to eliminate possible output glitches when the input voltage is close to the reference voltage of the IN-.

Diodes D5 and D6 are intended to protect the input of the chip exceeding the input voltage limit (if the H-Bridge is sourced from voltage bigger than VDD). The maximum input voltage is as big as VDD. In this circuit, the voltage drop at the limiting resistor is at 1.2 V.

The logic "1" will be present at the output Q of the DFF0, if a large current flows will through the load.

This will stop the motor.

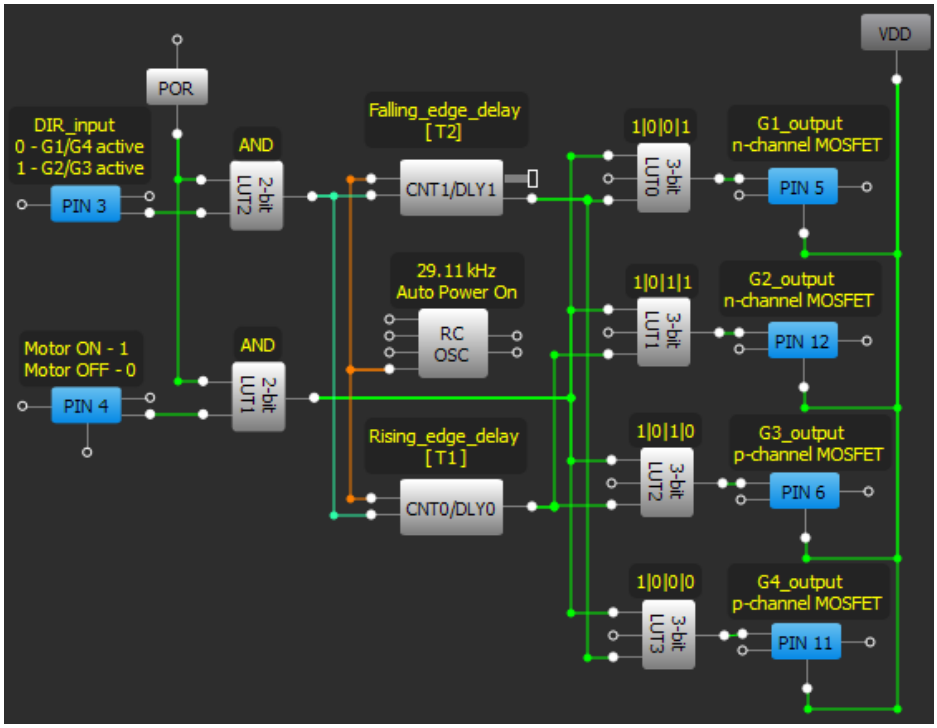

Figure 10. The internal structure of GreenPAK2 for driving the H-bridge with 4 MOSFETs and ON/OFF function

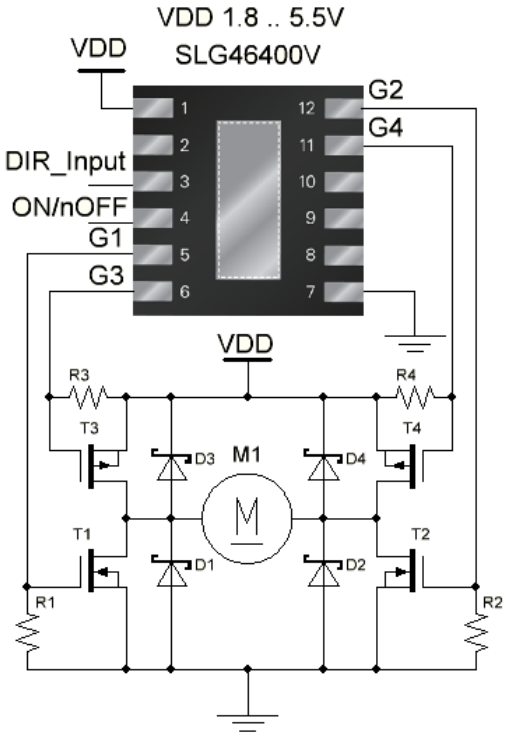

Figure 11. H-bridge with GreenPAK2 as driver controller

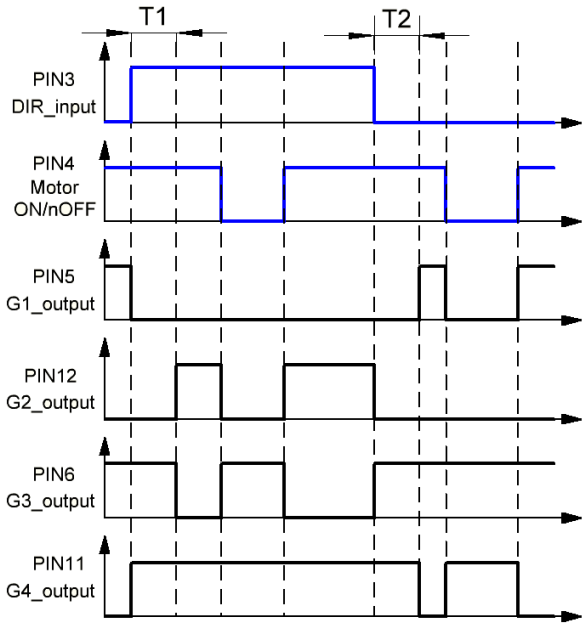

Figure 12. Design 3 timing diagram

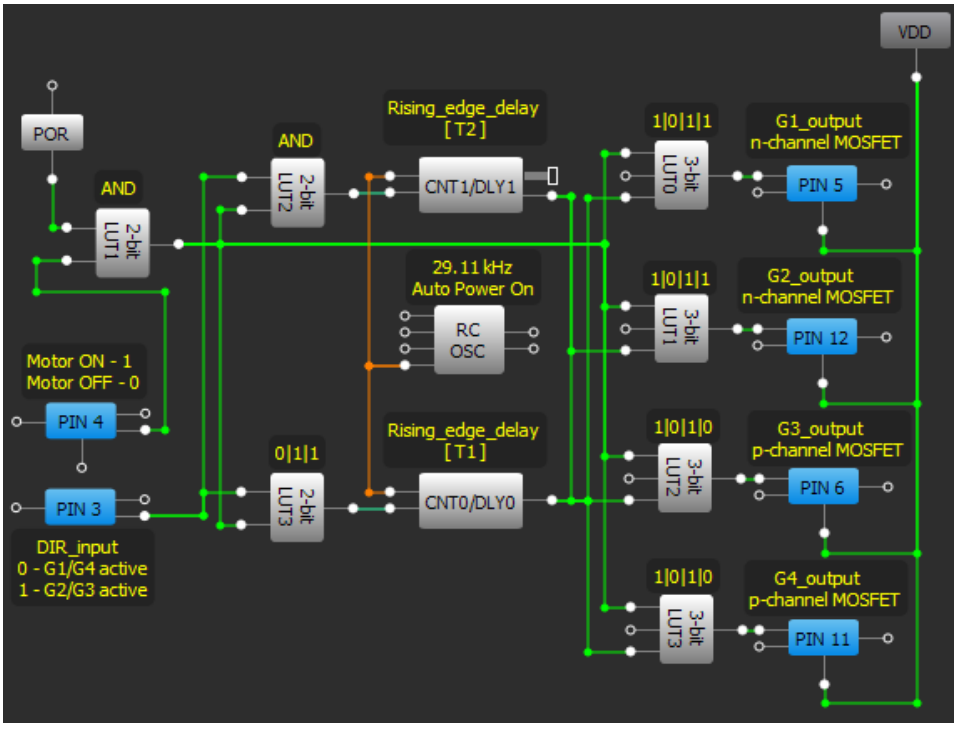

Figure 13. The internal structure of GreenPAK2 for driving the H-bridge with 4 MOSFETs and ON/OFF function

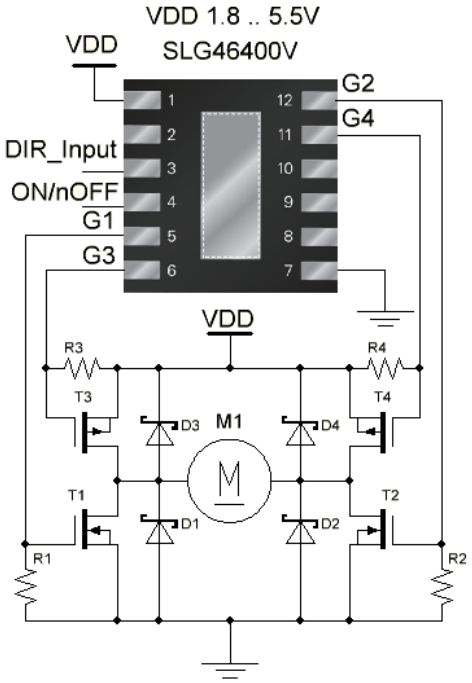

Figure 14. H-bridge with GreenPAK2 as driver controller

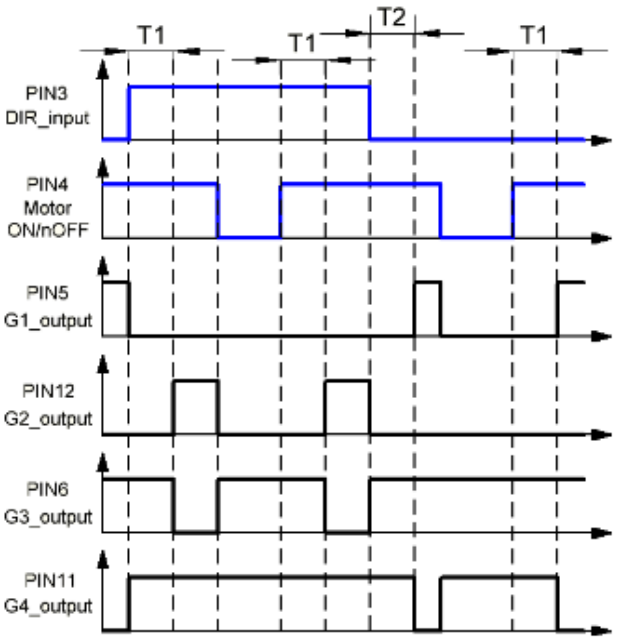

Figure 15. Design 4 timing diagram

Design 5

The advantage of the scheme is the use of motor over current protection (OCP). If more current will flow through the resistor R5, the more voltage will be dropped on this resistor. When the voltage on the resistor R5 exceeds the threshold of the comparator ACMP0, protection circuit will work and MOSFETs will switch to the closed state. Increasing of the current can be caused by overloading the motor pr breakdown of the switching circuits.

DLY2 and 2-bit LUT2 cells are used to successfully initialize the comparator at the start of the chip. Initialization time – 100 µs. PIN4 must be set to “Analog in”. The hysteresis in comparator is used to eliminate possible output glitches when the input voltage is close to the reference voltage of the IN-.

Diodes D5 and D6 are intended to protect the input of the chip exceeding the input voltage limit (if the H-Bridge is sourced from voltage bigger than VDD). The maximum input voltage is as big as VDD. In this circuit, the voltage drop at the limiting resistor is at 1.2 V.

The logic "1" will be present at the output Q of the DFF0, if a large current flows will through the load. This will stop the motor.

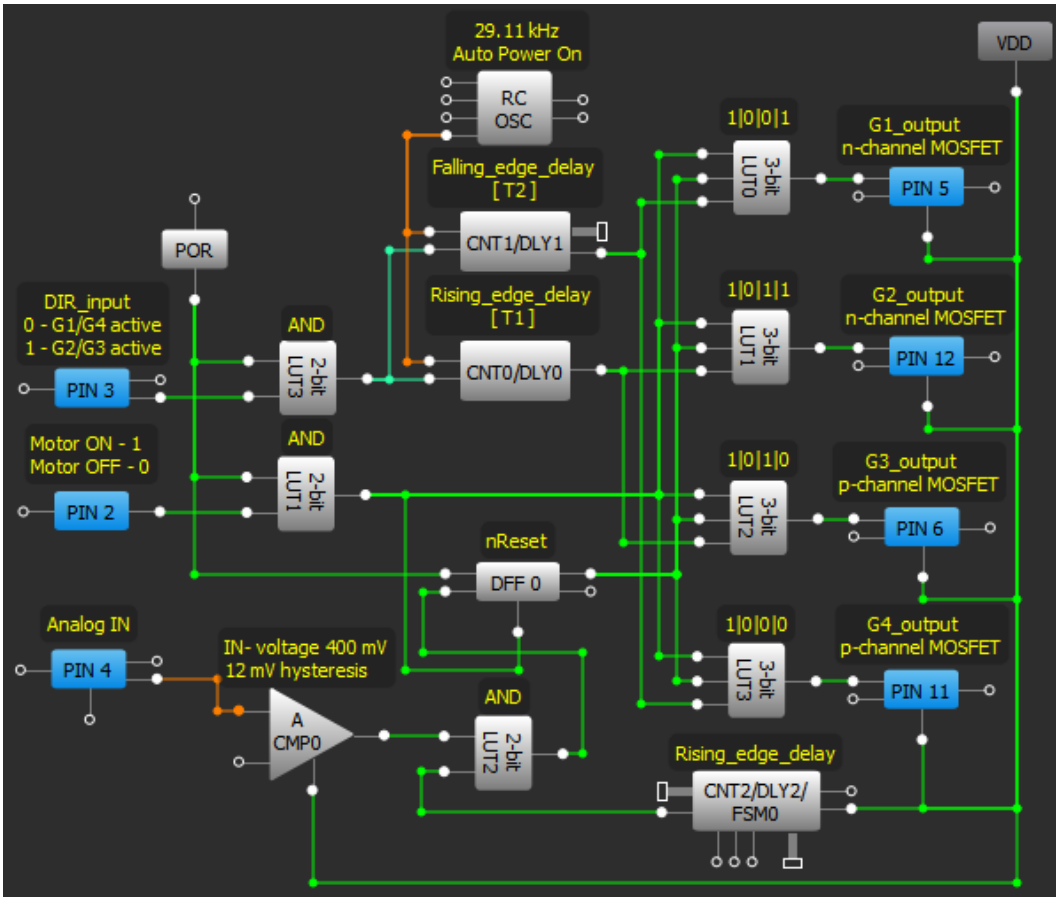

Figure 16. The internal structure of GreenPAK2 for driving the H-bridge with 4 MOSFET'S and motor over current protection

Design 6

The main feature of this scheme is the use of SPI code detector.

Serial Peripheral Interface (SPI) is a synchronous serial data protocol used by microcontrollers for communicating with one or more peripheral devices quickly over short distances. It can also be used for communication between two microcontrollers or another chip with SPI-interface. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

In this case, GreenPAK2 chip works in slave mode. When a logical HIGH is present at Input_nCSB PIN4, the chip is in an inactive state. When PIN4 receives a logical LOW, and PIN5 receives a clock pulses, the chip starts receiving 16-bit data from PIN6 Input_SDA.

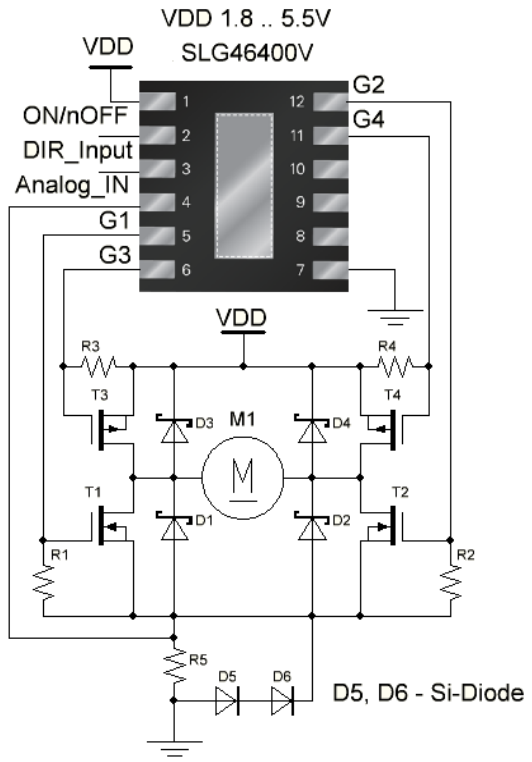

Figure 17. H-bridge with GreenPAK2 as driver controller

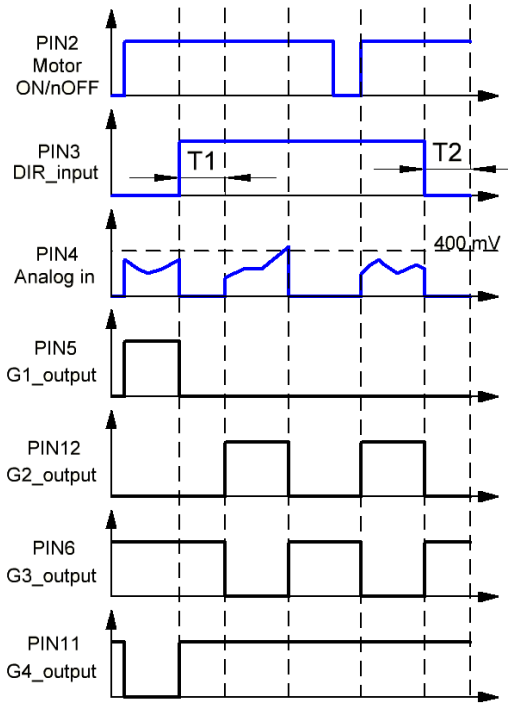

Figure 18. Design 5 timing diagram

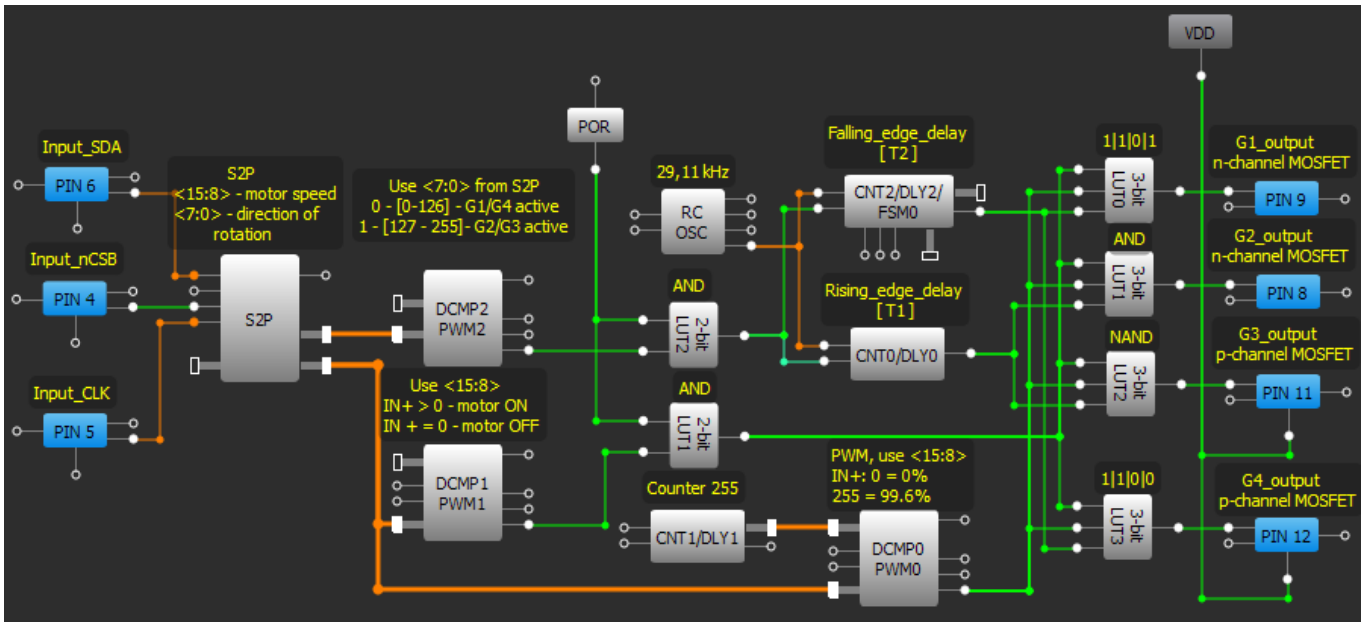

Figure 19. The internal structure of GreenPAK2 for driving the H-bridge with 4 MOSFETs, internal SPI-code detector and SPI-code PWM Duty cycle regulator

Device control is realized in the following way. First, MOSFETs T1-T4 are in a closed state. When the chip will now start receiving data, there may be the following conditions on the output. The most significant bit (MSB) in the SPI code determines the motor speed by varying the duty cycle. Per the duty cycle is responsible PWM0 block. It uses a MSBs and in direct proportion to its value changes the

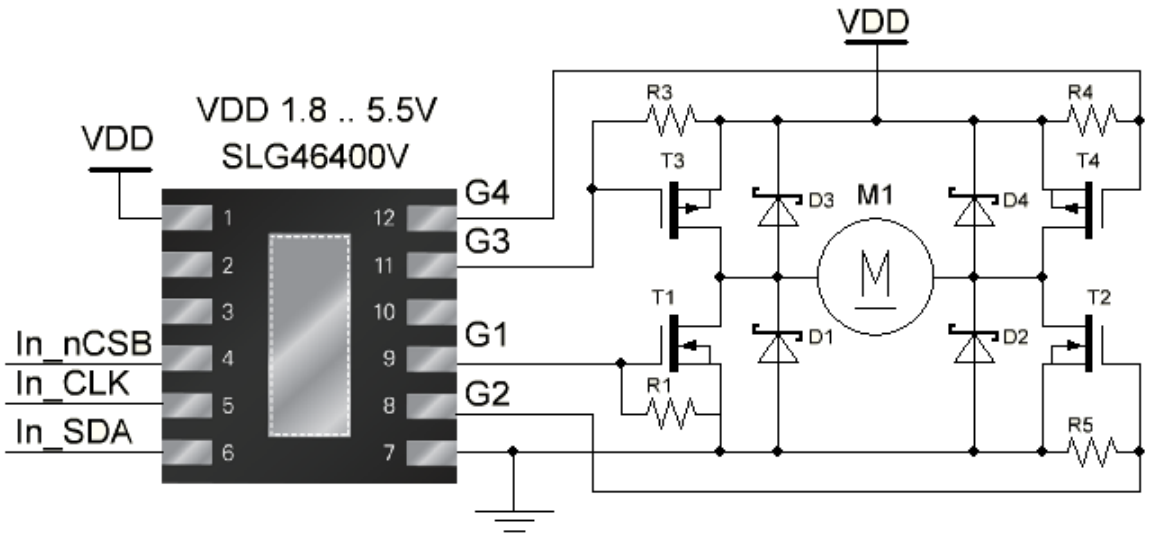

Figure 20. H-bridge with GPAK2 as driver controller

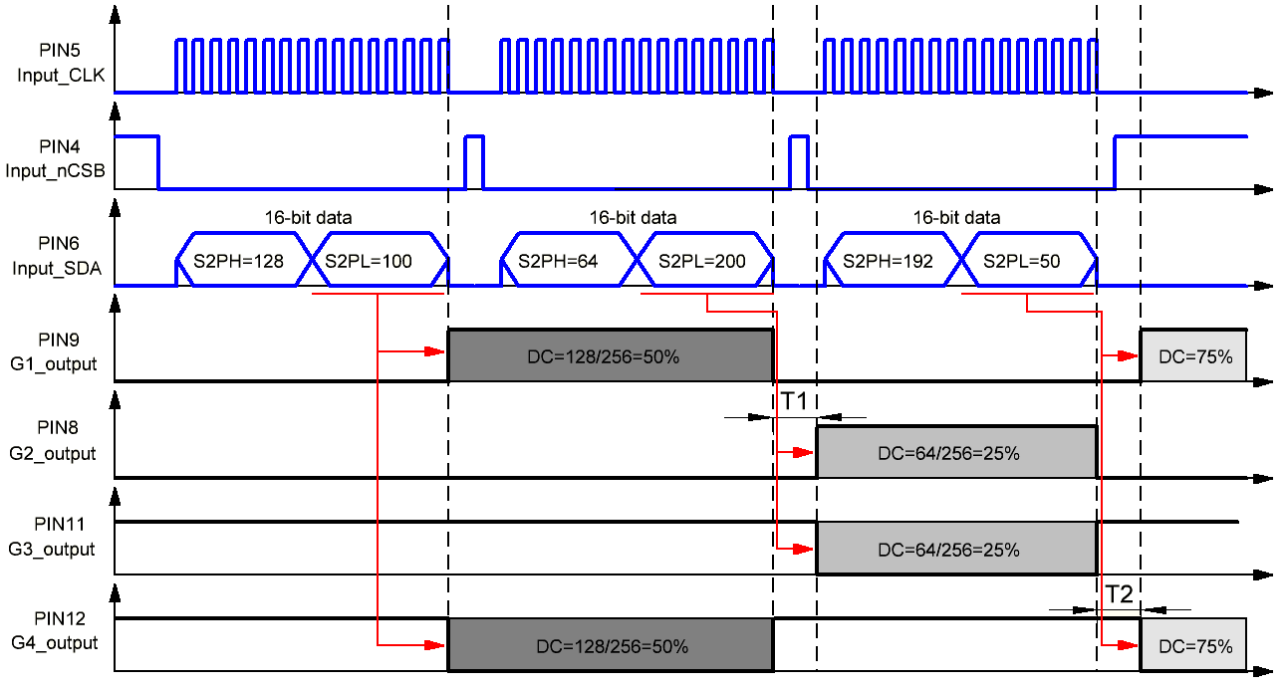

Figure 21. Design 6 timing diagram

width of the pulses. The duty cycle of the output pulses is calculated from the formula: DC=IN+/256. The minimum value can be 0%, the maximum value can be 99.6%. These values can be changed to the next interval – 0.39%-100%. It is set in the GreenPAK2 Designer inside the PWM0 “Duty Cycle” option. For the interval 0.39%-100% formula of output duty cycle pulse will be: DC=IN+ +1/256. The digital comparator DCMP1 is responsible for turning on/off the circuit. If the MSB is greater than zero - circuit is turned on. Digital comparator DCMP2 works with the least significant bits <7:0> (LSB) of SPI code. DCMP2 is responsible for direction of motor rotation. When the LSB is less than 126, outputs G1 and G4 will be active. When the LSB is more than 126, outputs G2 and G3 will be active. Counter data of the CNT1 must have value of “255” for correct PWM0 operation.

About the Author

Name: Olexander Reshotka

Background: Olexander Reshotka graduated from Lviv Polytechnic National University in 2012 and received a Master's Degree in "Micro- and nanoelectronics". Since 2012 he has been working with crystalline materials, measuring equipment, research acousto-optic interaction of the laser beam in crystalline materials. He has also practical skills in working with electronics, drafting circuit, making drawings of printed-circuit boards, repairing computer equipment, audio equipment.

Contact: **alexr@silego.com**

Document History

Document Title: H-bridge Motor Driver Using GreenPAK2

Document Number: AN-1023

Revision	Orig. of Change	Submission Date	Description of Change
A	Olexander Reshotka	09/03/2013	New application note

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Silego Technology Inc.
1715 Wyatt Drive
Santa Clara, CA 95054

Phone : 408-327-8800
Fax : 408-988-3800
Website : www.silego.com