# Button Reset Using GreenPAK2

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## Description

The SLG46400 can be used as a timer for resetting an electronic device where long reset times are needed. The long delay helps to avoid unintended resets caused by accidental key presses.

The GreenPAK based device has two- or more inputs for single- or dual-button resetting capability.

The I/O structure on the device has two output types: a push-pull output with 1mA driving capability for 1.8V power supply, 8mA at 5.0V power supply, and an open drain output with 5mA driving capability at 1.8V power supply (20mA for 5.0V power supply).

### Advantages of the chip are:

- Low Cost
- Small Package Size: TDFN-12 2.5mm x 2.5 mm
- Operating Temperature Range: -40°C to +85°C
- Supply Voltage from 1.8 V to 5 V
- Does not Require External Clock
- Configurable PINs
- Low Supply Current
- Low-Voltage Inputs are Present (HL=1.0V)

### Applications:

- Smart Phones
- Tablet's, E-Books
- MP3-players
- Network Routers
- Portable Consumer Electronics
- Navigation Devices
- Intelligent Instruments
- Embedded Control Systems

## Principles of Operation

The input pins are PIN4 and PIN5. 3-bit LUT5 is the input logic element. The LUT output is attached to the delay cell DLY0. DLY0 determines how much time the button must be pressed before generating RESET signal at the output of the chip. This time is denoted here as T1. It is specified by the parameter "Counter Data" in the DLY0 properties. The minimum period time delay is 0.1µs. Maximum period of time – 6.75s. The signal comes from DLY0 on rising edge detector. The edge detector is constructed using such elements as P_DLY and 3-bit LUT0. When logical HIGH signal comes from DLY0 the output of 3-bit LUT0 will generate 200ns pulse (at VDD= 1.8V) or 80 ns (at VDD=3.3 V), or 40 ns (at VDD=5.0V).

Then the signal from the 3-bit LUT0 comes on the delay cell DLY2 input. DLY2 is responsible for the duration of the reset signal pulse. This time is denoted here as T2. It is specified by the parameter "Counter Data" in the DLY0 properties. The minimum period time delay is 0.1µs. Maximum period of time – 6.75s. When the output RESET signal is appears the input IN2 of 3-bit LUT0 switches to logical HIGH which prohibits the rising edge detector to deliver pulses. This avoids RESET pulse to be constant output of the circuit, when the buttons are pushed for a long time. This is also useful if the buttons during RESET signal have been pressed again.

If you set a multiplexer, you can control the time of the RESET signal. See Figure 6. In this example, the multiplier will be equal to 3, because the frequency which will be supplied to the DLY2 is three times less when a logical HIGH signal will be present at PIN3.

The Power On Reset (POR) macro cell will produce a HIGH signal on its output when the power supply (VDD) rises to about 1.4-1.6V. External signals cannot affect the chip until the POR signal appears. It appears approximately in 7 ms, after powering up the chip.

PIN11 is configured as push-pull and correspond to RESET signal. Pin12 is configured with open-drain output. This output will be nRESET signal. The 2-bit LUT1 was used to create an inverter to generate nRESET signal.

The oscillator is set to “Auto Power On” mode. This makes power consumption smaller in standby mode (static inputs and outputs). Frequency is set to the minimum of 29.11 kHz, and can be increased to the desired value by changing the RC OSC block options.

**Advantages of this scheme are:**

- Variable and preprogrammed time of “RESET”
- Use of internal oscillator
- Variable and preprogrammed time before “RESET” (time the buttons are pressed) – 0.1us – 6.75s
- Free choice of I/O pin’s
- Two output types (open drain or push-pull)
- The maximum number of buttons or another additional I/Os – 8.

## Block Diagram

Internal structure of the chip is shown in Figures 1, 2, 4 and 6.

Buttons with different configurations can be connected to the chip. If the LOW state is active, one must use the circuit shown on Figure 2a. If the HIGH state is active, one must use the circuit shown in Figure 2b. Notice the 3-bit LUT5 truth table difference.

The Figure 3 shows the following timing diagrams. When the button S1 is pressed, then nothing happens. When the button S2 is pressed, then nothing happens. When both buttons S1 and S2 are pressed nothing happens if the buttons press time is shorter than for T1.

For the RESET signal to appear, buttons S1 and S2 must be pressed for time T1 or longer. RESET signal occurs for the time T2, after the time T1 passed. If both keys have not been released, the RESET signal will not appear again. If the buttons were pressed repeatedly during time T2, the RESET signal will not appear again too.

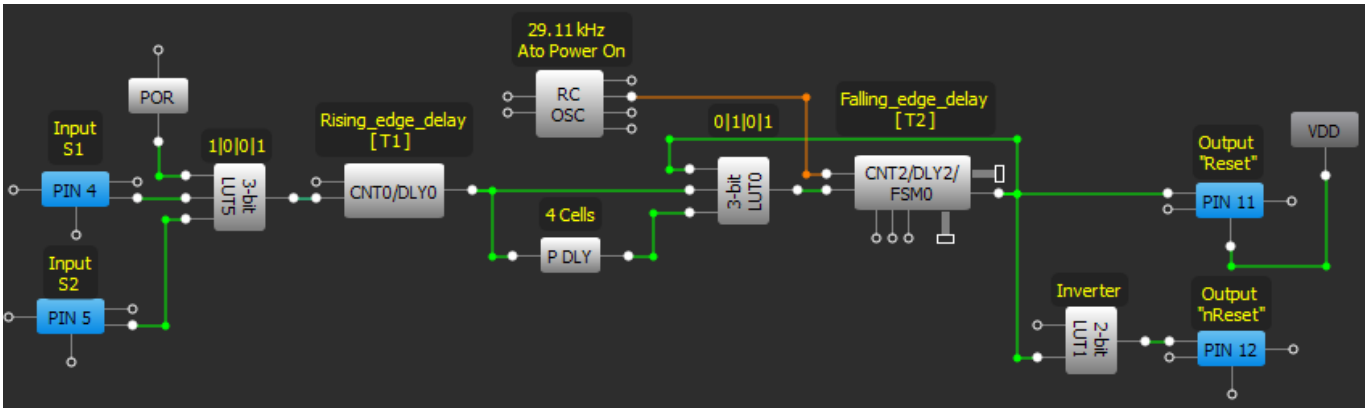


**Figure 1. 2-button reset. PIN4 and PIN5 are pulled up by the default**

Figure 4 represents the device that uses four buttons to create a reset signal. The difference of the scheme is that it has the input logic block is realized using 4-bit LUT0. In current design 4-bit LUT0 is configured as NOR logic cell. After input logic an AND cell is placed, which is based on 2-bit LUT2 with IN1 connected to POR block and IN0 connected to 4-bit LUT0 output. This scheme allows generating the RESET signal when all of four buttons are connected to the ground.

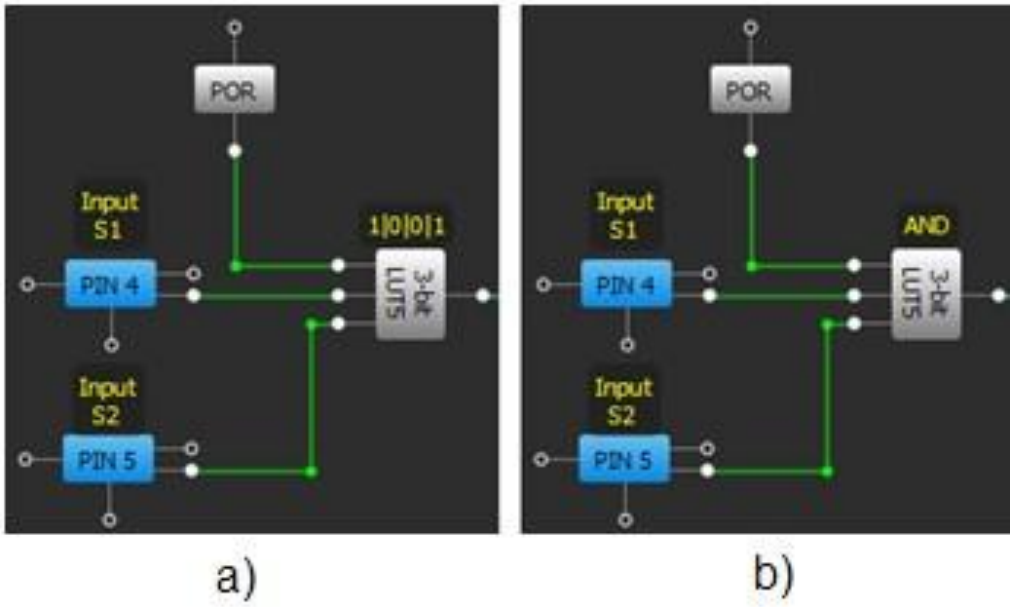


**Figure 2. Input logic for two types of buttons that are connected to the chip: a) active LOW; b) active HIGH**

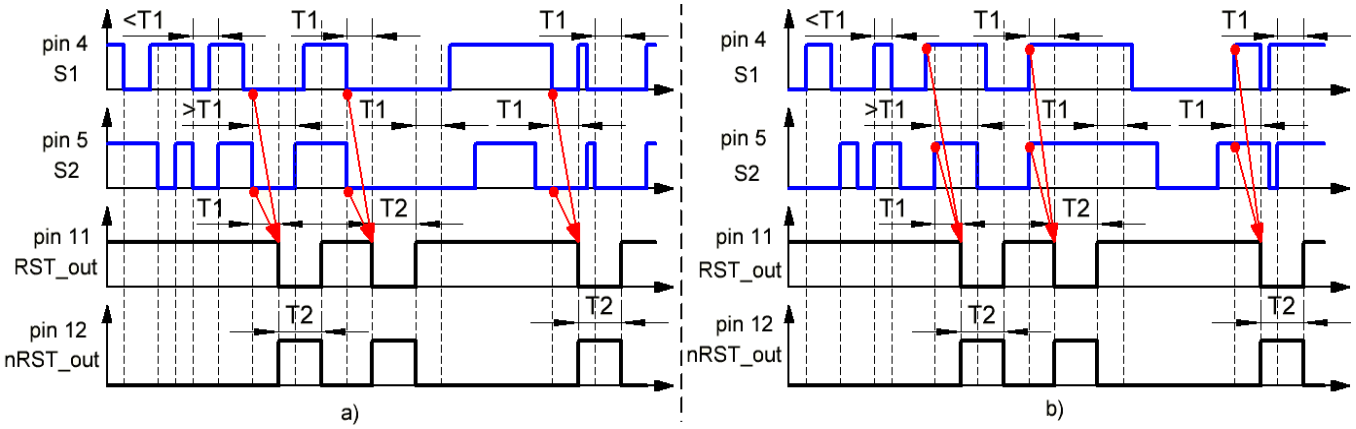


**Figure 3 Operation of the circuit shown in Figure 1: a) active LOW; b) active HIGH**

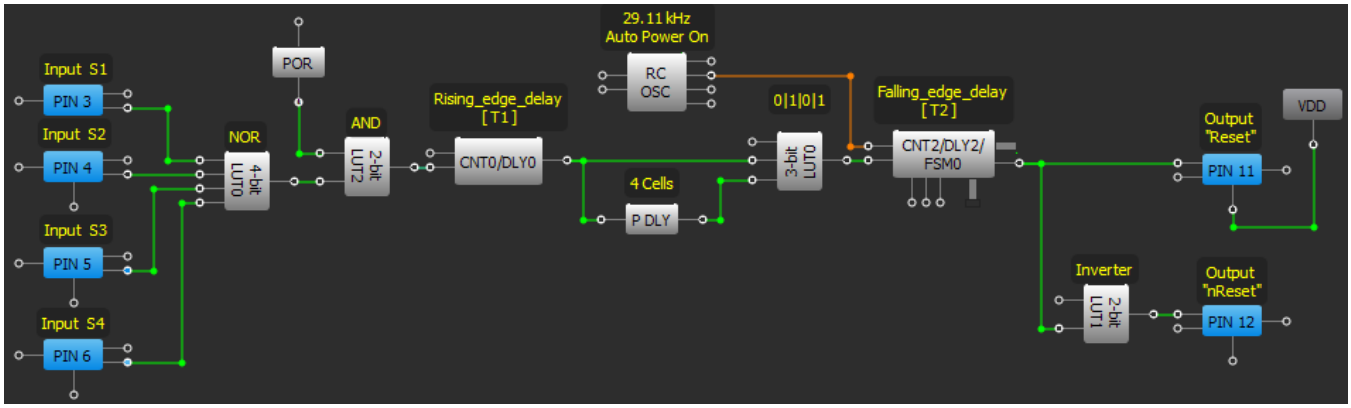


**Figure 4. 4-buttons Reset Design**

The design shown in Figure 6 has a distinguishing feature. The scheme allows adjusting the time of RESET signal. If the logic LOW signal is applied to

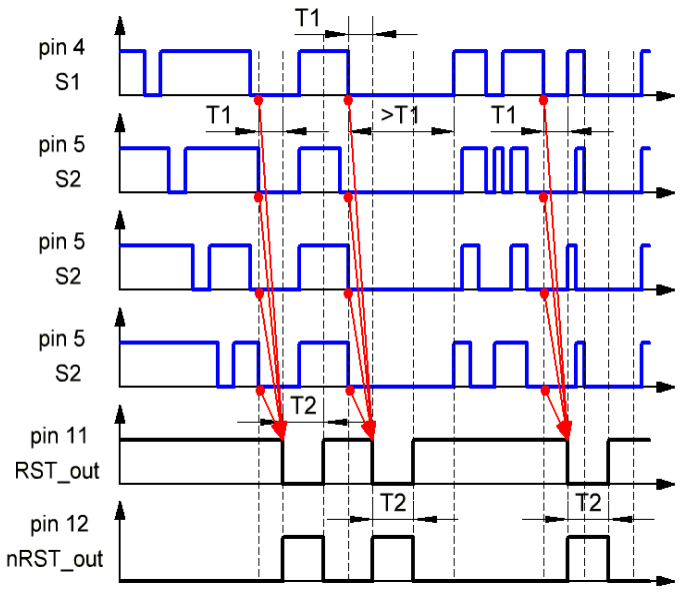


**Figure 5. Operation of the circuit shown in Figure 4**

PIN3, the time T2 will be defined by Counter Data of the delay DLY2 and RC OSC frequency divided by 4 (RC OSC/4 source is used). If the logic HIGH signal is applied to PIN3, then the reset signal time will increase three times. This happens due to the clocking signal frequency that is used by DLY2 will be three times slower, sourced from RC OSC output divided by 12. Division factor can be different if the counter is used to make a frequency division (factor can be as high as to 16384 which is equal to maximal Counter Data +1).

Circuit shown on Figure 6 can be modified to have unchangeable division factor during reset signal, see Figure 7.

The circuit shown in Figure 7 uses LATCH0 in addition. LATCH0 makes the signal on the MUX input fixed and holds it until the RESET signal ends. POR-block connected to the nRESET of the LATCH0 to ensure the initial state of the block to be LOW on Q output.

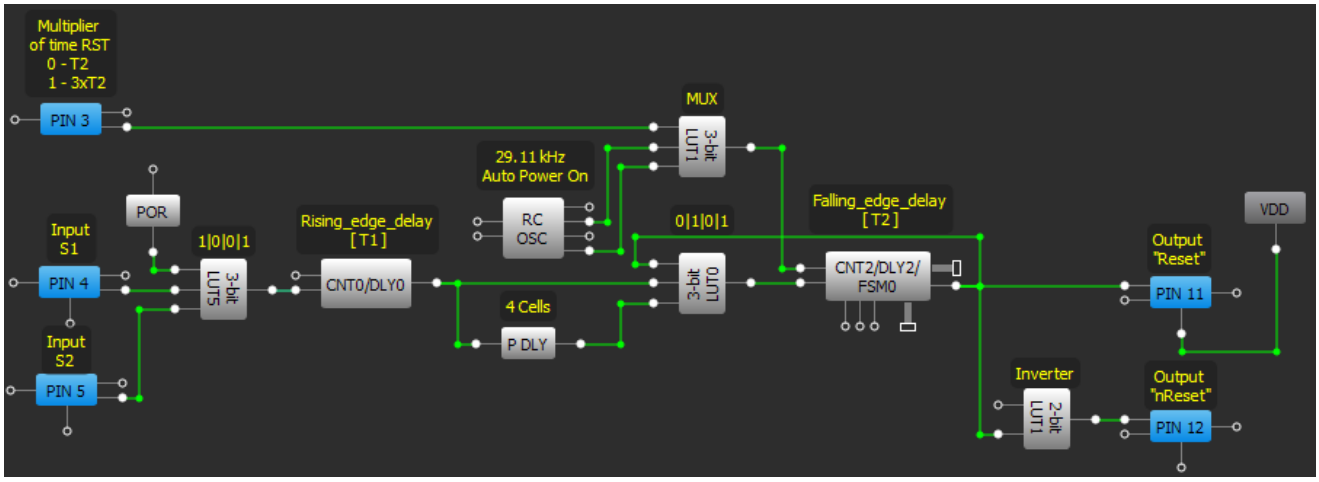


**Figure 6. 2-buttons Reset Circuit with configurable reset duration time**

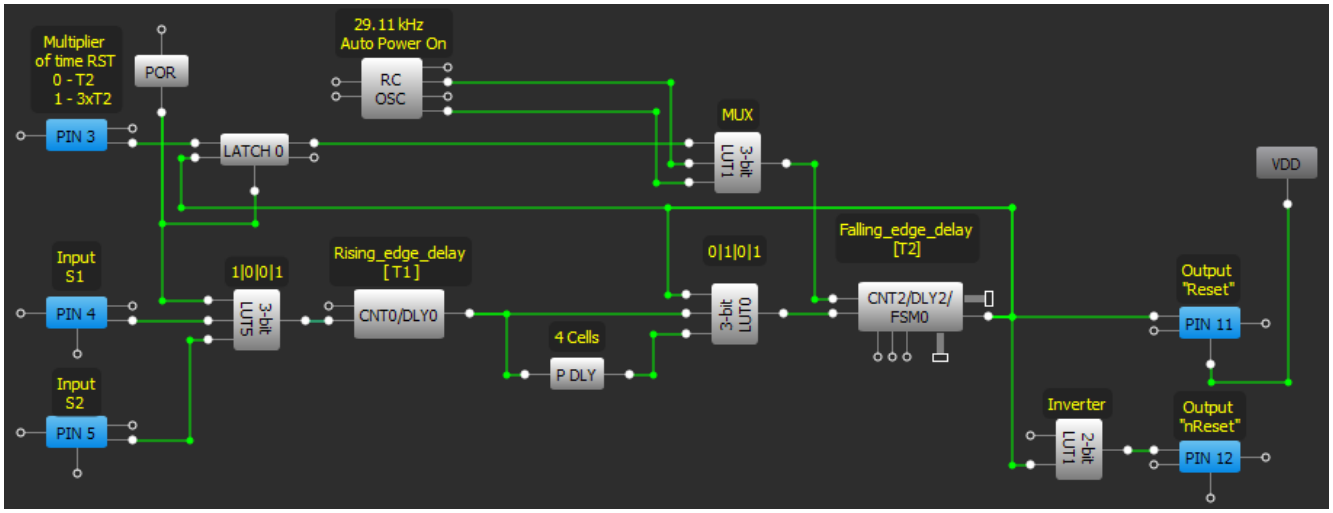


**Figure 7. 2-buttons Reset Circuit with configurable reset duration time (unchangeable division factor during RESET)**

The input PINs of the circuit shown in Figure 9 should be configured as follows (option “Mode – Digital input with Schmitt trigger” valid for all input PINs):

- PIN4/5 should be configured with the options “Resistor – Pull Up” , “Resistor value – 300k”
- PIN4/5 should be configured with the options “Resistor – Pull Down” , “Resistor value – Floating”
- PIN4/5 should be configured with the options “Resistor – Pull Down” , “Resistor value – Floating”
- PIN4/5 should be configured with the options “Resistor – Pull Down” , “Resistor value – 300k”
- PIN4/5 should be configured with the options “Resistor – Pull Up” , “Resistor value – 300k”, PIN3 should be in the option “Resistor – Pull Down” , “Resistor value – Floating’;
- PIN3/4/5/6 should be configured with the options “Resistor – Pull Up”, “Resistor value – 300k”.
- PIN11 should be configured as: “Mode – 1x push pull”, “Resistor – Pull Up”, “Resistor value – Floating”
- PIN12 should be configured as: “Mode – 1x open drain”, “Resistor – Pull Up”, “Resistor value – Floating”

| Vendor | Chip | Package | Extra PIN's (for additional user functionality) | Temperature Range | Times of "RESET" | Time to "RESET" |
|---|---|---|---|---|---|---|
| Silego | SLG46400 | 2.5mm×2.5mm TDFN-12 or WLCSP (1.3×1.9 mm) | 6* | -40°C to +85°C | 0.1 us-6.75s** | 0.1us-6.75s** |
| Texas Instruments | TPS3421 | 1.45mm×1mm SON | - | -40°C to +125°C | 400ms | 0s-7.5s |
| ST Micro-electronics | STM650x | 2mm×2mm TDFN8L | - | -40°C to +85°C | 140-480ms | 2/6/10s (min 10ms) |
| Fairchild Semiconductors | FT3001 | 1.4mm×1.8mm UMLP or 2mm×2mm MLP | - | -40°C to +85°C | 400ms | 2.4s-7.2s |
| Maxim | MAX6443/6444 | 2.8mm×1.4mm SOT143 | - | -40°C to +85°C | 140-210ms | 1.68/3.36/6.72/10.08s |
| Micrel | MIC2782 | 0.8mm×1.2mm WLCSP | - | -40°C to +85°C | 0.5/1/2s | 6/8/10/12s |

** - 2 PINs are used for power supply, 2 input PINs, 2 output PINs*

*** -Time can be increased. Please contact Silego.*

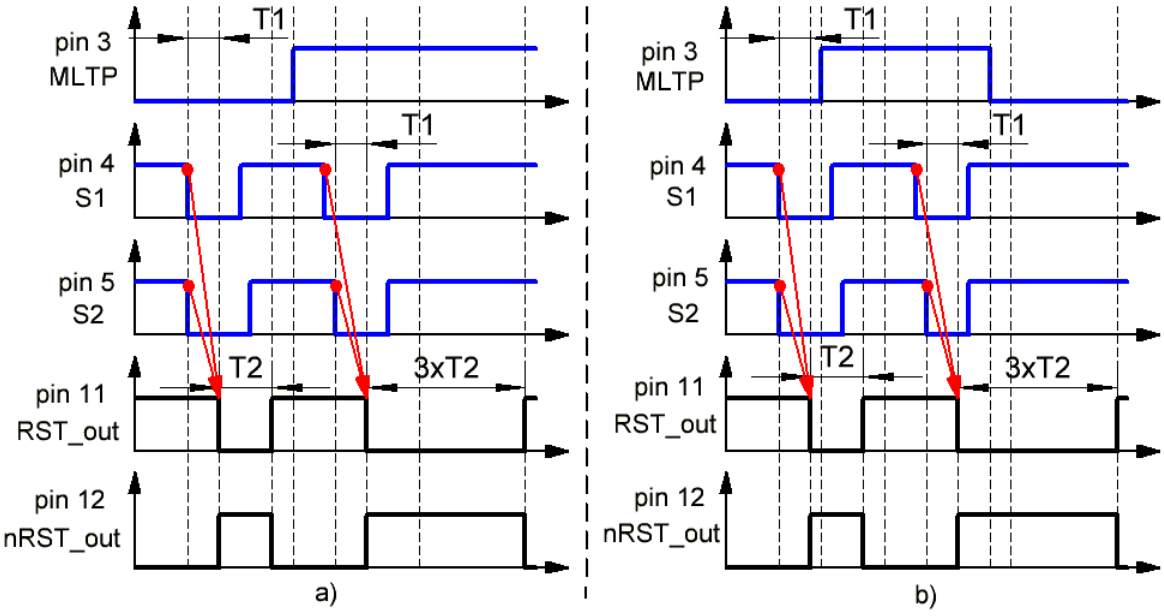


**Figure 8. Operation of the circuit shown in Figure 6 (left side - a) and 7 (right side - b)**

## Typical Application Circuits

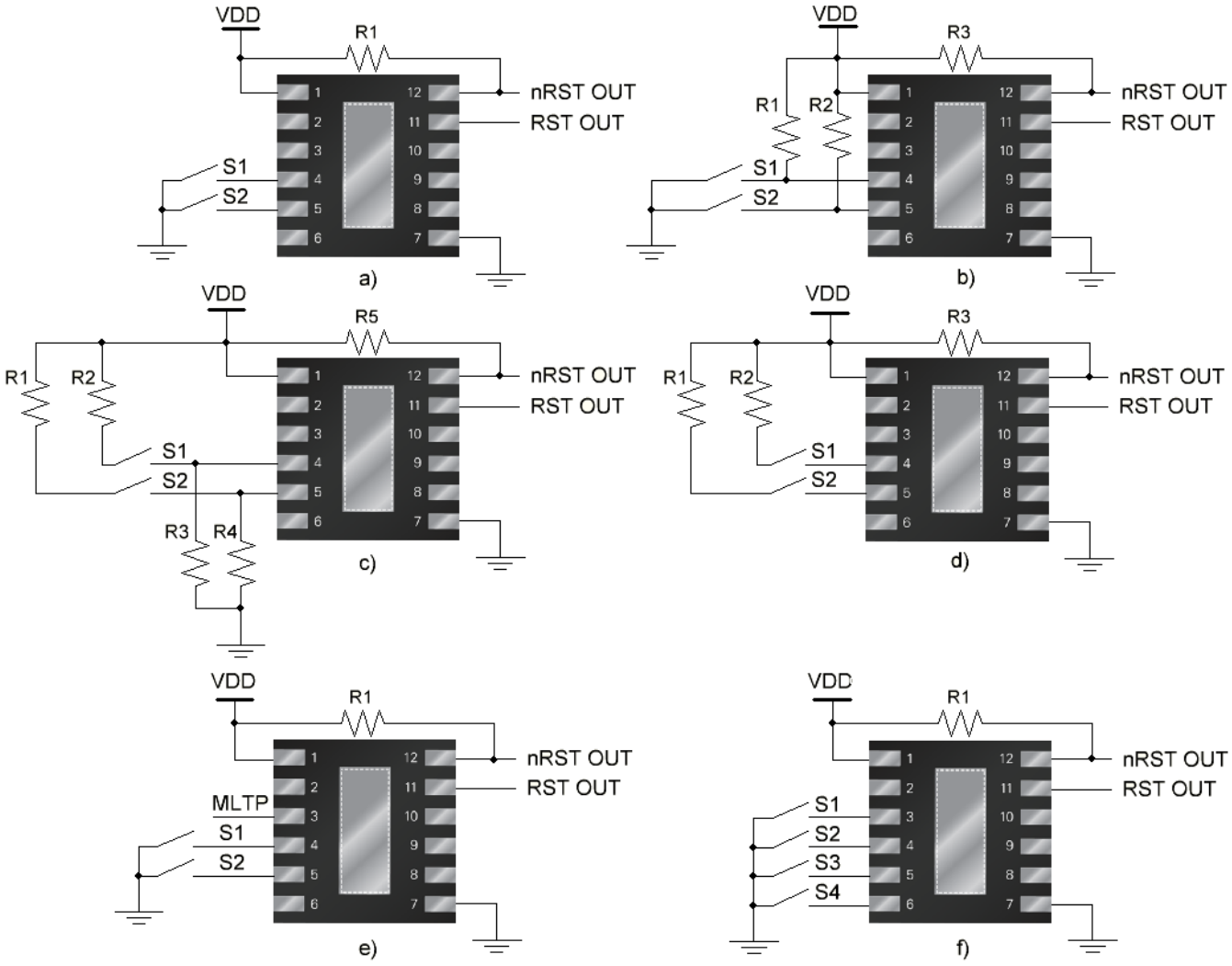


**Figure 9. Application Circuits for the SLG46400 chip in several versions a) with buttons connected to GND; b) with buttons connected to GND and external pull-up resistors; c) with buttons connected to pull up resistors and pull-down resistors; d) with buttons connected to external pull-up resistors; e) with RESET time configuration input; f) with four buttons**

## About the Author

Name: Olexander Reshotka

Background: Olexander Reshotka graduated from Lviv Polytechnic National University in 2012 and received a Master's Degree in "Micro- and nanoelectronics". Since 2012 he has been working with crystalline materials, measuring equipment, research acousto-optic interaction of the laser beam in crystalline materials. He has also practical skills in working with electronics, drafting circuit, making drawings of printed-circuit boards, repairing computer equipment, audio equipment.

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## Document History

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| Revision | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|
| A | Olexander Reshotka | 09/04/2013 | New application note |

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