



## Introduction

In this application the GreenPAK2 monitors the power on a load within the range (0.5W - 1.5W) by measuring the voltage and the current on the load. Two of the outputs drive indicator LED's to show the status.

In this design example, the voltage range to be monitored is between 3.5V - 5.5V. PIN4 is configured as Analog in, which takes its value from the output of the voltage divider Vx. ACMP0 & ACMP1 compare the value of the input against the desired limits derived from the voltage divider ratio.

We connect the analog input voltage Vx to PIN4 (configured as Analog In with floating resistor). Vx is calculated as shown using the external voltage divider circuit:

$$V_x = V_{DD} \frac{R_4}{R_4 + R_3}$$

When VDD = 3.5V then:

$$V_x = 3.5 \frac{100k\Omega}{100k\Omega + 400k\Omega}$$

Resulting Vx = 700mV

When VDD = 5.5V then:

$$V_x = 5.5 \frac{100k\Omega}{100k\Omega + 400k\Omega}$$

Resulting Vx = 1100mV.

The resulting level-shifted limits of 700mV and 1100mV are set as the IN- analog comparator references. ACMP0 is configured as 700mV with 12mV Hysteresis, and ACMP1 is configured as 1100mV with 12mV Hysteresis.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>THD</sub>	ACMP0 Voltage Threshold	694	-	706	mV
V <sub>THD</sub>	ACMP1 Voltage Threshold	1094	-	1106	mV
V <sub>AIR</sub>	ACMP Analog Input Voltage Range	0	-	1000	mV
V <sub>REF ADC</sub>	ADC Voltage Reference	-	1000	-	mV

Table 1. Design Main Electrical Characteristics



PIN 4	
Mode:	Analog in
Resistor:	Pull Down
Resistor value:	Floating
Initial state:	Output floating
OE:	From matrix

Figure 1. PIN 4 properties

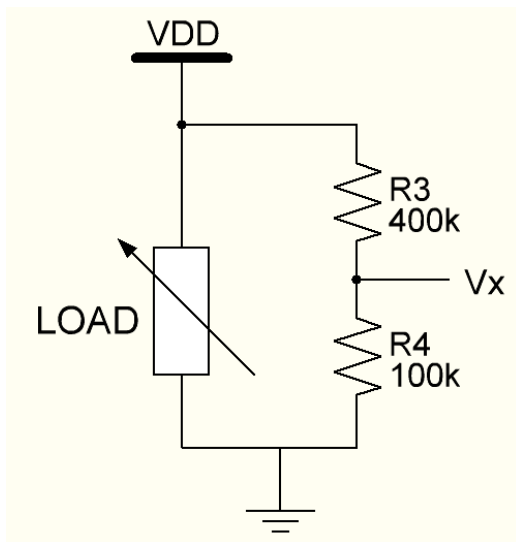


Figure 2. Circuit Design

2-bit LUT1		
IN1	IN0	OUT
0	0	0
0	1	1
1	0	0
1	1	0

Figure 3. 2-bit LUT1

A CMP0	
1uA pullup on input:	Disable
Hysteresis:	12 mV
Low bandwidth:	Disable
ACMP VREF Band:	50 mV - 1.5 V
IN- voltage:	700 mV
Connections	
A CMP0	
IN+ source:	PIN4 out

Figure 4. ACMP0 properties

A CMP1	
1uA pullup on input:	Disable
Hysteresis:	12 mV
Low bandwidth:	Disable
ACMP VREF Band:	50 mV - 1.5 V
IN- voltage:	1100 mV
Connections	
A CMP0	
IN+ source:	PIN4 out
A CMP1	
0.5 gain to IN+:	Disable (PIN4 out)
IN- source:	From 'IN- voltage'
DAC input source:	ADC

Figure 5. A CMP1 properties



Also, we use POR (configured as Auto power detect function on) for analog comparator power savings.

Connection of the POR block also ensures that the device wouldn't be influenced by external signals before all the blocks have powered up.

Next, the outputs of analog comparators go through LUT1 logic cell.

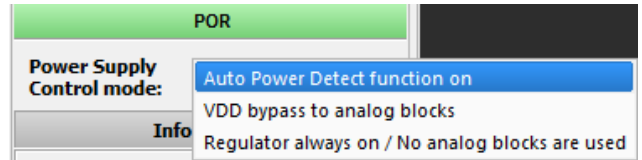


Figure 6. POR properties

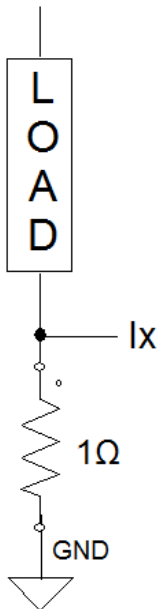


Figure 7. Circuit Design with PIN 8 configured as Analog In

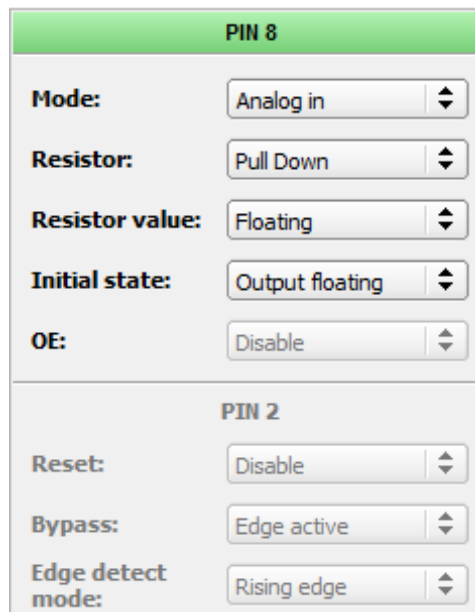


Figure 8. Pin 8 properties

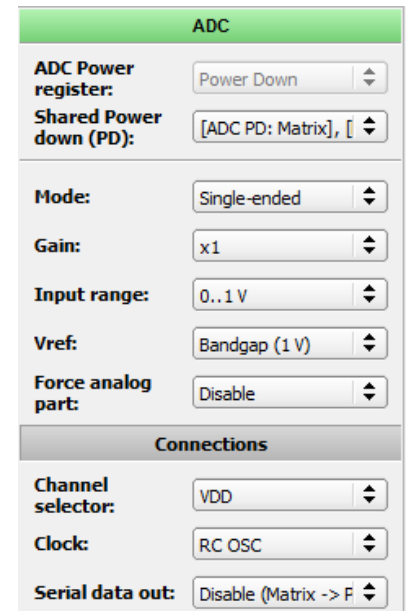


Figure 9. ADC properties

2-bit LUT2		
IN1	IN0	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Figure 10. 2-bit LUT2 properties

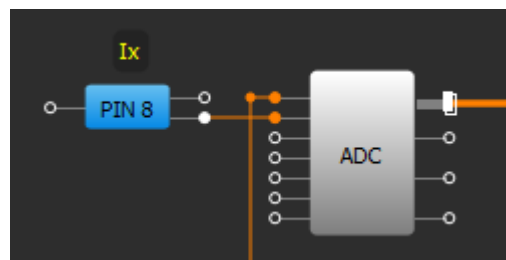


Figure 11. PIN 8 and ADC in GreenPAK2 Designer

2-bit LUT3		
IN1	IN0	OUT
0	0	0
0	1	1
1	0	0
1	1	0

Figure 12. 2-bit LUT3 properties



### Current Monitoring

The voltage range is between (3.5V - 5.5V), and the power range which we need to monitor is between (0.5W - 1.5W), so the resulting load current range is 140mA - 273mA. This current is detected by the ADC on the second channel named Ix (PIN 8: configured as Analog In with floating resistor).

DCMP0/PWM0 and DCMP1/PWM1 are used to compare the output of the ADC with the digital value that represents the threshold limits of current.

In this case:

$$I_{x_{min}} = \frac{36}{256} \times 1 = 140mV$$

$$I_{x_{max}} = \frac{70}{256} \times 1 = 273mV$$

Note that DCMP0/PWM0 IN- selector is from "Register 0", and DCMP1/PWM1 IN- selector is from "Register selected through matrix"

To indicate the required power range, we used two LEDs. One LED is Green indicating power within range of 0.5W - 1.5W, and the Red LED alerts power outside that range.

- PIN10 is an output pin which is configured as 1x Open Drain; it's connected to the Green LED.
- PIN5 is an output pin which is configured as 1x Open Drain; it's connected to the Red LED.

**DCMP0/PWM0**

DCMP/PWM Power register: Power On

Shared Power down (PD): [ADC PD: Matrix], [

Clock invert: Disable

Duty cycle: 0% - 99.6%

PWM Deadband time: 8 ns

Register 0: 36  
MTRX SEL: (0:0)

Register 1: 70  
MTRX SEL: (0:1)

Register 2: 0  
MTRX SEL: (1:0)

Register 3: 0  
MTRX SEL: (1:1)

**Connections**

IN+ selector: ADC [7:0]

IN- selector: Register 0

Figure 13. DCMP0/PWM0 properties

**DCMP1/PWM1**

DCMP/PWM Power register: Power On

Shared Power down (PD): [ADC PD: Matrix], [

Clock invert: Disable

Duty cycle: 0% - 99.6%

PWM Deadband time: 8 ns

Register 0: 36  
MTRX SEL: (0:0)

Register 1: 70  
MTRX SEL: (0:1)

Register 2: 0  
MTRX SEL: (1:0)

Register 3: 0  
MTRX SEL: (1:1)

**Connections**

IN+ selector: ADC [7:0]

IN- selector: Register selected th

Figure 14. DCMP1/PWM1 properties

**PIN 5**

Mode: 1x open drain

Resistor: Pull Down

Resistor value: Floating

Initial state: Output floating

**PIN 10**

Mode: 1x open drain

Resistor: Pull Down

Resistor value: Floating

Initial state: Output floating

Figure 15. Pin 5 and PIN 10 properties

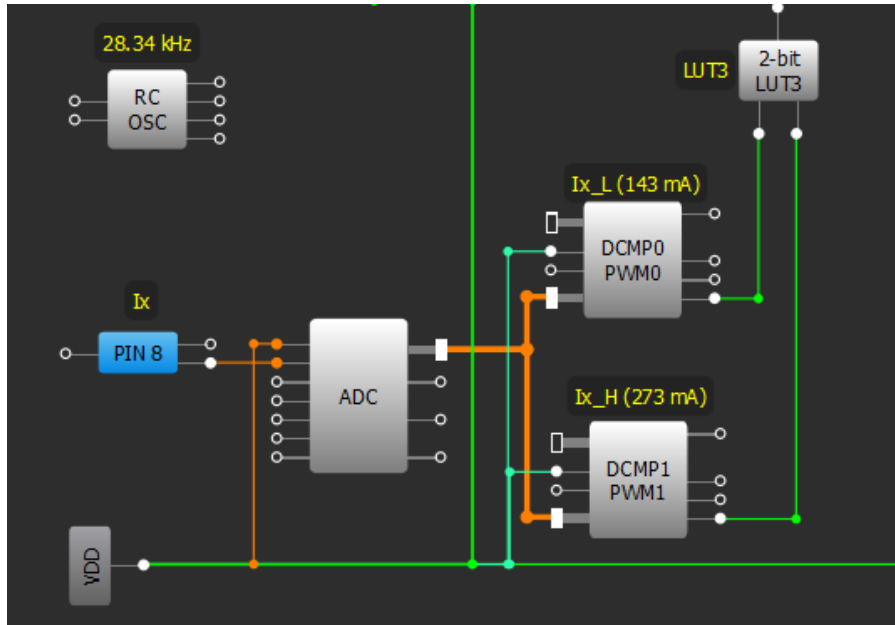


Figure 16. Design connections in GreenPAK2 Designer

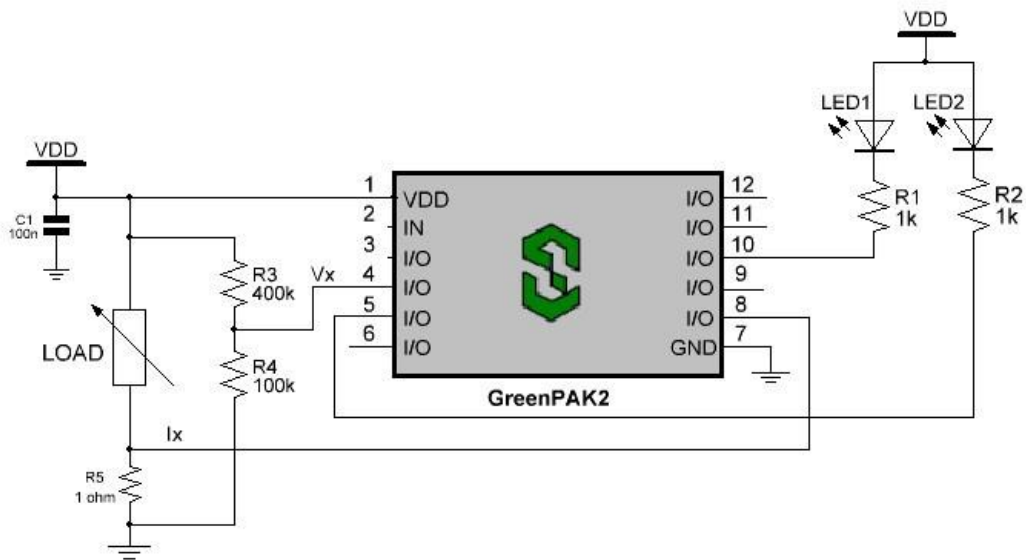
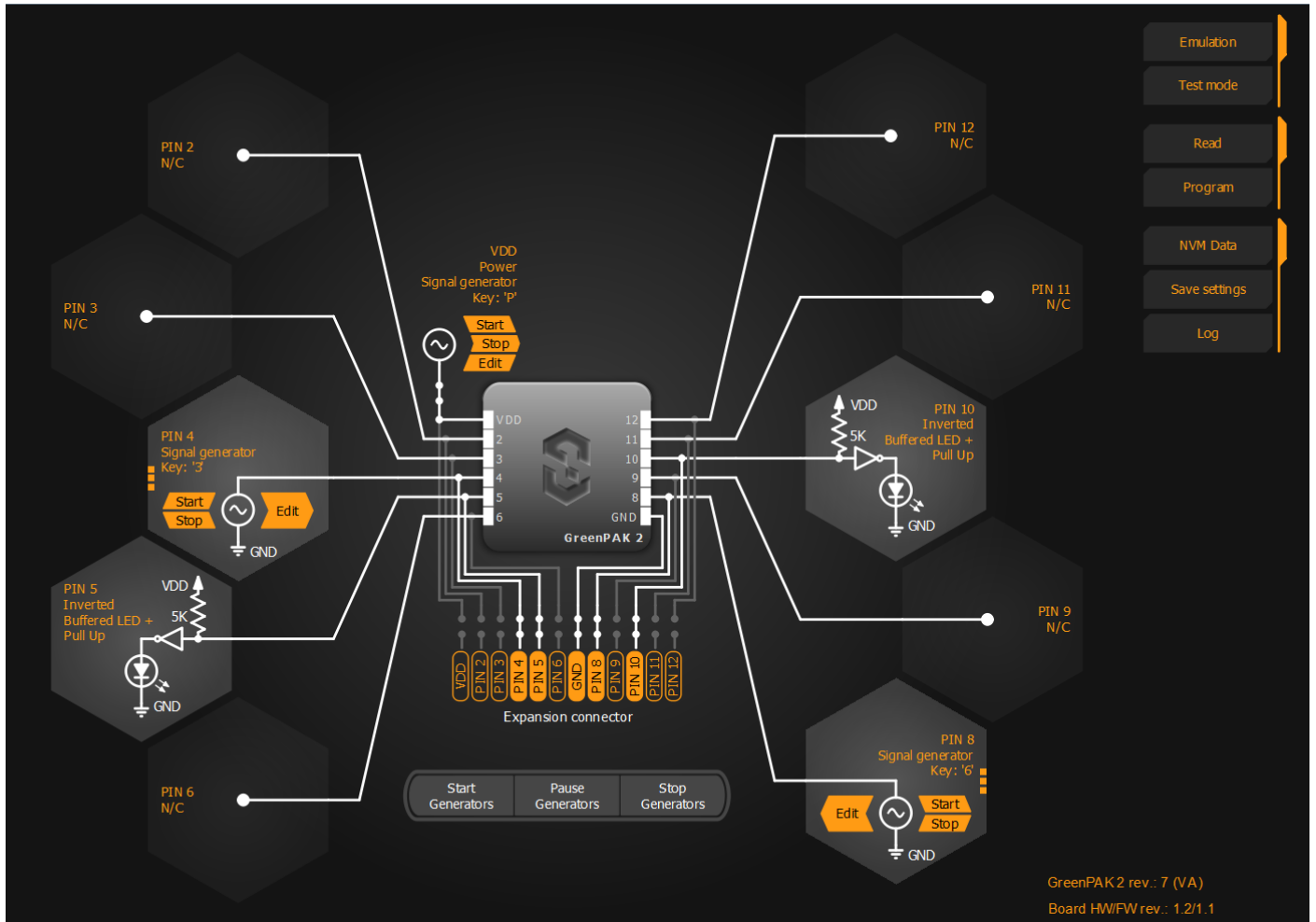


Figure 17. Typical Application Circuit



**Figure 18. Configuration in GreenPAK2 Emulation Tool**

*Note: For proper operation of circuit, do not forget to correctly configure input and output pins. In case of schematic you see on Figure 16, PIN4 and PIN8 configured as analog input, the output PIN5 and PIN10 are configured as open drain.*

*For testing purposes, a custom Input Signal from PIN4 and PIN8 are generated using Signal Wizard in GreenPAK2 emulation tool. As you can see in Figure 19 and Figure 20.*



### Functionality Waveforms

Generated signal from signal generator as the Input Signal from PIN4 (Vx).  
Generated signal from signal generator as the input signal to PIN 8 (Ix).

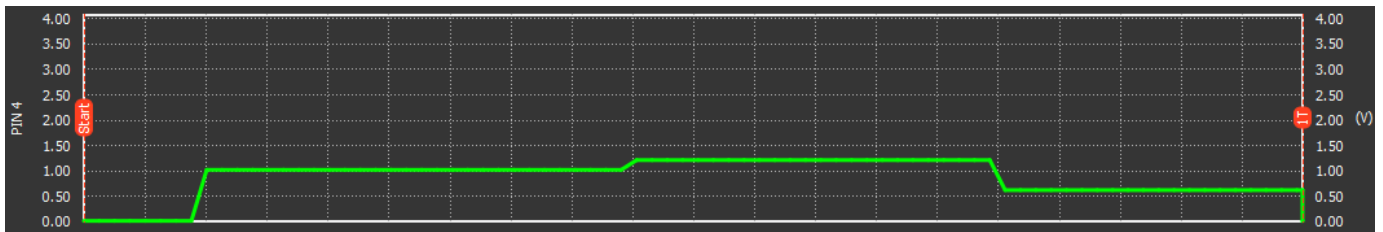


Figure 19. PIN 4 Signal Diagram

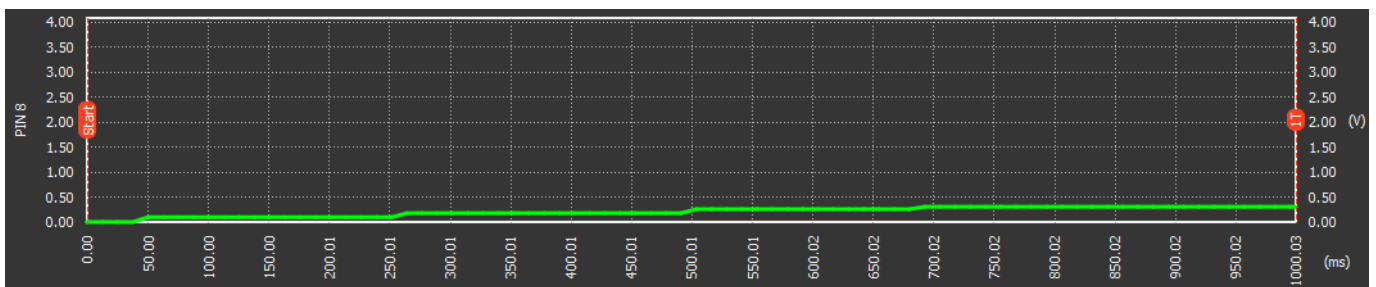


Figure 20. PIN 8 Signal Diagram

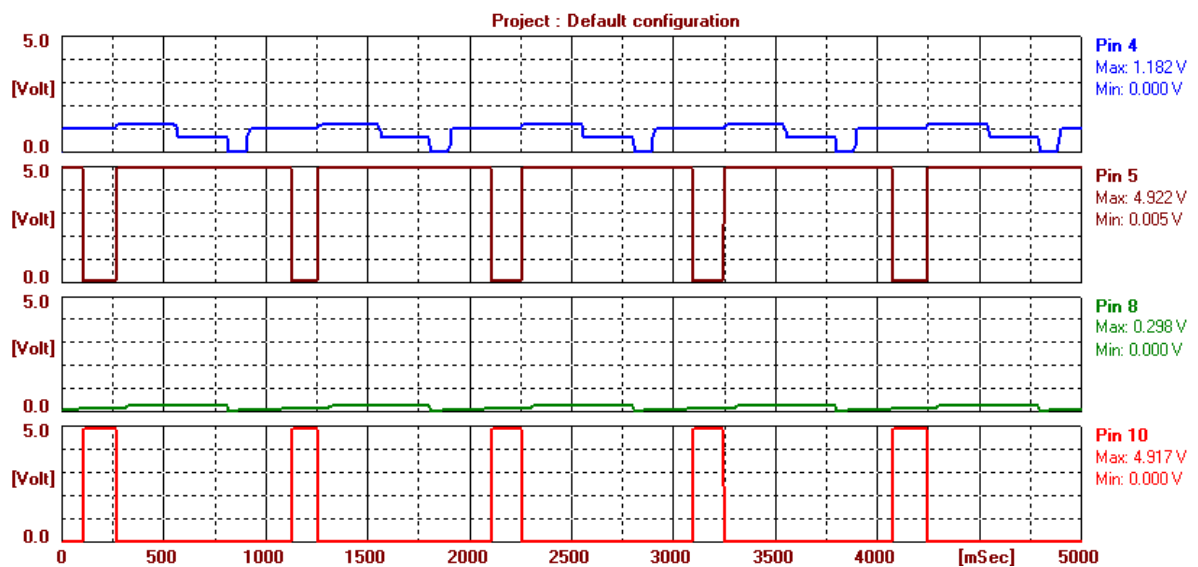


Figure 21. Timing diagram



### Conclusion

The GreenPAK2 product can be configured to measure the current and voltage for a specified load, and then indicate corresponding power limits. For more sensitive applications, variants of this circuit can be constructed using monitoring resistors lower than 1 ohm.

Functionality waveforms of this Load Monitor circuit created in GreenPAK2 Designer are shown in Figure 21. Where Channel1 (blue/top line) – PIN4 (Vx), Channel2 (brown/2<sup>nd</sup> line) – PIN5 (Red\_LED), Channel3 (green/3<sup>rd</sup> line) – PIN8 (Ix), Channel4 (red/bottom line) – PIN10 (Green\_LED).





### About the Author

Name: Ahmad Al Shari

Background: Ahmad Al Shari graduated from Jordan University of Science and Technology -Jordan in 2013, studying at the Department of Electrical Power Engineering. Presently he is working with Configurable Mixed Signal ICs (CMICs) and their application notes. At the moment he is an employee at Core Nano Technology-Jordan.

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A	Ahmad Al Shari	3/20/2014	New application note

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