

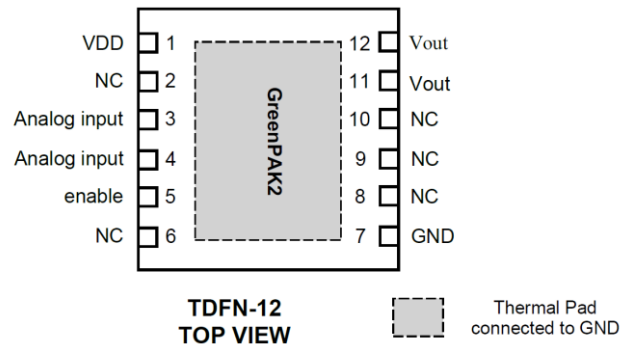
## Introduction

Many applications require a controlled cycle during power-up and power-down.

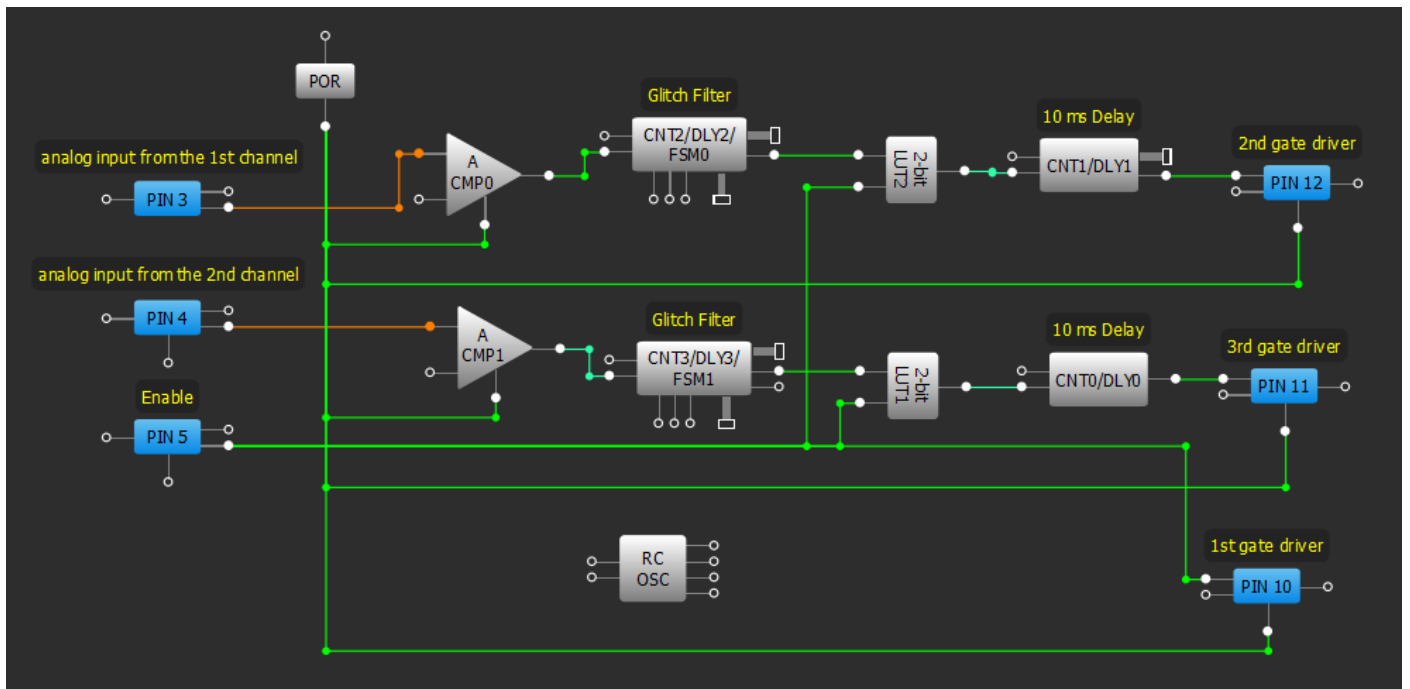
The GreenPAK2 controls the starting time of each of 3 power rails, and the shutdown time.

## Description

Pins 3, 4 each have an internal 300KΩ resistor, and 300KΩ external resistors in the schematic to make a voltage divider at the analog inputs to the analog comparators. The circuit then determines if the previous channel got started up based on the voltage, and whether to start the next channel. (outputs at pins 10, 11, 12).



**Figure 1. Pin configuration**



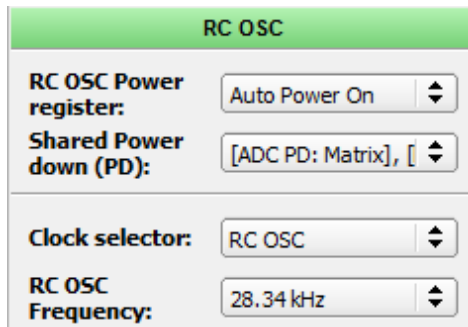
**Figure 2. Design connections in GreenPAK2 Designer**



The enable switch starts the circuit by pin 5, and drives the 1st channel signal through pin 10, and on to a loadswitch (SLG59M301V).

The loadswitches used in this design are Silego GreenFETs. They have integrated MOSFETs, short/thermal protection, and slew rate control based on capacitors C2, C3, C4.

In this example, the RC OSC is set to be always ON by choosing the option Force Power On, and it will provide a 28.34 KHz clock frequency.



**Figure 3. RC OSC properties**

The ACMP0 and ACMP1 properties are set as 600mV reference voltage to make delay equal to the input ramp time reaching the 600mV x 2 (because of the 300K external resistor voltage dividers). Also, the Hysteresis is set to 50 mV to reduce effect of input glitches.

POR is used to remove any ACMP glitch during powerup. ACMP0 is configured to auto power detect.



**Figure 4. POR properties**

Pins 3, 4 are configured as analog inputs with floating pull down resistor. Pin 5 is configured as digital input with 300k pull down resistor (figure 7)

The pins 10, 11, 12 are configured as 1X push pull with floating pull down resistor (figure 8).

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>THD</sub>	ACMP0 Voltage Threshold	575	-	625	mV
V <sub>THD</sub>	ACMP1 Voltage Threshold	575	-	625	mV
V <sub>AIR</sub>	ACMP Analog Input Voltage Range	0	-	1000	mV
T <sub>DLY0</sub>	DLY0 Time Delay	-	10.0917	-	ms
T <sub>DLY1</sub>	DLY1 Time Delay	-	10.0917	-	ms
T <sub>DLY2</sub>	DLY2 Time Delay	-	0.1059	-	ms
T <sub>DLY3</sub>	DLY3 Time Delay	-	0.1059	-	ms

**Table 1. Design Main Electrical Characteristics**



A CMP0	
1uA pullup on input:	Disable
Hysteresis:	50 mV
Low bandwidth:	Disable
ACMP VREF Band:	30 mV - 1 V
IN- voltage:	600 mV
Connections	
A CMP0	
IN+ source:	PIN3 out

Figure 5. A CMP0 properties

Signal Generator Settings	
Type:	Trapeze (Triangle, S
Mode:	Normal
Umax:	4.08 V
Umin:	0.00 V
T1:	300.00 ms
T2:	50.10 ms
T3:	800.00 ms
T4:	50.10 ms

Figure 6. Signal Generator Settings

PIN 3	
Mode:	Analog in
Resistor:	Pull Down
Resistor value:	Floating
Initial state:	Output floating
OE:	Disable

PIN 4	
Mode:	Analog in
Resistor:	Pull Down
Resistor value:	Floating
Initial state:	Output floating
OE:	From matrix

PIN 5	
Mode:	Digital in without Sc
Resistor:	Pull Down
Resistor value:	300K
Initial state:	Output floating
OE:	From matrix

Figure 7. PIN 3, PIN 4 and PIN 5 properties

PIN 10	
Mode:	1x push pull
Resistor:	Pull Down
Resistor value:	Floating
Initial state:	Output floating
OE:	From matrix

PIN 11	
Mode:	1x push pull
Resistor:	Pull Down
Resistor value:	Floating
Initial state:	Output floating
OE:	From matrix

PIN 12	
Mode:	1x push pull
Resistor:	Pull Down
Resistor value:	Floating
Initial state:	Output floating
OE:	From matrix

Figure 8. PIN 10, PIN 11 and PIN 12 properties

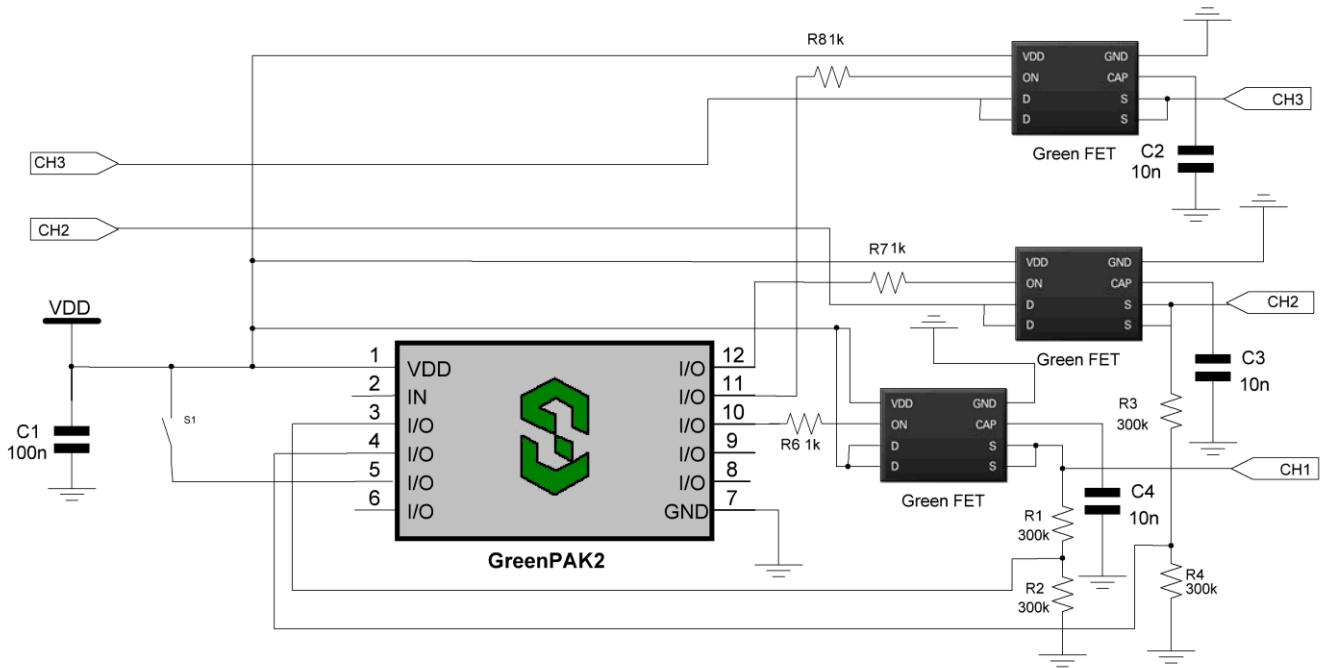


Figure 9. Typical Application Circuit

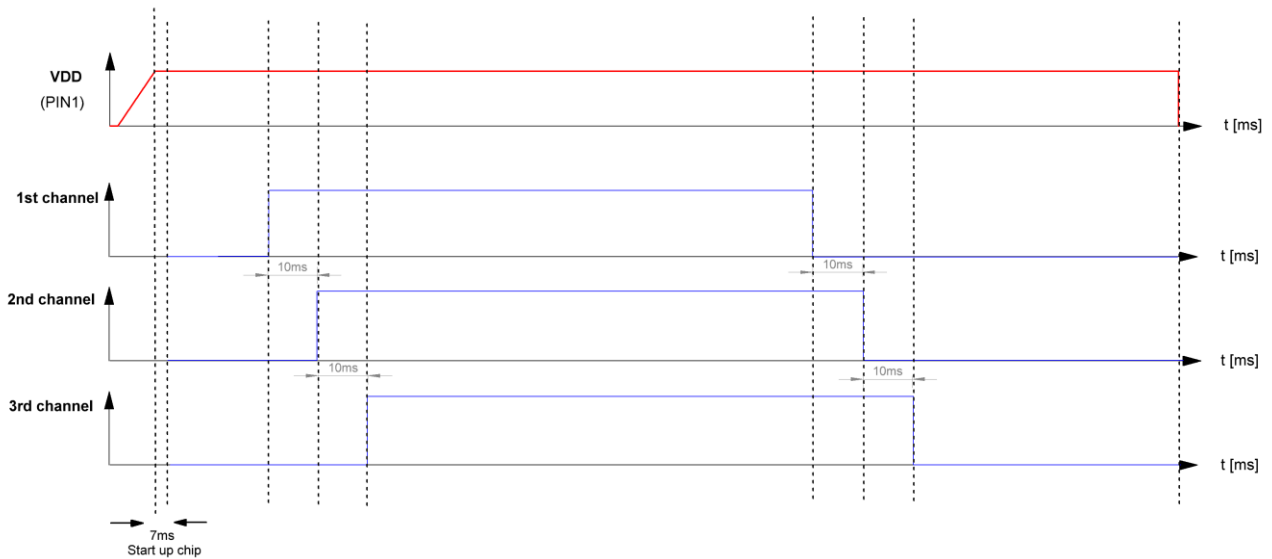


Figure 10. Timing Diagram

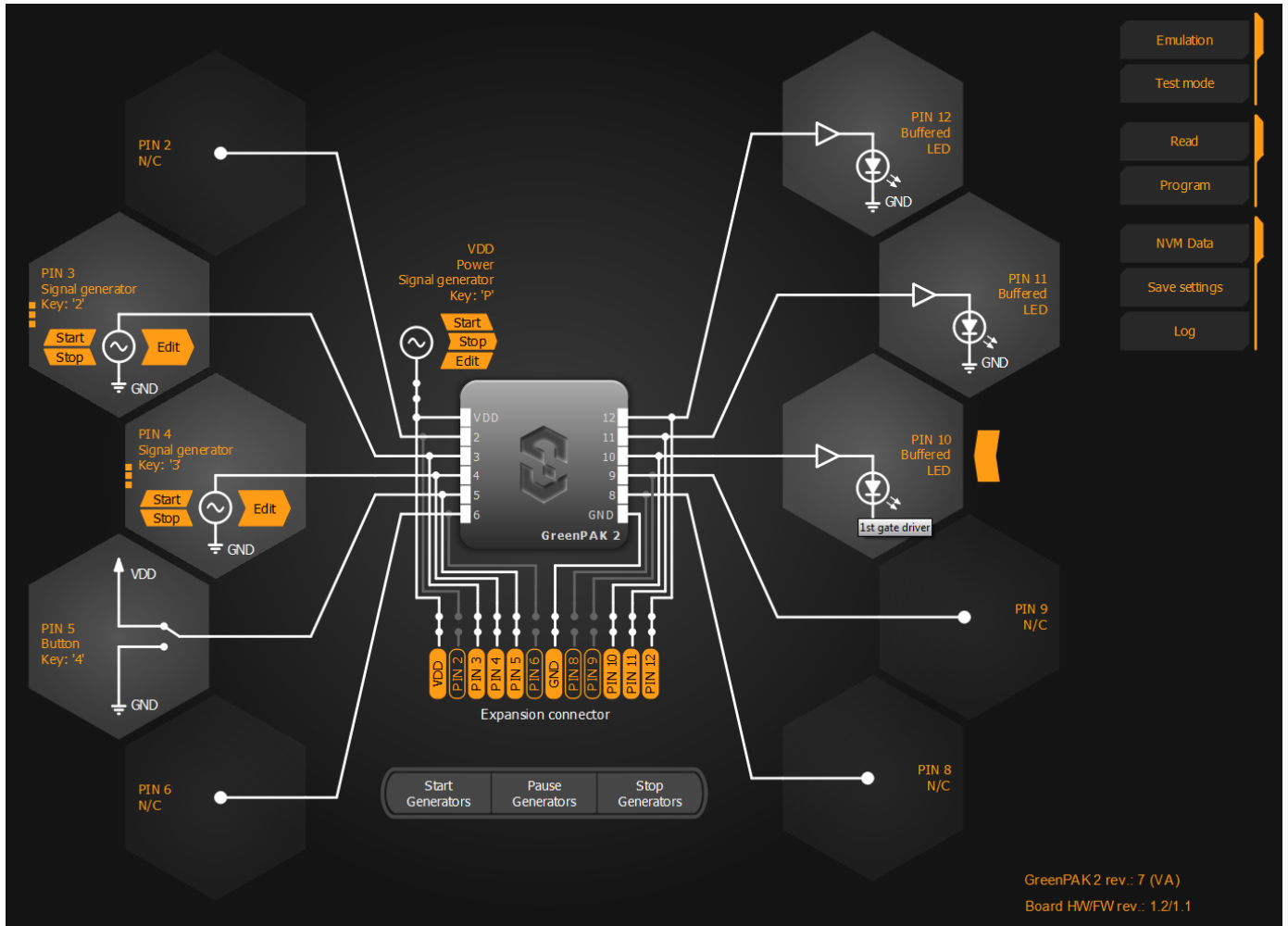


Figure 11. GreenPAK2 Emulation Tool

## Conclusion

A GreenPAK2 was configured to control the power sequence of several power rails. This is useful for power management or system control considerations.



### About the Author

Name: Saif Abu Baker

Background: Saif Abu Baker graduated from Yarmouk University in 2013, studying at the Department of Electrical Power Engineering. Presently he is working with Configurable Mixed Signal ICs (CMICs) and their application notes and power supplies designing.

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### Document History

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Revision	Orig. of Change	Submission Date	Description of Change
A	Saif Abu Baker	3/26/2014	New application note

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