GreenPAK Macro Circuit Design: Delay cell configuration with auto powerdown

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Introduction

Using a counter is a good method to create long time delays. However, delay times are often too limited because counter data may not be large enough. GreenPAK solves this by providing large configurable counters. This note describes the behavioral differences among the GreenPAK chips, and the suggested circuit configuration. This is particularly important to preserve the accompanying RC OSC powerdown feature for power savings.

SLG46400 and SLG46200 chip delay circuit configuration

As can be seen in Figure 1, PIN3 (DLY_IN) is connected to IN0 of 2-bit LUT1, configured as an AND gate with POR on its IN1 input.

This ensures a known CNT2/DLY2/FSM0 initial powerup and startup state. CNT1/DLY1 cell is configured as a counter, with its output connected to clock input of CNT2/DLY2/FSM0 delay cell. The DELAY_CELL output is connected to PIN12 (DLY_OUT). For clarity, RC_OSC output test point (RC_OSC_OUT) is on PIN4, while POR test point (POR_OUT) is on PIN5.

SLG46400 chip delay circuit behavior

RC_OSC is configured as Auto Power On in the properties menu and is actually triggered ON by the DLY IN signal of CNT2/DLY2. After chip powerup, the POR signal goes HIGH and allows 2-bit LUT1 an input signal (DLY IN) HIGH level to propagate.

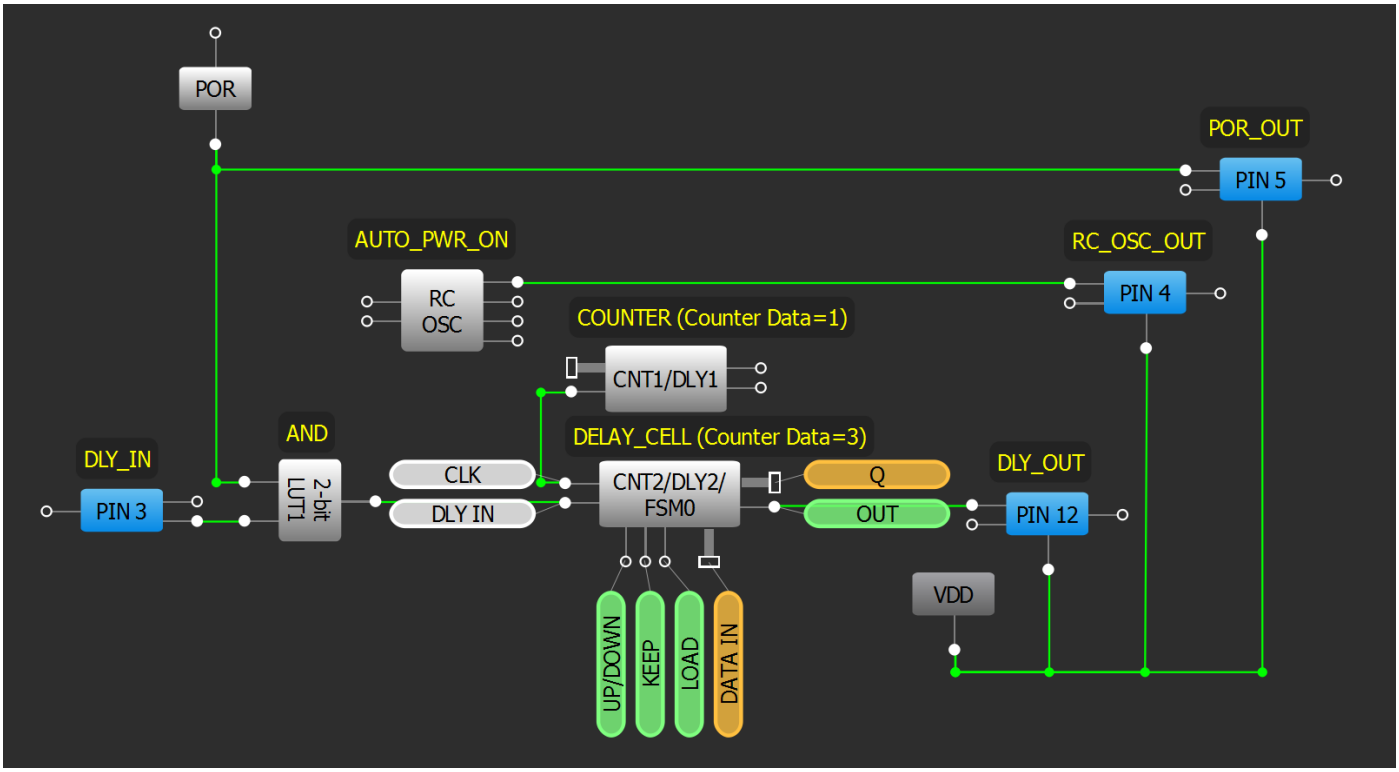

Figure 1. Proper connection of CNT2/DLY2/FSM0 configured as delay cell and CNT1/DLY1 configured as counter in SLG46400 chip

This first rising edge signal will be the one that triggers the RC _OSC to turn ON. Then the RC OSC output is divided by CNT1/DLY1 cell and becomes the input clock for CNT2/DLY2 delay cell. Figure 2 timing diagram illustrates how RC_OSC runs only during the delay cell counting, and then turns off. This is normal powerdown operation for power savings.

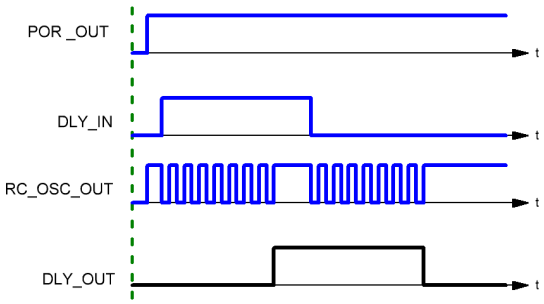

Figure 2. Delay cell Timing Diagrams

PAK3 chip family delay circuit configuration

Figure 3 shows the PAK3 chip family (SLG46721, SLG46722, SLG46110, SLG46120) circuit schematic. The main difference between SLG46400/SLG46200 chip circuit design and PAK3 family is that for proper powerdown operation, CNT2/DLY2 cell should be configured as a counter with external clock. Also its clock input should be manually connected to the RC_OSC output. If configured otherwise, RC_OSC will always run, even when set to Auto Power On mode, as illustrated in Figure 4.

Functionality waveform of real circuit created in GreenPAK2 Designer is shown in Figure 5, where Channel1 (yellow/top line) – PIN5 (POR_OUT), Channel2 (light blue/2nd line) – PIN3 (DLY_IN), Channel3 (magenta/3rd line) – PIN4 (RC_OSC_OUT) Channel4 (blue/bottom line) – PIN12 (DLY_OUT).

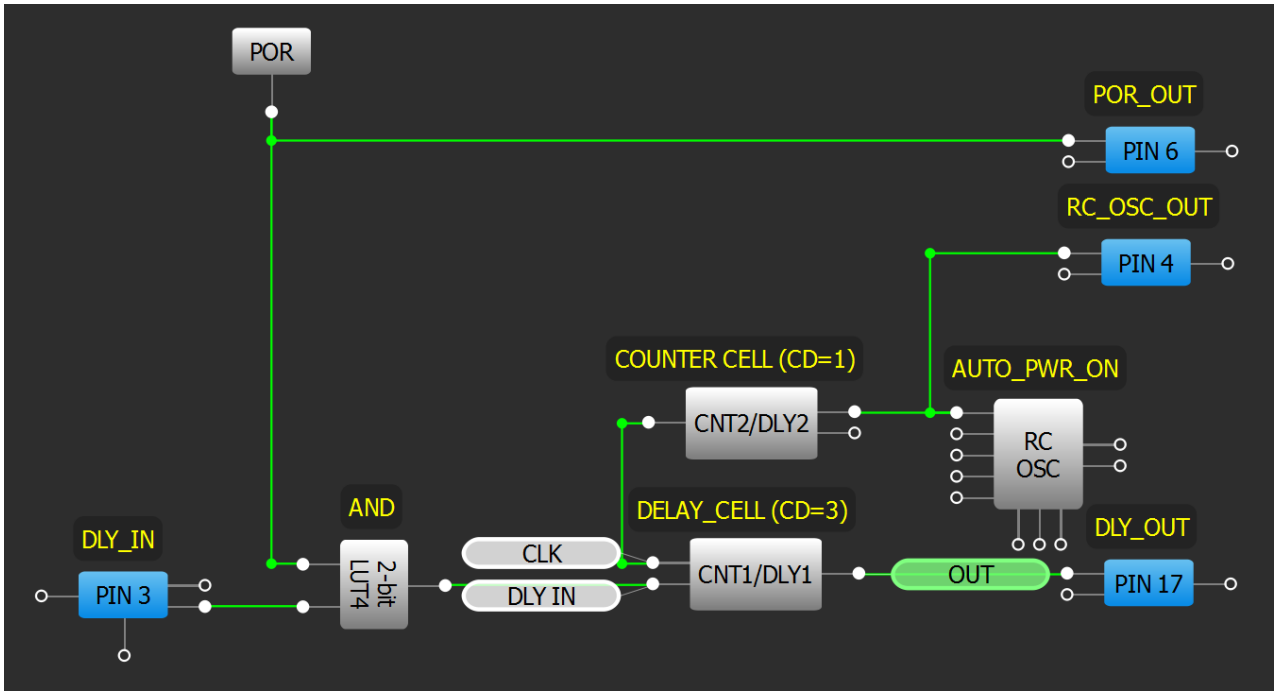

Figure 3. Proper connection of CNT1/DLY1 configured as delay cell and CNT2/DLY2 configured as counter in PAK3 chip family

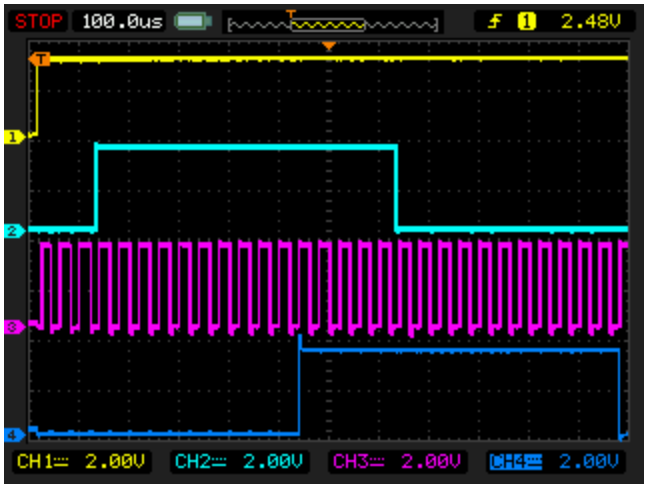

Figure 4. PAK3 delay cell showing RC_OSC continuously running

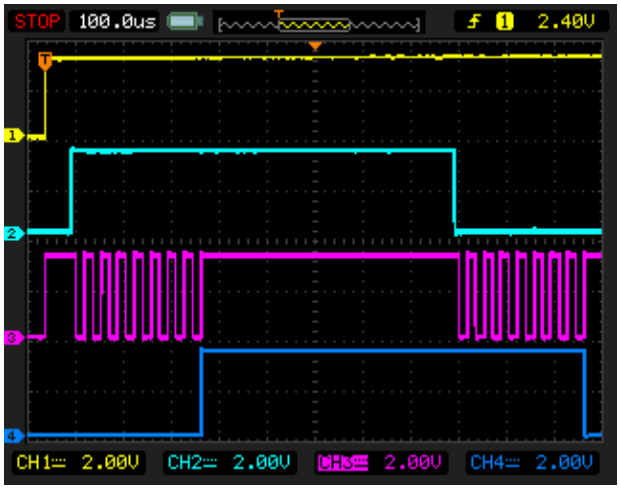

Figure 5. PAK3 delay cell properly configured for auto powerdown

As can be seen in Figure 5, the real waveforms coincide with the theoretical shown in Figure 2.

Note: For proper operation of circuit, don't forget to configure input and output pins correctly. In case of schematics you see in Figure 1 and Figure 3, inputs are configured as digital input without Schmitt trigger, and outputs as push-pull.

Conclusion

Full functionality and operation of RCOSC powerdown feature can be preserved among the variants of the PAK family of products. This in turn preserves the power saving benefits.

Related Files

Programming code for **GreenPAK Designer**.

About the Author

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Background: Volodymyr Batig graduated from Ivan Franko Lviv National University in 2012, studying at the Department of Medical and Biomedical Electronics. Presently he's working with Configurable Mixed Signal ICs (CMICs) and their application notes. Moreover, for more than 10 years his particular sphere of interest has included design, modernization and repair of everything related to electronics.

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Document History

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A	Volodymyr Batig	05/27/2014	New application note

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