Single input security passcode entry

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Example circuit application

A passcode entry circuit is constructed without the use of any switches, touch displays, or keypads. In this example the input uses an earbud, which also has properties of a microphone. Almost any microphone or speaker can be used in a similar fashion.

When the earbud is tapped, it generates a small output pulse which is amplified by an analog comparator in the GPAK2 IC. This also initiates a string of clock pulses inside the GPAK2. Each tap gets latched as a logic “one”, while the absence of a tap gets latched as a logic “zero”.

Not only does the pattern need to be correct, but also the “beat”, or timing must match as well. In other words, this circuit detects a “secret knock”.

Both the pattern and timing are user configurable. The circuit to perform this must be capable of serial input pattern and timing recognition.

Circuit operation summary:

1. On-chip analog comparator converts small analog signal inputs to full CMOS levels.

2. First input of a pattern (chosen always as 1) triggers the clock count sequence.

3. Successive bit positions are latched according to a user preconfigured clock period. A train of 16 clock pulses is started synchronous from that first input pulse. Only the first 8 bit positions are used to interpret the data.

4. Incoming data bits are latched into a serial to parallel converter (S2P).

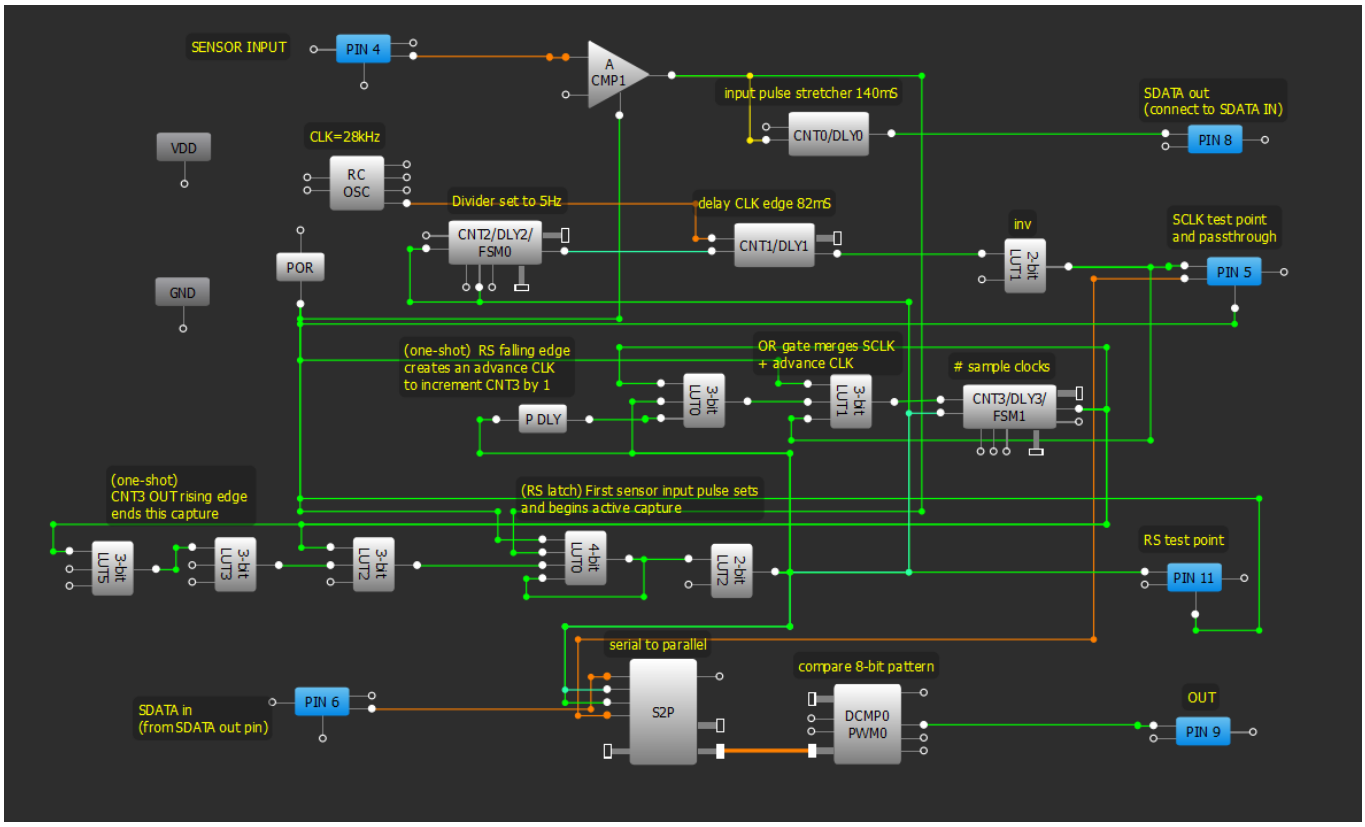

Figure 1. Complete PAK2 schematic

5. A digital comparator compares the completed S2P against the desired pattern (stored as a binary equivalent in a register).

6. If the results match, OUT pin goes high.

7. Any mismatched input will set OUT pin low.

8. The RS latch then goes HI, preparing the circuit for the next input train.

Circuit detail

An earbud is used as a transducer input. Since the signal generated is somewhat small, PIN4 is configured as analog input. Then the corresponding comparator (ACMP1) input threshold is set to 70mV. That setting seemed to be about right for this earbud, requiring definitive knocks (finger taps on the outside case). With this small a signal, it is necessary to ensure that the earbud cable has a shield to GND to minimize extraneous noise.

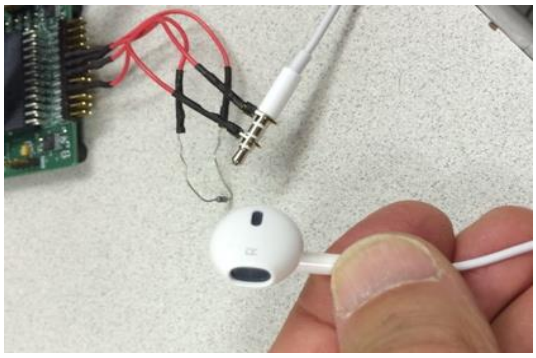

Figure 2. Earbud example input

Once the first input pulse is detected, it sets the 4-bit LUT0 latch RS to LOW. That in turn will trigger a one-shot 3-bit LUT0 to advance the CLK counter CNT3 by one.

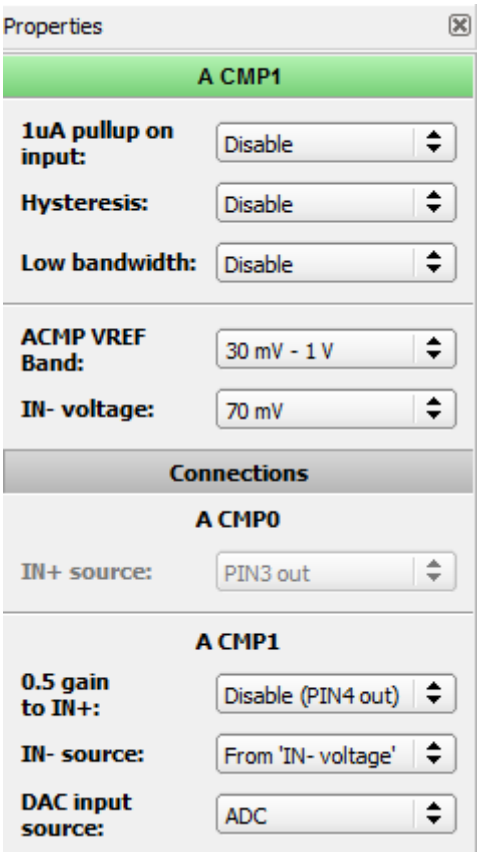

Figure 3. ACMP1 configuration

This is necessary so that the CNT3 will have its' output count set to the zero state. 3-bit LUT1 is an OR gate so that it can pass either the one-shot or the sampling clocks from CNT2 which are divided down from the RCOSC. This then becomes a merged CLK as shown in Figure 4.

It is the CNT2 that determines the timing setting. In this example, that happens to be approx. 5Hz. Once RS has been set LOW, CNT3 will keep counting until 16 SCLK pulses have been generated, and then 3-bit LUT2 one-shot will reset RS latch to HIGH.

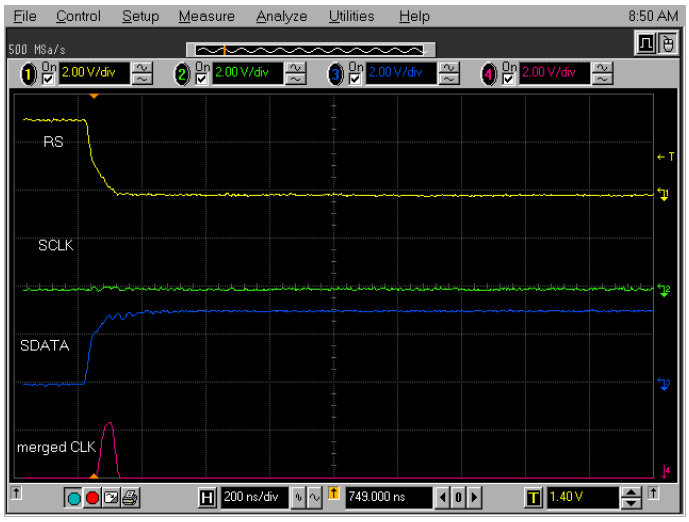

Figure 4. Merged CLK

That stops the entire train of CLK pulses, resets the counters, and prepares for the next possible input pulse train. Simply put, the RS latch and the CNT3 counter comprise a monostable circuit that is triggered by an input signal. The effect of the 3-bit LUT2 one-shot is shown in Figure 5.

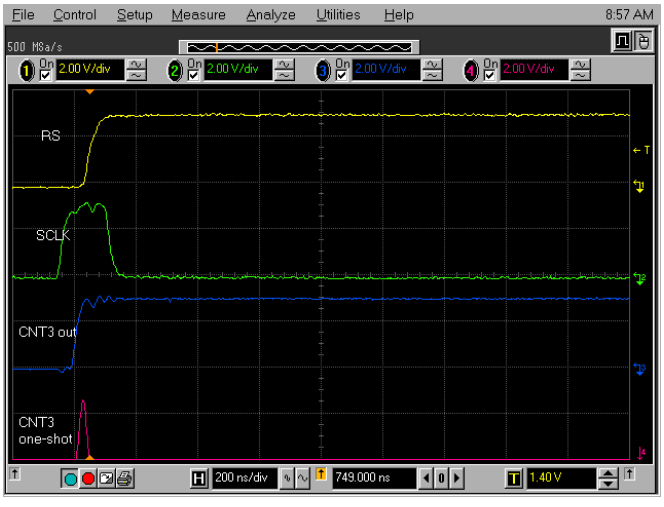

Figure 5. One-shot from CNT3 that resets RS

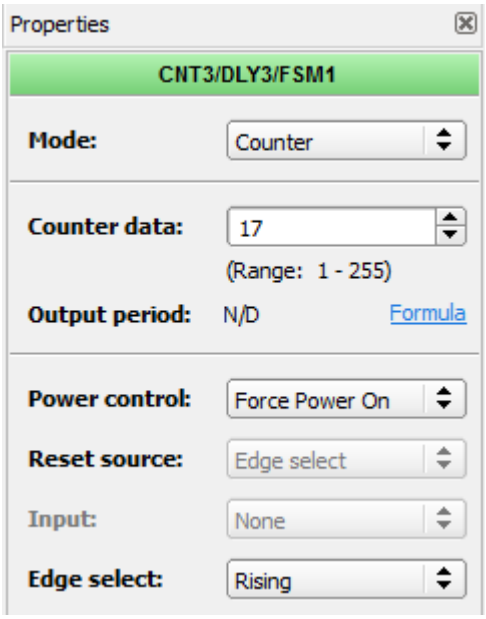

Figure 6. CNT3 setting

CNT0 is configured as a delay and is triggered at the falling (trailing) edge of the ACMP0. It acts as a pulse stretcher and produces SDATAout. CNT1 is configured as a delay for centering of the sample clock around the stretched input pulses. SCLK then latches the SDATA into the S2P, and also increments CNT3. 16 pulses are the minimum required for the S2P conversion, and then the updated output goes to the digital comparator DCMP0. The comparison “equal” result is then presented to the OUT pin9.

The configurable pattern chosen in this example is 10101110 , which must start with a 1.

This timing was also easy for this user to remember because it has the cadence of a dance step: cha---cha---cha-cha-cha. Conversion to decimal equals 174 and is stored in register 0 of the DCMP0 as shown in Figure 7.

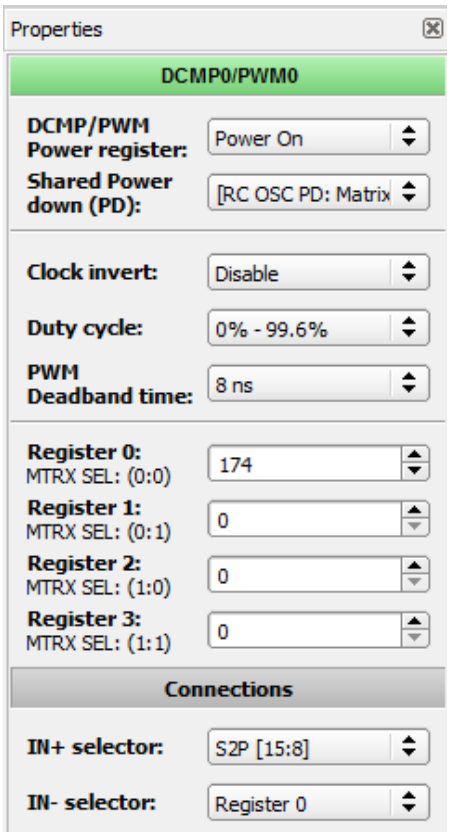

Figure 7. DCMP0 setting

The oscilloscope waveforms are shown in Figure 8. Note that the extra SDATA “ones” after the first 8 SCLK’s are ignored. It is possible to connect another DCMP to check for all 16 places, but it was deemed too difficult for an average user to time an input train that precisely.

To reset the OUT pin state to low requires another 16CLK pulse train to change the S2P output. This is shown in Figure 9.

Note that SDATAout PIN5 travels outside the chip through a 10k ohm resistor and then back into SDATAin PIN6. Two pins were necessary because there was no internal connection from CNT0 to S2P available in PAK2. It was designed only for external connections to S2P using pins 5,6. Similarly, SCLK must drive the S2P through PIN5, but PIN5 can be set as input and output as the same time so we don’t use up another external pin.

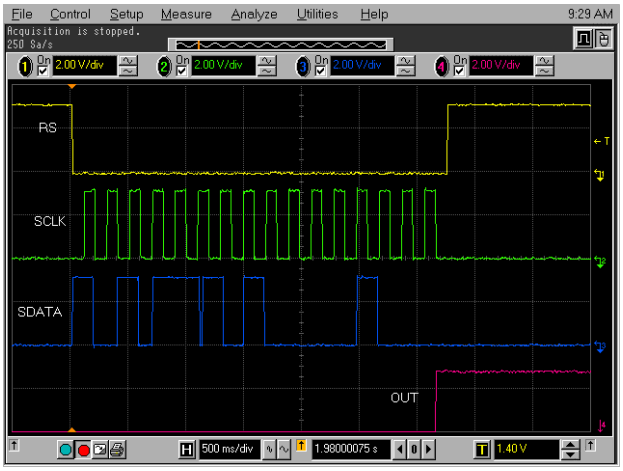

Figure 8. Waveforms of a match condition

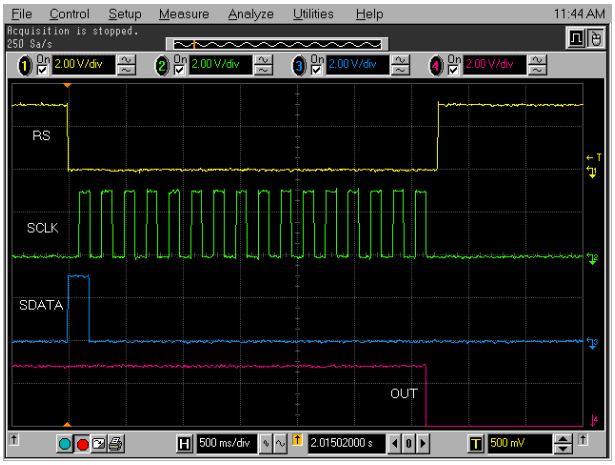

Figure 9. Any un-match condition resets OUT low

Conclusion

This circuit performs single input pattern and timing recognition. It was shown that an asynchronous bit stream can be captured and compared to a predetermined pattern for passcode or security type purposes. The input timing requirement became part of the security feature. While the input example used an earbud, other transducers can generate enough signal for the input comparator.

Related Files

Programming code for **GreenPAK Designer**.

About the Author

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A	Jozef Froniewski	06/3/2014	New application note

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