SLG84901

Clock Synthesizer for Intel PCI-Express Gen3 Chipset

Features

- CK420BQ Clock Specification Revision 1.0
- PCIe Gen2: 3.1ps rms phase jitter compliant
- PCIe Gen3: 1.0ps rms phase jitter compliant
- Intel QPI: 0.3ps rms phase jitter compliant
- 64 pin TSSOP Package (6/6 RoHS Compliant)

Output Summary

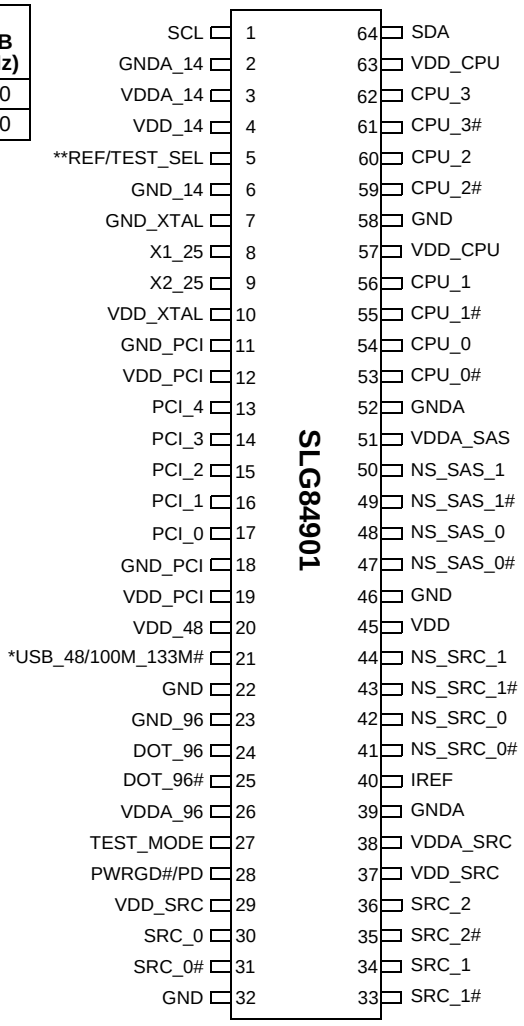
- 4- differential CPU clock outputs
- 5 - single-ended PCI clock outputs
- 2 - non-spread differential SAS clock outputs
- 3 - differential Serial Reference Clock (SRC) clock outputs
- 2 - non-spread differential NTB SRC clock outputs
- 1 - single-ended 48MHz clock output
- 1 - differential DOT96 clock output
- 1 - single-ended REF 14.318MHz clock output

Table 1. Frequency Select Table (FS_C, FS_B, FS_A)

100M_133M#	CPU (MHz)	SRC (MHz)	NS_SAS NS_SRC (MHz)	PCI (MHz)	REF (MHz)	DOT_96 (MHz)	USB (MHz)
0	133.3	100.0	100.0	33.3	14.318	96.0	48.0
1*	100.0	100.0	100.0	33.3	14.318	96.0	48.0

* Default power up frequency

Pin Configuration



64-pin TSSOP

** contains internal pull-down
* contains internal pull-up

Pin Description

Pin #	Name	Type	Description
1	SCL	I	Serial Interface bus clock input.
2	GNDA_14	GND	Ground for outputs.
3	VDDA_14	PWR	3.3V power supply for outputs.
4	VDD_14	PWR	3.3V power supply for outputs.
5	REF/TEST_SEL	I/O, SE	14.318MHz reference clock output. When TEST_SEL input is pulled to 3.3V during CKPWRGD# assertion, the device will configure into TEST MODE. Refer to DC Parameters section for FS input voltage threshold. After CKPWRGD assertion, this pin will be configured as REF output.
6	GND_14	GND	Ground for outputs.
7	GND_XTAL	GND	Ground for outputs.
8	X1_25	I	25MHz crystal input.
9	X2_25	O, SE	25MHz crystal output.
10	VDD_XTAL	PWR	3.3V power supply for outputs.
11	GND_PCI	GND	Ground for outputs.
12	VDD_PCI	PWR	3.3V power supply for outputs.
13	PCI_4	O, DIF	PCI clock output.
14	PCI_3	O, DIF	PCI clock output.
15	PCI_2	O, DIF	PCI clock output.
16	PCI_1	O, DIF	PCI clock output.
17	PCI_0	O, DIF	PCI clock output.
18	GND_PCI	GND	Ground for outputs.
19	VDD_PCI	PWR	3.3V power supply for outputs.
20	VDD_48	PWR	3.3V power supply for outputs.
21	USB_48/100M_133M#	I/O, SE	USB clock output. CPU Frequency Select, latched input.
22	GND	GND	Ground for outputs.
23	GND_96	GND	Ground for outputs.
24	DOT_96	O, DIF	96 MHz DOT clock output.
25	DOT_96#	O, DIF	96 MHz DOT clock output.
26	VDDA_96	PWR	3.3V power supply for outputs.
27	TEST_MODE	I	When in test mode, TEST_MODE will configure outputs to run at REF or Hi-Z. 0 = Hi-Z, 1 = REF
28	PWRGD#/PD	I	CKPWRGD is a 3.3V LVTTL iput. It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs. After CKPWRGD assertion, it becomes a real time input for asserting power down (active high).
29	VDD_SRC	PWR	3.3V power supply for outputs.
30	SRC_0	O, DIF	Differential Serial Reference Clock output.
31	SRC_0#	O, DIF	Differential Serial Reference Clock output.

Pin Description (continued)

Pin #	Name	Type	Description
32	GND	GND	Ground for outputs.
33	SRC_1#	O, DIF	Differential Serial Reference Clock output.
34	SRC_1	O, DIF	Differential Serial Reference Clock output.
35	SRC_2#	O, DIF	Differential Serial Reference Clock output.
36	SRC_2	O, DIF	Differential Serial Reference Clock output.
37	VDD_SRC	PWR	3.3V power supply for outputs.
38	VDDA_SRC	PWR	Low voltage I/O power supply for outputs.
39	GNDA	GND	Ground for outputs.
40	IREF	I	A precision resistor is attached to this pin, which is connected to the internal current reference. No Spread.
41	NS_SRC_0#	O, DIF	Differential Serial Reference Clock output. No Spread.
42	NS_SRC_0	O, DIF	Differential Serial Reference Clock output. No Spread.
43	NS_SRC_1#	O, DIF	Differential Serial Reference Clock output. No Spread.
44	NS_SRC_1	O, DIF	Differential Serial Reference Clock output. No Spread.
45	VDD	PWR	3.3V power supply for outputs.
46	GND	GND	Ground for outputs.
47	NS_SAS_0#	O, DIF	Differential SAS Clock output. No Spread.
48	NS_SAS_0	O, DIF	Differential SAS Clock output. No Spread.
49	NS_SAS_1#	O, DIF	Differential SAS Clock output. No Spread.
50	NS_SAS_1	O, DIF	Differential SAS Clock output. No Spread.
51	VDDA_SAS	PWR	3.3V power supply for outputs.
52	GNDA	GND	Ground for outputs.
53	CPU_0#	O, DIF	Differential CPU Clock output.
54	CPU_0	O, DIF	Differential CPU Clock output.
55	CPU_1#	O, DIF	Differential CPU Clock output.
56	CPU_1	O, DIF	Differential CPU Clock output.
57	VDD_CPU	PWR	3.3V power supply for outputs.
58	GND	GND	Ground for outputs.
59	CPU_2#	O, DIF	Differential CPU Clock output.
60	CPU_2	O, DIF	Differential CPU Clock output.
61	CPU_3#	O, DIF	Differential CPU Clock output.
62	CPU_3	O, DIF	Differential CPU Clock output.
63	VDD_CPU	PWR	3.3V power supply for outputs.
64	SDA	I/O, SE	Serial Interface bus data input and output.

*Note: Do not leave unused hardware strap pin floating, please add external pull-up and pull-down resistors on the schematic.

Block Diagram

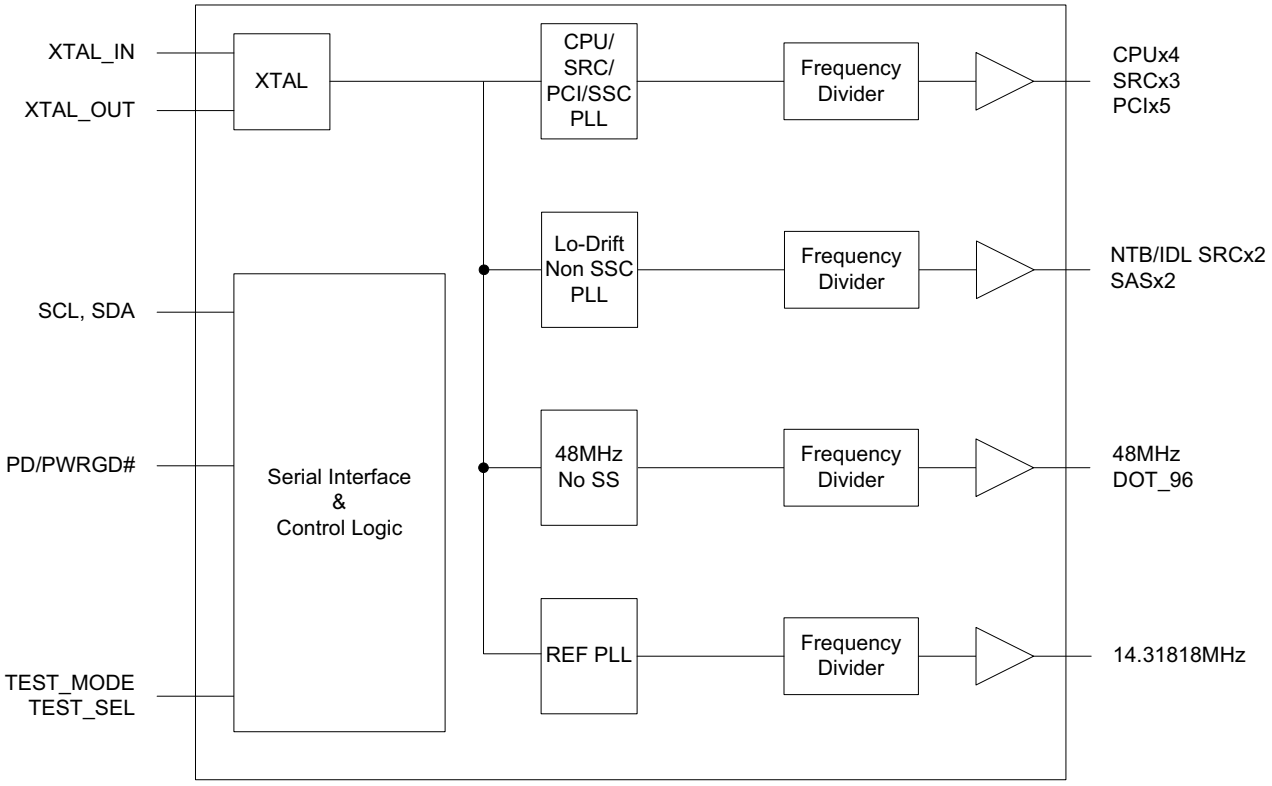


Figure 1. Simplified Block Diagram

Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 2*. The slave receiver address is 11010010 (D2h).

Table 2. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit '00000000' stands for block operation	11:18	Command Code - 8 Bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop

Table 3. Byte Read and Byte Write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Control Register Summary

Control Register 0

Bit	Type	Description/Function	Power up condition
7	RW	DOT_96 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	NS_SAS_1 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	NS_SAS_0 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	NS_SRC_1 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	NS_SRC_0 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	SRC_2 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	SRC_1 Output Enabled 0 = Disabled 1 = Enabled	1
0	RW	SRC_0 Output Enabled 0 = Disabled 1 = Enabled	1

Control Register 1

Bit	Type	Description/Function	Power up condition
7	RW	REF Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	Reserved	0
5	RW	Reserved	0
4	RW	CPU_3 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	CPU_2 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	CPU_1Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	CPU_0 Output Enabled 0 = Disabled 1 = Enabled	1
0	RW	Spread Spectrum Mode 0 = Spread off 1 = Spread on	0

Control Register 2

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	PCI_4 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	PCI_3 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	PCI_2 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	PCI_1 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	PCI_0 Output Enabled 0 = Disabled 1 = Enabled	1
0	RW	USB_48 Output Enabled 0 = Disabled 1 = Enabled	1

Control Register 3

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	0
4	RW	Reserved	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

Control Register 4

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	0
4	RW	Reserved	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

Control Register 5

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	0
4	RW	NS_SAS/NS_SRC Frequency Select FS_4	0
3	RW	NS_SAS/NS_SRC Frequency Select FS_3	1
2	RW	NS_SAS/NS_SRC Frequency Select FS_2	1
1	RW	NS_SAS/NS_SRC Frequency Select FS_1	1
0	RW	NS_SAS/NS_SRC Frequency Select FS_0	1

NS_SAS Frequency Margining Table

Byte 5					NS_SAS/NS_SRC (MHz)
Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	98.50
0	1	1	1	1	**100M (Default)**
1	1	1	1	1	101.50

Note: All values not listed in the table above are not supported.

Control Register 6

Bit	Type	Description/Function	Power up condition
7	RW	Test Mode 0 = Hi-Z or tristate 1 = REF/N	0
6	RW	Test Select 0 = Normal operation 1 = Test Mode enabled	0
5	RW	Reserved	0
4	R	100M_133MHz# Frequency Select	1
3	RW	CPU Frequency Margining bit 3	1
2	RW	CPU Frequency Margining bit 2	0
1	RW	CPU Frequency Margining bit 1	0
0	RW	CPU Frequency Margining bit 0	0

CPU Frequency Margining Table

Byte 6							
Bit 4 (HW Latch)	Bit 3	Bit 2	Bit 1	Bit 0	CPU (MHz)	SRC (MHz)	PCI (MHz)
1 = 100MHz	1	0	0	0	**100.00 (Default)**	**100.00**	**33.33**
1 = 100MHz	0	0	0	0	95.00	95.00	31.66
1 = 100MHz	1	1	1	1	105.00	105.00	35.00
0 = 133MHz	1	0	0	0	**133.33 (Default)**	**100.00**	**33.33**
0 = 133MHz	0	0	0	0	126.66	95.00	31.66
0 = 133MHz	1	1	1	1	140.00	105.00	35.00

Note:
.[1] Frequency values not listed in the table above are not supported.

Control Register 7

Bit	Type	Description/Function	Power up condition
7	R	Revision ID bit 3	0
6	R	Revision ID bit 2	0
5	R	Revision ID bit 1	0
4	R	Revision ID bit 0	0
3	R	Vendor ID bit 3	0
2	R	Vendor ID bit 2	1
1	R	Vendor ID bit 1	1
0	R	Vendor ID bit 0	0

Control Register 8

Bit	Type	Description/Function	Power up condition
7:0	RW	Byte count register for block read operation Note: The default value is 10. To read more than 10 bytes, system BIOS needs to change this register to the number of bytes it intends to read.	00001010

Control Register 9

Bit	Type	Description/Function	Power up condition
7	R	Device ID bit 7	0
6	R	Device ID bit 6	0
5	R	Device ID bit 5	0
4	R	Device ID bit 4	0
3	R	Device ID bit 3	0
2	R	Device ID bit 2	0
1	R	Device ID bit 1	0
0	R	Device ID bit 0	0

Control Register 10

Bit	Type	Description/Function	Power up condition
7:6	RW	REF Drive Strength **00 = 1X** 01 = 2X 10 = 3X 11 = Reserved	00
5	RW	PCI Drive Strength 0 = 1X 1 = 2X	0
4	RW	USB Drive Strength 0 = 1X 1 = 2X	0
3	RW	CPU PLL SS 0 = Center Spread 1 = Down Spread	1
2	RW	Reserved	0
1:0	RW	Table SS Ratio 00 = 0.2% 01 = 0.3% **10 = 0.5%** 11 = 1.0%	10

Crystal Recommendations

The SLG84901 requires a **Parallel Resonance Crystal.** Substituting a series resonance crystal will cause the SLG84901 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 4. Crystal Recommendations.

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Cut Accuracy (max.)	Temp Stability (max.)	Aging (max.)
25.000MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	35ppm	30ppm	5ppm

Absolute Maximum Ratings

Max VDD Supply Voltage (VDD_3.3):.....4.6V

Max Input Voltage (Vih):.....4.6V

Min Input Voltage (Vil):.....-0.5V

Storage Temperature::..... –65°C to + 150°C

Operating Temperature (Ambient, no airflow): . 0°C to +70°C

ESD Protection (Min):..... 2000V

DC Electrical Characteristics

Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDDA	3.3V Core Supply Voltage	±5%	3.135		3.465	V
VDD_3.3	3.3V Supply Voltage	±5%	3.135		3.465	V
Vih	Input High Voltage		2.0		VDD+0.3	V
Vil	Input Low Voltage		VSS-0.3		0.8	V
Iil	Input Leakage Current	0 < Vin < VDD	-5		+5	uA
Vih_FS	Input High Voltage (FS)		0.7		1.5	V
Vil_FS	Input Low Voltage (FS)		VSS-0.3		0.35	V
Voh	Output High Voltage (SE)	Ioh = -1mA	2.4			V
Vol	Output Low Voltage (SE)	Iol = 1mA			0.4	V
Cin	Input Pin Capacitance		2.5		4.5	pF
Cxtal	Xtall Pin Capacitance		3		5	pF
Cout	Output Pin Capacitance		2.5		4.5	pF
Lpin	Pin Inductance				7	nH
Ta	Ambient Temerature	No Airflow	0		70	°C
V_max	Diff Max Output	Include Overshoot			1.15	V
V_min	Diff Min Output	Include Undershoot			-0.3	V
Idd	Full Active				350	mA
Idd_pd	Power Down Mode	Outputs = tristate		30		mA

AC Electrical Characteristics

Differential Outputs (CPU, SRC, DOT_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Laccurracy	Long term accuracy		100	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average CPU Period (100MHz, SSC enabled)	9.99906	10.05107	ns	Average period over 1 us
Tperiod	Average CPU Period (133MHz, SSC enabled)	7.44930	7.53830	ns	Average period over 1 us
Tperiod	Average SRC Period (100MHz, SSC enabled)	9.99906	10.05107	ns	Average period over 1 us
Tperiod	Average DOT_96 Period (96MHz)	10.41354	10.41979	ns	Average period over 1 us
Tabs	Absolute Min/Max CPU Period (100, SSC disabled)	9.94900	10.05100	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC disabled)	7.44925	7.55075	ns	
Tabs	Absolute Min/Max CPU Period (100, SSC enabled)	9.94906	10.10107	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC enabled)	7.44930	7.58830	ns	
Tabs	Absolute Min/Max SRC Period (100, SSC disabled)	9.94900	10.05100	ns	
Tabs	Absolute Min/Max SRC Period (100, SSC enabled)	9.94906	10.10107	ns	
Tabs	Absolute Min/Max NS_SRC Period (SSC enabled)	9.94900	10.05100	ns	
Tabs	Absolute Min/Max NS_SAS Period (SSC disabled)	9.94900	10.05100	ns	
Tabs	Absolute Min/Max DOT_96 Period (96MHz)	10.16563	10.66771	ns	
Slew_rise	Rising slew rate	1.0	4.0	V/ns	1. Use ‘average’ acquisition mode of the scope 2. Measurement taken from differential waveform 3. Slew rate measured through V_swing voltage range centered about differential zero
Slew_fall	Falling slew rate	1.0	4.0	V/ns	1. Use ‘average’ acquisition mode of the scope 2. Measurement taken from differential waveform 3. Slew rate measured through V_swing voltage range centered about differential zero
Slew_var	Slew rate matching		20	%	1. Use ‘average’ acquisition mode of the scope 2. Measurement taken from single ended waveform 3. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculation
V_swing	Differential output swing	300		mV	Measurement taken from differential waveform
V_cr	Crossing point voltage	250	550	mV	1. Measurement taken from single ended waveform 2. V_cross is defined as the voltage where Clock = Clock# 3. Only applies to the differential rising edge (i.e. Clock rising and Clock# falling)
V_cr_dlt	Variation of V_cr		140	mV	1. Measurement taken from single ended waveform 2. V_cross is defined as the voltage where Clock = Clock# 3. V_cross delta is defined as the total variation of all crossing voltages of rising Clock and falling Clock#
Tskew	CPU[0:3] skew		50	ps	
Tccjitter	Cycle to Cycle Jitter (CPU)		50	ps	
Tccjitter	Cycle to Cycle Jitter (SRC)		50	ps	
Tccjitter	Cycle to Cycle Jitter (NS_SAS)		50	ps	

Differential Outputs (CPU, SRC, DOT_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Tccjitter	Cycle to Cycle Jitter (NS_SRC)		50	ps	
Tccjitter	Cycle to Cycle Jitter (DOT_96)		250	ps	
Tpj_src	SRC Phase Jitter PCIe Gen 2		3.1	ps	RMS Jitter. PCI-SIG Gen 2 Condition
Tpj_src	SRC Phase Jitter PCIe Gen 3		1.0	ps	RMS Jitter. PCI-SIG Gen 3 Condition
Tpj_cpu	QPI Phase Jitter (QPI 4.8Gb/s or 6.4Gb/s, 100MHz or 133Mhz)		0.5	ps	RMS Jitter. QPI
Tpj_cpu	QPI Phase Jitter (QPI 8Gb/s, 100MHz)		0.3	ps	RMS Jitter. QPI
Duty Cycle	Duty Cycle	45	55	%	

PCI Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		100	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 33.333333MHz
Tperiod	Average Period (SSC disabled)	29.99700	30.00300	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tperiod	Average Period (SSC enabled, -0.5%)	29.99718	30.15320	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tabs	Absolute Min/Max Period (SSC disabled)	29.49700	30.50300	ns	
Tabs	Absolute Min/Max Period (SSC enabled, -0.5%)	29.49718	30.65320	ns	
Thigh	CLK high time	12		ns	
Tlow	CLK low time	12		ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		500	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45	55	%	Measured with respect to 1.5V

USB_48 Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		100	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 48.000000MHz
Tperiod	Average Period	20.83125	20.83542	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tabs	Absolute Min/Max Period	20.48125	21.18542	ns	
Thigh	CLK high time	8.094	10.036	ns	
Tlow	CLK low time	7.694	9.836	ns	
Edge Rate	Rising edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system

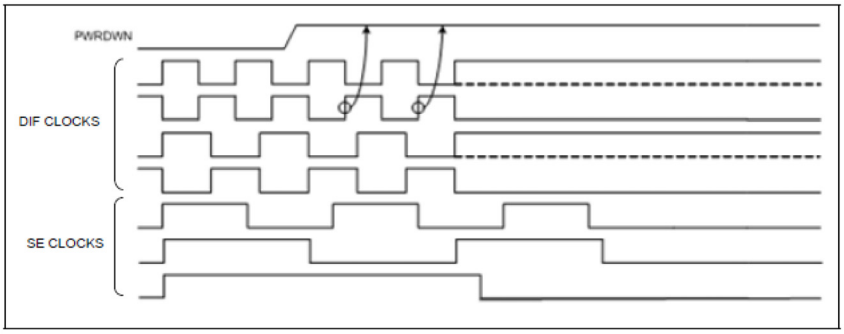
USB_48 Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Tccjitter	Cycle to cycle jitter		350	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45	55	%	Measured with respect to 1.5V

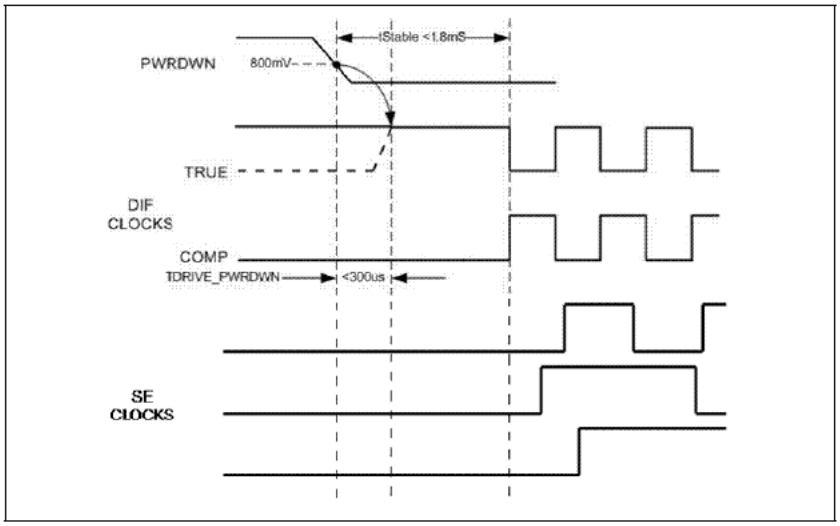
REF Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		100	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 25MHz
Tperiod	Average Period	69.83429	69.84826	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tabs	Absolute Min/Max Period	68.78429	69.89826	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		1000	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45	55	%	Measured with respect to 1.5V

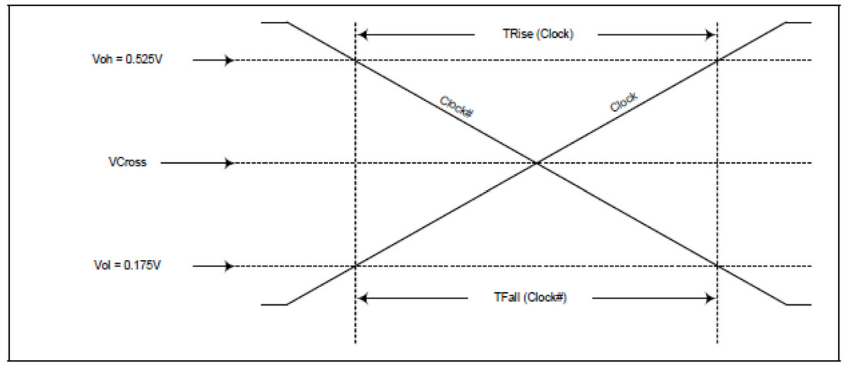
PWRDN# Assertion



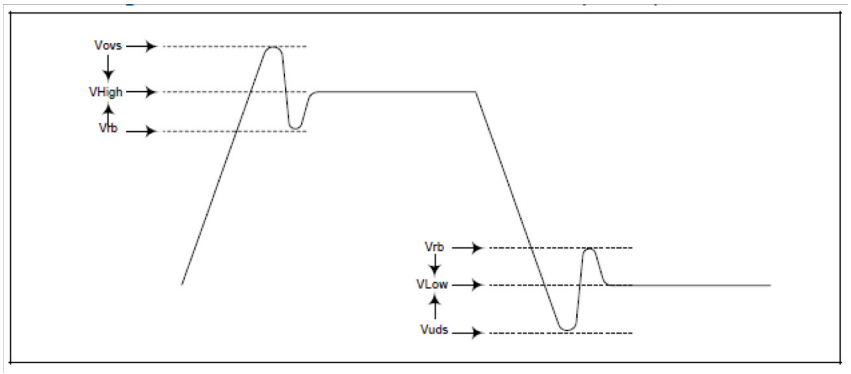
PWRGD Assertion (PWRDN# De-assertion)



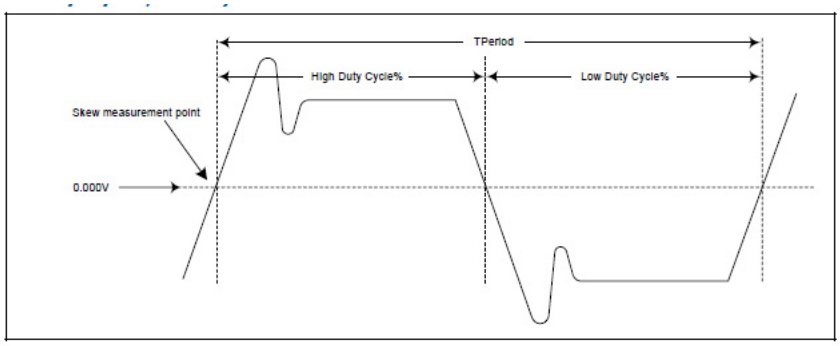
Single-ended Measurement Points for Trise, Tfall



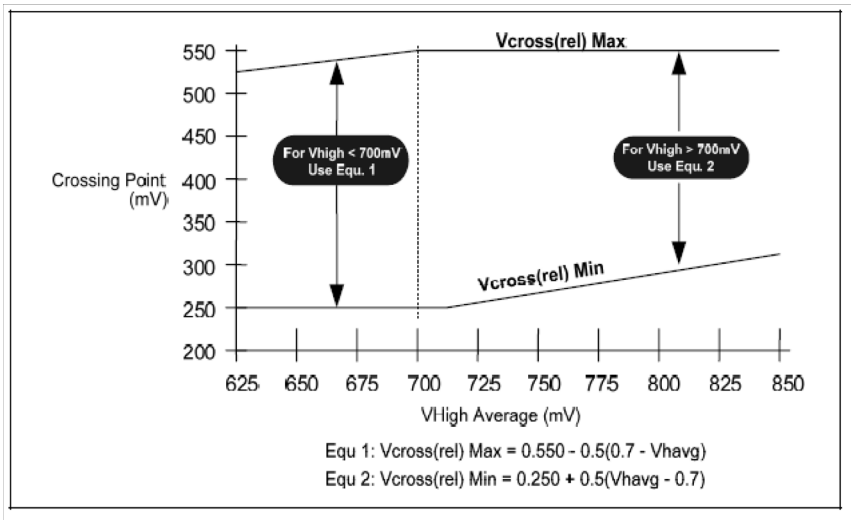
Single-ended Measurement Points for Vovs, Vuds, Vrb



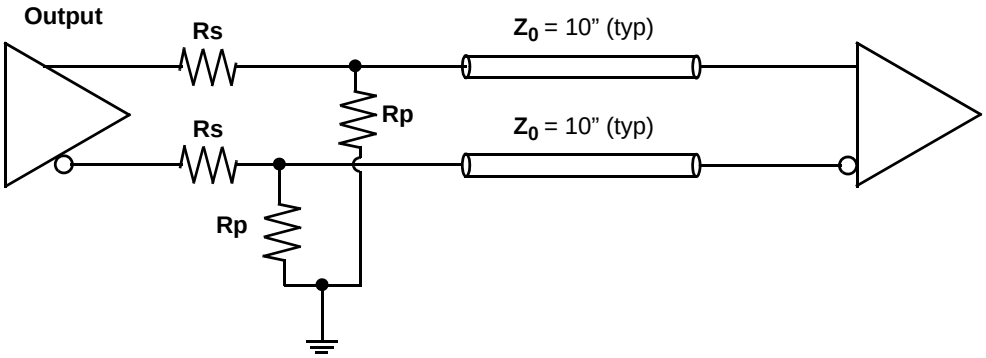
Differential (Clock - Clock#)Measurement Points for Tperiod, Duty Cycle, Jitter



Vcross Range Clarification



Test and Measurement - Differential Impedance Transmission Line



Clock	Board Trace Impedance	Rs	Rp	RIref	Units
DIFF Clocks 50Ω Configuration	100	33 (5%)	49.9 (1%)	475 (1%)	Ω
DIFF Clocks 43Ω Configuration	85	27 (5%)	42.2 (1%)	412 (1%)	Ω

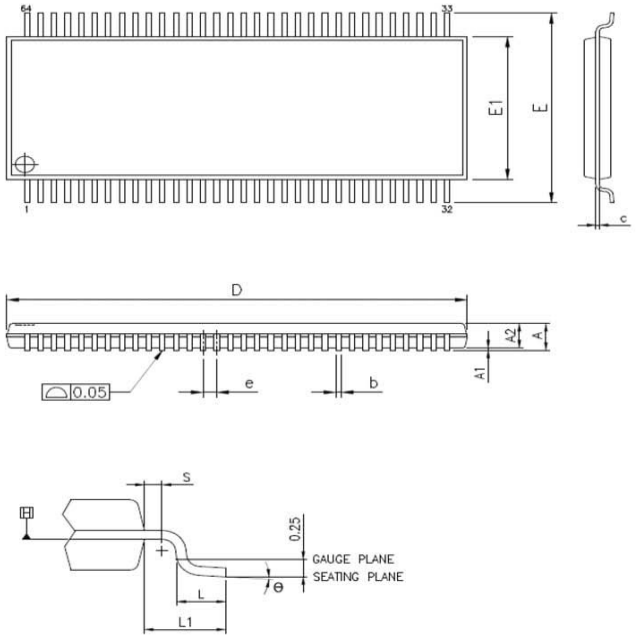
Part Number	Package Type	Temperature Range
SLG84901T	64 Lead Green Package TSSOP	Commercial, 0° to 70°C
SLG84901TTR	64 Lead Green Package TSSOP - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

64 Lead TSSOP Package

Package Type: TSSOP-64L (240 mil)

Unit: mm	Silego Spec (Comply to JEDEC MO-153 EF)		
Symbol	Min	NOM	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	0.95	1.05
b	-	0.20 TYP	-
c	0.09	-	0.20
D	16.90	17.00	17.10
E	7.95	8.10	8.25
E1	6.00	6.10	6.20
L	0.45	0.60	0.75
L1		1.00 REF	
e		0.50 BSC	
S		0.20 REF	
θ (Degree)	0	-	8



NOTES:

1. JEDEC OUTLINE : MO-153 EF.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Hub & Reel Size (mm)	Trailer A		Leader B		Pocket Tape (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TSSOP 64L 240 mil Green	64	17x8.1	2,000	2,000	330/100	42	504	42	504	24	12

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TSSOP 64L 240 mil Green	8.4	17.3	1.6	4	12	1.5	1.75	11.5	24