SLG84401

High Performance Server & PCI Express Gen 2 Synthesizer

Features

- CK410B+ clock for Intel-based servers, PCI Express Gen 2 and QPI support.
- Supports spread spectrum modulation, 0 to 0.5% down spread
- Uses external 14.318MHz crystal and external load capacitors for low ppm synthesis error
- CPU clocks independent of SRC/PCI clocks
- D2/D3 SMBus address

Key Specifications

- CPU cycle-cycle jitter: < 50 ps
- SRC cycle-cycle jitter: < 125ps
- PCI cycle-cycle jitter: < 500ps
- CPU output skew: < 50ps
- SRC output skew: < 250ps
- ± 300ppm frequency accuracy on all outputs except 48MHz
- ± 100ppm frequency accuracy on 48MHz
- PCIe Gen 2 Phase jitter: 3.1ps rms
- 56-pin & TSSOP

Output Summary

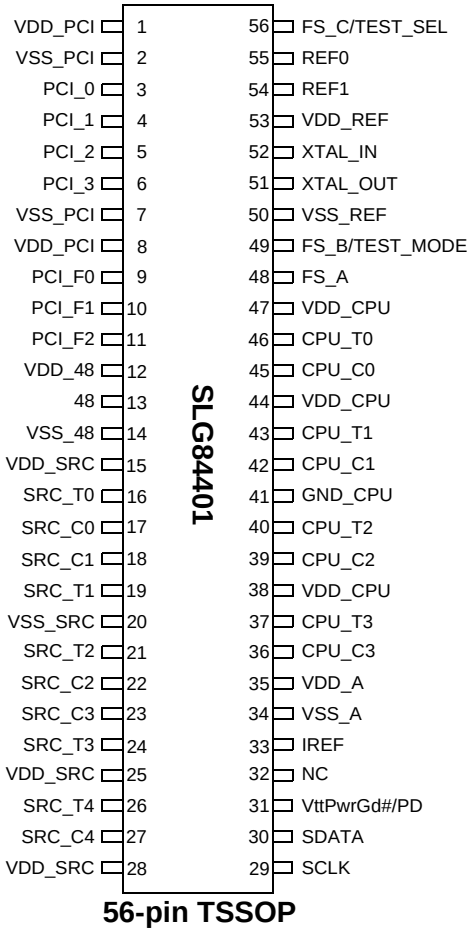
- 4 - 0.7V differential CPU clock outputs
- 5 - 0.7V differential SRC outputs
- 4 - PCI (33MHz)
- 3 - PCICLK_F, (33MHz) free-runnning
- 1 - single-ended 48MHz clock output
- 2 - single-ended 14.318MHz clock output

Table 1. Frequency Select Table (FS_C, FS_B, FS_A)

FS_C	FS_B	FS_A	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	48.0
0	0	1	133.3	100.0	33.3	14.318	48.0
0	1	0	200.0	100.0	33.3	14.318	48.0
0	1	1	166.6	100.0	33.3	14.318	48.0
1	0	0	333.3	100.0	33.3	14.318	48.0
1	0	1	100.0	100.0	33.3	14.318	48.0
1	1	0	400.0	100.0	33.3	14.318	48.0
1	1	1	Reserved				

*Other brands and names may be claimed as the property of others

Pin Configuration



56-pin TSSOP

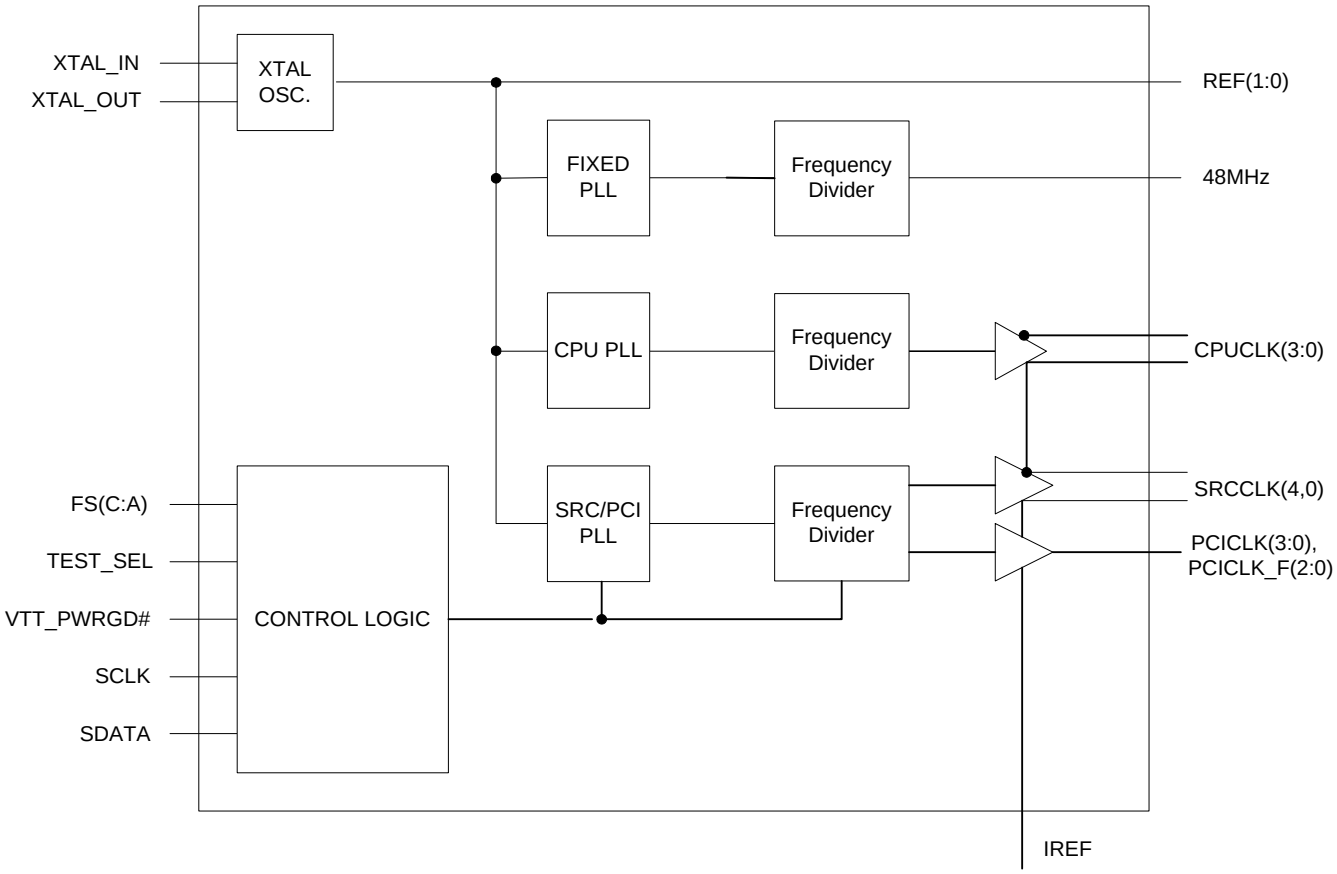
Pin Description

Pin #	Name	Type	Description
1	VDD_PCI	PWR	3.3V power supply for outputs.
2	VSS_PCI	GND	Ground for outputs.
3	PCI_0	OUT	PCI clock output.
4	PCI_1	OUT	PCI clock output.
5	PCI_2	OUT	PCI clock output.
6	PCI_3	OUT	PCI clock output.
7	VSS_PCI	GND	Ground for outputs
8	VDD_PCI	PWR	3.3V power supply for outputs.
9	PCI_F0	OUT	Free running PCI clock output.
10	PCI_F1	OUT	Free running PCI clock output.
11	PCI_F2	OUT	Free running PCI clock output.
12	VDD_48	PWR	3.3V power supply for outputs.
13	48	OUT	48MHz clock output
14	VSS_48	GND	Ground for outputs.
15	VDD_SRC	PWR	3.3V power supply for outputs.
16	SRC_T0	OUT	True clock of differential SRC clock pair.
17	SRC_C0	OUT	Complement clock of differential SRC clock pair.
18	SRC_C1	OUT	Complement clock of differential SRC clock pair.
19	SRC_T1	OUT	True clock of differential SRC clock pair.
20	VSS_SRC	GND	Ground for outputs.
21	SRC_T2	OUT	True clock of differential SRC clock pair.
22	SRC_C2	OUT	Complement clock of differential SRC clock pair.
23	SRC_C3	OUT	Complement clock of differential SRC clock pair.
24	SRC_T3	OUT	True clock of differential SRC clock pair.
25	VDD_SRC	PWR	3.3V power supply for outputs.
26	SRC_T4	OUT	True clock of differential SRC clock pair.
27	SRC_C4	OUT	Complement clock of differential SRC clock pair.
28	VDD_SRC	PWR	3.3V power supply for outputs.
29	SCLK	IN	Clock pin for SMBus circuitry, 5V tolerant
30	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant
31	VttPwrGd#/PD	IN	VTT_PWRGD# is a 3.3V LVTTL iput. It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs. After VTT_PWRGD# assertion, it becomes a real time input for asserting power down (active high).
32	NC	N/A	No Connection
33	IREF	OUT	This pin establishes the reference current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
34	VSS_A	GND	Ground for PLL core.

Pin Description (continued)

Pin #	Name	Type	Description
35	VDD_A	PWR	3.3V power supply for PLL.
36	CPU_C3	OUT	Complement clock of differential CPU clock pair.
37	CPU_T3	OUT	True clock of differential CPU clock pair.
38	VDD_CPU	PWR	3.3V power supply for outputs.
39	CPU_C2	OUT	Complement clock of differential CPU clock pair.
40	CPU_T2	OUT	True clock of differential CPU clock pair.
41	GND_CPU	GND	Ground for outputs.
42	CPU_C1	OUT	Complement clock of differential CPU clock pair.
43	CPU_T1	OUT	True clock of differential CPU clock pair.
44	VDD_CPU	PWR	3.3V power supply for outputs.
45	CPU_C0	OUT	Complement clock of differential CPU clock pair.
46	CPU_T0	OUT	True clock of differential CPU clock pair.
47	VDD_CPU	PWR	3.3V power supply for outputs.
48	FS_A	IN	3.3V power supply for outputs.
49	FS_B/TEST_MODE	IN	Frequency Select input to determine CPU output frequency. When in test mode, FS_B/TEST_MODE will configure outputs to run at Ref or Hi-Z. 0 = Hi-Z, 1 = Ref
50	VSS_REF	GND	Ground for outputs.
51	XTAL_OUT	OUT	14.318MHz crystal output.
52	XTAL_IN	IN	14.318MHz crystal input.
53	VDD_REF	PWR	3.3V power supply for outputs.
54	REF1	OUT	14.318 reference clock.
55	REF0	OUT	14.318 reference clock.
56	FS_C/TEST_SEL	IN	Frequency Select input to determine CPU output frequency. When FS_C/TEST_SEL input is pulled to 3.3V during VTT_PWRGD# assertion, the device will configure into TEST MODE. Refer to DC Parameters section for FS input voltage threshold.

Block Diagram



PD (Power Down) Clarification

The VTT_PWRGD#/PD pin is a dual function pin. During initial power-up, the pin functions as VTT_PWRGD#. Once VTT_PWRGD# has been sampled low by the device, the pin assumes PD functionality. The PD pin is an asynchronous active high input used to shut off ALL clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. When PD is asserted high, all clocks are driven to a low value and held prior to turning off the VCOs and the crystal oscillator.

Table 2. PD Functionality

PD	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	REF
0	Normal	Normal	Normal	Normal	33MHz	48MHz	14.318MHz
1	Iref*2 or Float	Float	Iref*2 or Float	Float	Low	Low	Low

PD# - Assertion

When PD is sampled high by two consecutive rising edges of CPU#, all single-ended outputs will be held low on their next high to low transition and differential clocks will be held high or tristated (depending on the state of the control register drive mode bit) on the next “Diff clock#” high to low transition. When the PD drive mode bit corresponding to the differential (CPU, SRC and DTOT_96) clock output of interest is programmed to ‘0’, the clock output will be held with the “Diff clock” pin driven high at 2 x Iref, and “Diff clock#” tristated. If the control register PD drive mode bit corresponding to the output of interest is programmed to ‘1’, then both the “Diff clock” and the “Diff clock#” are tristated.

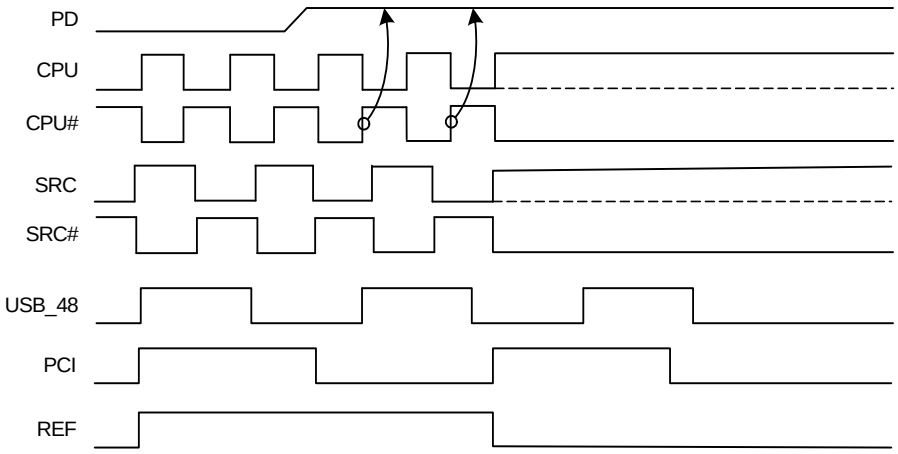


Figure 1. Power Down Assertion

PD De-assertion

The power-up latency is less than 1.8ms. This is the time from the de-assertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock device. All differential outputs stopped in a tristate condition resulting from power down will be driven high in less than 300us of PD de-assertion to voltage greater than 200mV.

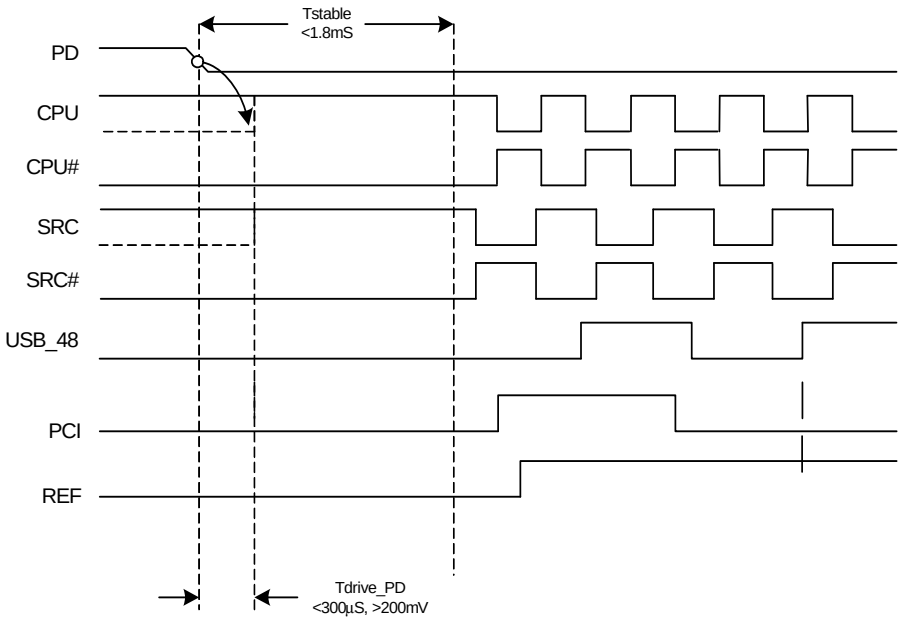


Figure 2. Power Down De-assertion

General SMBus serial interface information for the SLG84401

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- Silego clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- Silego clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- Silego clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
(see Note 2)
- Silego clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- Silego clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- Silego clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- Silego clock will ***acknowledge***
- Silego clock will send the data byte count = X
- Silego clock sends ***Byte N + X -1***
- Silego clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).***
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation			
Controller (Host)			**Silego(Slave/Receiver)**
T	Start Bit		
Slave Address D2 (H)			
WR	Write		
			Ack
Beginning Byte = N			
			Ack
Data Byte Count = X			
			Ack
Beginning Byte N		X Byte	
			Ack
O			
O			O
O			O
			O
Byte N + X - 1			
			Ack
P	Stop Bit		

Index Block Read Operation			
Controller (Host)		**Silego (Slave/Receiver)**	
T	Start Bit		
Slave Address D2 (H)			
WR	Write		
			Ack
Beginning Byte = N			
			Ack
RT	Repeat Start		
Slave Address D3 (H)			Ack
RD	Read		
			Ack
			Data Byte Count = X
Ack			
		X Byte	Beginning Byte N
Ack			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not Ack		
P	Stop Bit		

SMBus Table: SRC Output Enable Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	NA	SRCCLK7 Enable	Output Enable	RW	Disable -Hi-Z	Enable	1
Bit 6	NA	SRCCLK6 Enable	Output Enable	RW	Disable -Hi-Z	Enable	1
Bit 5	NA	SRCCLK5 Enable	Output Enable	RW	Disable -Hi-Z	Enable	1
Bit 4	26,27	SRCCLK4 Enable	Output Enable	RW	Disable -Hi-Z	Enable	1
Bit 3	23,24	SRCCLK3 Enable	Output Enable	RW	Disable -Hi-Z	Enable	1
Bit 2	21,22	SRCCLK2 Enable	Output Enable	RW	Disable -Hi-Z	Enable	1
Bit 1	18,19	SRCCLK1 Enable	Output Enable	RW	Disable -Hi-Z	Enable	1
Bit 0	16,17	SRCCLK0 Enable	Output Enable	RW	Disable -Hi-Z	Enable	1

SMBus Table: CPU, REF and 48MHz Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	54	REF1 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 6	55	REF0 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 5	36,37	CPUCLK3	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 4	39,40	CPUCLK2	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 3	Reserved						0
Bit 2	42,43	CPUCLK1	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 1	45,46	CPUCLK0	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 0	CPU,SRC,PCI	Spread Spectrum Enable	Spread Off/On	RW	Spread Off	Spread On	0

SMBus Table:PCI and PCI_F Output Enable Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	6	PCI_3	Output Control	RW	Disable-Low	Enable	1
Bit 6	5	PCI_2	Output Control	RW	Disable-Low	Enable	1
Bit 5	4	PCI_1	Output Control	RW	Disable-Low	Enable	1
Bit 4	3	PCI_0	Output Control	RW	Disable-Low	Enable	1
Bit 3	11	PCI_F2 Enable	Output Control	RW	Disable-Low	Enable	1
Bit 2	10	PCI_F1 Enable	Output Control	RW	Disable-Low	Enable	1
Bit 1	9	PCI_F0 Enable	Output Control	RW	Disable-Low	Enable	1
Bit 0	13	48 MHz Enable	Output Control	RW	Disable-Low	Enable	1

SMBBus Table: PCI_F and SRC Stop Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	11	PCI_F2 Stop En	Free Running Control, Default: not affected by PCI/SRC_STOP (Byte 4, bit5)	RW	Free-Running	Stoppable	1
Bit 6	10	PCI_F1 Stop En		RW	Free-Running	Stoppable	1
Bit 5	9	PCI_F0 Stop En		RW	Free-Running	Stoppable	1
Bit 4	26,27	SRCCLK4 Stop En		RW	Free-Running	Stoppable	1
Bit 3	23,24	SRCCLK3 Stop En		RW	Free-Running	Stoppable	1
Bit 2	21,22	SRCCLK2 Stop En		RW	Free-Running	Stoppable	1
Bit 1	18,19	SRCCLK1 Stop En		RW	Free-Running	Stoppable	1
Bit 0	16,17	SRCCLK0 Stop En		RW	Free-Running	Stoppable	1

SMBBus Table: CPU and SRC Stop and Power Down Mode Drive Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	36,37	CPUCLK3 PD Drive	Drive Mode in PD	RW	Driven	Hi-Z	0
Bit 6	39,40	CPUCLK2 PD Drive	Drive Mode in PD	RW	Driven	Hi-Z	0
Bit 5	42,43	CPUCLK1 PD Drive	Drive Mode in PD	RW	Driven	Hi-Z	0
Bit 4	45,46	CPUCLK0 PD Drive	Drive Mode in PD	RW	Driven	Hi-Z	0
Bit 3	36,37	CPUCLK3 Stop En	Free Running Control, Default: not affected by CPU_STOP	RW	Free Running	Stoppable	1
Bit 2	39,40	CPUCLK2 Stop En		RW	Free Running	Stoppable	1
Bit 1	42,43	CPUCLK1Stop En		RW	Free Running	Stoppable	1
Bit 0	45,46	CPUCLK0 Stop En		RW	Free Running	Stoppable	1

SMBus Table: Output and Spread Spectrum Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Reserved					0
Bit 6	SRC	SRC Stop Drive Mode	Driven in STOP	RW	Driven	Hi-Z	0
Bit 5	SRC	SRC PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 4		Reserved					0
Bit 3	36,37	CPUCLK3 Stop Drive	Drive Mode in Stop	RW	Driven	Hi-Z	0
Bit 2	39,40	CPUCLK2 Stop Drive	Drive Mode in Stop	RW	Driven	Hi-Z	0
Bit 1	42,43	CPUCLK1 Stop Drive	Drive Mode in Stop	RW	Driven	Hi-Z	0
Bit 0	45,46	CPUCLK0 Stop Drive	Drive Mode in Stop	RW	Driven	Hi-Z	0

SMBus Table: Device ID Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Test Mode Sel.	Test Mode Selection	RW	Hi-Z	REF/N	0
Bit 6	-	Test Clock Mode Entry	Test Mode	RW	Disable	Enable	0
Bit 5	-	Reserved					0
Bit 4	55,54	REF Drive Strength	1X or 2X	RW	1X	2X	1
Bit 3	PCI, SRC	PCI_STOP Control	Stop Non-free running PC and SRC clocks	RW	Stop	Run	1
Bit 2	-	FS_C	FS_C Readback	R	See 932S401 Functionality Table		latch
Bit 1	-	FS_B	FS_B Readback	R			latch
Bit 0	-	FS_A	FS_A Readback	R			latch

SMBus Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	Revision ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	Vendor ID	R	-	-	0
Bit 2	-	VID2		R	-	-	1
Bit 1	-	VID1		R	-	-	1
Bit 0	-	VID0		R	-	-	0

SMBus Table: Vendor & Revision ID Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 8 bytes. (0 to 7)		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			0
Bit 2	-	BC2		RW			1
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			1

REF Drive Strength Functionality

Byte6, bit 4	Byte10, bit 1	Byte10, bit 0	REF1	REF0
0	X	X	1x	1x
1	0	0	1x	1x
1	0	1	1x	2x
1	1	0	2x	1x
1	1	1	2x	2x

CPU, SRC and PCI Divider Ratios

	Div(3:0)	Divider
0	0000	2
1	0001	3
2	0010	5
3	0011	15
4	0100	4
5	0101	6
6	0110	10
7	0111	30
8	1000	8
9	1001	12
10	1010	20
11	1011	60
12	1100	16
13	1101	24
14	1110	40
15	1111	120

Crystal Recommendations

The SLG84401 requires a **Parallel Resonance Crystal.** Substituting a series resonance crystal will cause the SLG84401 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 3. Crystal Recommendations.

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Cut Accuracy (max.)	Temp Stability (max.)	Aging (max.)
14.31818MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	35ppm	30ppm	5ppm

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
VDD_A	3.3V Core Supply Voltage		V_{DD} + 0.5V	V
VDD_In	3.3V Logic Supply Voltage	GND - 0.5	V_{DD} + 0.5V	V
T_S	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD protection	Input ESD protection human body model	2000		V

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 -70 °C; Supply Voltage V_{DD} = 3.3V +/-5%

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input High Voltage	V_{IH}	V_{DD} = 3.3 V +/-5%	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	V_{DD} = 3.3V +/-5%	V_{SS} - 0.3		0.8	V	
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	
Input Low Current	I_{IL1}	V_{IN} = 0V; Inputs with no pull-up resistors	-5			uA	
	I_{IL2}	V_{IN} = 0V; Inputs with pull-up resistors	-200			uA	
Low Threshold Input High Voltage	V_{IH_FS}	V_{DD} = 3.3 V +/-5%	0.7		V_{DD} + 0.3	V	
Low Threshold Input Low Voltage	V_{IL_FS}	V_{DD} = 3.3V +/-5%	V_{SS} - 0.3		0.35	V	
Operating Supply Current	$I_{DD3·3OP}$	V_{DD} = 3.465V, Full load		246	300	mA	
Powerdown Current	$I_{DD3·3PD}$	All differential pairs driven		60	90	mA	
		All differential pairs tri-stated		5.4	15	mA	
Input Frequency	F_i	V_{DD} = 3.3V		14.318		MHz	1
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	CINX	XTAL_IN and XTAL_OUT pins			5	pF	
CLK Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or deassertion of PD# to 1st clock			1.8	ms	1,2
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		CPU output enable after PD# de-assertion			300	us	1
Tfall		Fall time of PD#			5	ns	1
Trise		Rise time of PD#			5	ns	2
SMBus voltage	V_{IMAX}	Max Voltage on SCLK/SDATA			5.5	V	1
Low-level Output Voltage	$V_{OLSM-BUS}$	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH +0.15) to (Max ViL - 0.15)			300	ns	1

[1] Guaranteed by design and characterization, not 100% tested in production.
[2] See timing diagrams for timing requirements.
[3] Input frequency should be measured at the REF output tuned to ideal 14.31818 MHz to meet ppm accuracy on PLL outputs.

Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

T_A = 0 - 70 °C; V_{DD} = 3.3V +/-5% C_L=2pF, R_S=33.2Ω R_P=49.9Ω I_{REF} = 475Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Current Source Output Impedance	Z_O	$V_O = V_X$	3000			Ω	1
Voltage High	V_{High}	Statistical measurement on single ended signal using oscilloscope math function.	660	775	850	mV	1
Voltage Low	V_{Low}		-150	70	150		1
Max Voltage	V_{ovs}	Measurement on single ended signal using absolute value			1150	mV	1
Min Voltage	V_{uds}		-300				1
Crossing Voltage (abs)	$V_{cross(abs)}$		250	355	550	mV	1
Crossing Voltage (var)	d-V_{cross}	Variation of crossing over all edges		90	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300	0	300	ppm	1,2
Average Period	T_{period}	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66Hz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	400 MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.4128			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	240	700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	359	700	ps	1
Rise Time Variation	d-t_r			49	125	ps	1
Fall Time Variation	d-t_f			59	125	ps	1
Duty Cycle	d_{t3}	Measurement from differential waveform	45	49	55	%	1
Skew	t_{sk3}	CPU(3:0) V_T = 50%		33	50	ps	1
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	Measurement from differential waveform		38	50	ps	1

[1] Guaranteed by design, not 100% tested in production
[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that the REFout is at 14.31813MHz.
[3] Post process evaluation through PCI-SIG Matlab scripts (Intel Jitter Tool Rev 1.5)

Electrical Characteristics - SRC 0.7V Current Mode Differential Pair

T_A = 0 -70 °C; V_{DD} = 3.3V +/-5% C_L=2pF, R_S=33.2Ω R_P=49.9Ω I_{REF} = 475Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Current Source Output Impedance	Z_O[1]	$V_O = V_X$	3000			Ω	1
Voltage High	V_{High}	Statistical measurement on single ended signal using oscilloscope math function.	660	780	850	mV	1
Voltage Low	V_{Low}		-150	10	150		1
Max Voltage	V_{ovs}	Measurement on single ended signal using absolute value			1150	mV	1
Min Voltage	V_{uds}		-300				1
Crossing Voltage (abs)	$V_{cross(abs)}$		250	369	550	mV	1
Crossing Voltage (var)	d-V_{cross}	Variation of crossing over all edges		57	140	mV	1
Long Accuracy	ppm	see T_{period} min-max values	-300	0	300	ppm	1,2
Average period	T_{period}	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, VOH = 0.525V	175	283	700	ps	1
Fall Time	t_f	V_{OH} = 0.525V VOL = 0.175V	175	291	700	ps	1
Rise Time Variation	d-t_r			27	125	ps	1
Fall Time Variation	d-t_f			30	125	ps	1
Duty Cycle	d_{t3}	Measurement from differential waveform	45	501	55	%	1
Skew	t_{sk3}	SRC(4:0) V_T = 50%		15	250	ps	1
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	Measurement from differential waveform		38	125	ps	1
Phase Jitter	t_{pj_src}	SRC Phase Jitter PCIe Gen 1			86	ps	1,3
Phase Jitter	t_{pj_src}	SRC Phase Jitter PCIe Gen 2 Low Frequency			3.0	ps	1,3
Phase Jitter	t_{pj_src}	SRC Phase Jitter PCIe Gen 2 High Frequency			3.1	ps	1,3

[1] Guaranteed by design and characterization, not 100% tested in production.
[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFout is at 14.31818MHz
[3] Post process evaluation through PCI-SIG Matlab scripts (Intel Jitter Tool Rev 1.5)

Electrical Characteristics - PCICLK/PCICLK_F

T_A = 0 -70 °C; V_{DD} = 3.3V +/-5% C_L=5pF (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Long Accuracy	ppm	see T_{period} min-max values	-300	0	300	ppm	1,2
Clock period	T_{period}	33.33MHz output nominal	29.99100		30.00900	ns	2
		33.33MHz output spread	29.99100		30.15980	ns	2
Absolute min period	T_{abs}	33.33MHz output nominal	29.49100		30.50900	ns	2
		33.33MHz output spread	29.49100		30.65980	ns	2
Clock High Time	t_{h1}		12		N/A	ns	1
Clock Low Time	t_{l1}		12		N/A	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.55	V	
Output High Current	I_{OH}	V_{OH} @MIN = 1.0V	-33			mA	
		V_{OH} @MAX = 3.135V			-33	mA	
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95V	30			mA	
		V_{OHL} @MAX = 0.4V			38	mA	
Rise Time	t_{r1}	V_{OL} = 0.4V, V_{OH} = 2.4V	0.5	0.74	2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4V, V_{OL} = 0.4V	0.5	0.73	2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5V	45	50.4	55	%	1
Skew	t_{sk1}	V_T = 1.5V		43	500	ps	1
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	V_T = 1.5V		98	500	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.
[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFout is at 14.31818MHz

Electrical Characteristics - 48MHz

T_A = 0 -70 °C; V_{DD} = 3.3V +/-5% C_L=5pF (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Long Accuracy	ppm	see T_{period} min-max values	-100	0	100	ppm	1,2
Clock period	T_{period}	48.0000MHz output nominal	20.83125		20.83542	ns	2
Absolute Min/Max Clock period	T_{abs}	Nominal	20.48125		21.18542	ns	2
Clock High Time	t_{h1}		8.094			ns	1
Clock Low Time	t_{l1}		7.694			ns	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0V	-33			mA	
		V_{OH} @MAX = 3.135V			-33	mA	
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95V	30			mA	
		V_{OL} @MAX = 0.4V			38	mA	
Rise Time	t_{r1}	V_{OL} = 0.4V, V_{OH} = 2.4V	1	1.1	2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4V, V_{OL} = 0.4V	1	1.3	2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5V	45	52.3	55	%	1
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	V_T = 1.5V		243	350	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.
[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFout is at 14.31818MHz

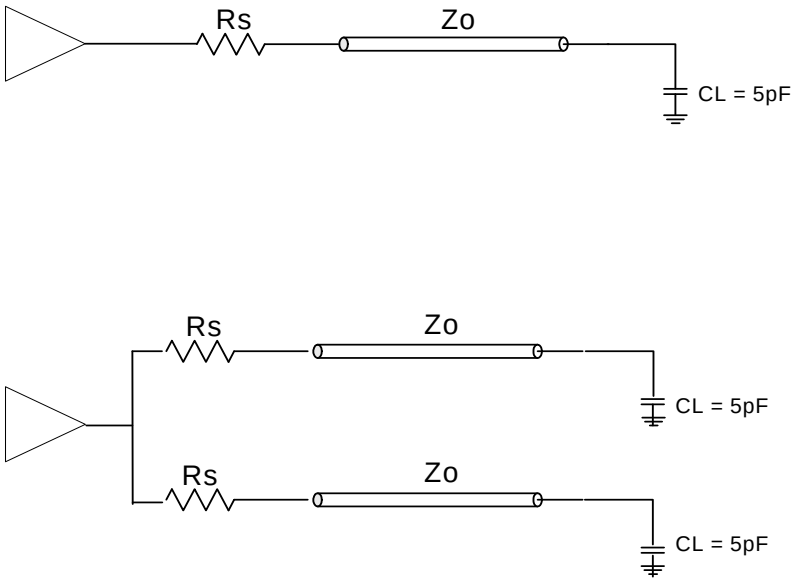
Electrical Characteristics - REF-14.318MHz

T_A = 0 -70 °C; V_{DD} = 3.3V +/-5% C_L=5pF (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Long Accuracy	ppm	see T_{period} min-max values	-300	0	300	ppm	1
Clock period	T_{period}	48.0000MHz output nominal	69.82033		69.86224	ns	1
Absolute Min/Max Clock period	T_{abs}	Nominal	68.82033		70.86224	ns	
Output High Voltage	V_{OH}	I_{OH} = -1mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0V V_{OH} @MAX = 3.135V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95V V_{OHL} @MAX = 0.4V	29		27	mA	1
Rise Time	t_{r1}	V_{OL} = 0.4V, V_{OH} = 2.4V	0.5	0.6	2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4V, V_{OL} = 0.4V	0.5	0.85	2	ns	1
Skew	t_{sk1}	V_T = 1.5V			500	ps	1
Duty Cycle	d_{t1}	V_T = 1.5V	45	52.7	55	%	1
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	V_T = 1.5V		917	1000	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

Single Ended Output Terminations

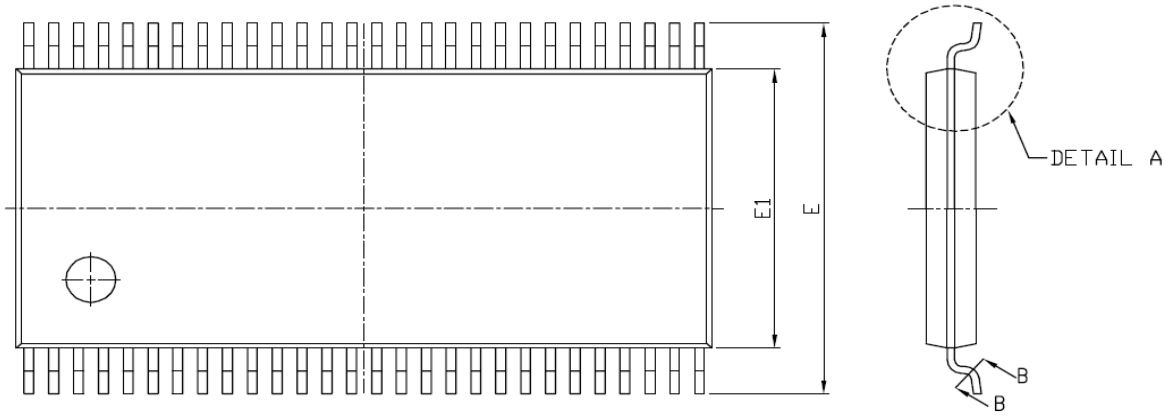


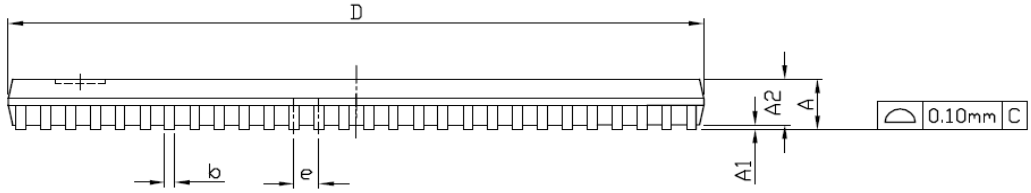
The single-ended outputs of the SLG84401default to a drive strength of 2 loads. The REF clocks can be turned down to 1-load strength via the SMBus. Suggested termination resistors are as follows for transmission lines with Zo = 50 ohms.

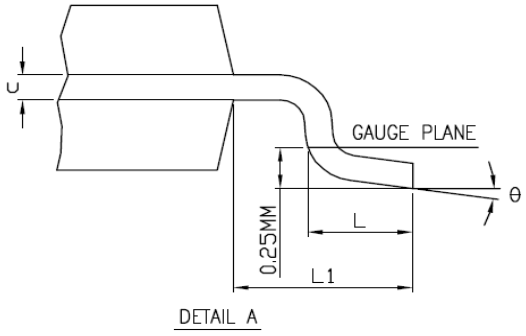
Single-ended outputs at 2-load strength (Power up default for all single-ended outputs)	Driving 1 load, Rs =33 ohms
	Driving 2 loads, Rs = 7.5 ohms
Single-ended outputs at 1-load strength (REF clock only)	Driving 1 load, Rs = 22 ohms

Package Drawing and Dimensions

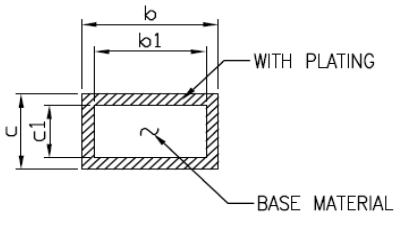
56 Lead TSSOP Package







DETAIL A



SECTION B–B

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
E	8.00	8.10	8.20	0.315	0.319	0.323
E1	6.00	6.10	6.20	0.236	0.240	0.244
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
b	0.20 TYP.			0.008 TYP.		
⚠ b1	0.15 TYP.			0.006 TYP.		
c	0.09		0.20	0.004		0.008
⚠ c1	0.05	0.15	0.16	0.002		0.006
e	0.50 BSC.			0.020 BSC.		
θ	0		8	0		8

	D (MM)			JEDEC
N	MIN.	NOM	MAX.	
48	12.40	12.50	12.60	MO–153ED
56	13.90	14.00	14.10	MO–153EE
64	16.90	17.00	17.10	MO–153EF

Ordering Information

Part #	Package Type	Temp Range
SLG84401T	56 LEAD TSSOP	0°C to 70°C
SLG84401TTR	56 LEAD TSSOP - Tape and Reel	0°C to 70°C

OOrdering