Testing Power-up Conditions on GPAK Evaluation Board

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Introduction

Testing each combination of input logic at power-up is important in ensuring correctness in all cases for a given design. The GreenPAK evaluation board is designed for testing power-up conditions in GPAK hardware.

This application note will cover a simple example where the designer must test power-up conditions and determine an appropriate solution.

A Simple Delayed Output

The example circuit is a rising edge delay with one input and one output. The output copies the input; however, the input must be held HIGH for 500ms before the output will be HIGH. The design of this circuit is only one delay block in the GreenPAK software. The design is shown in Figure 1.

Testing the Power-Up Response

To test the device's power-up response, you must program the design into the NVM (Non-Volatile Memory). Since GreenPAK is a one-time programmable device, make sure the design does as you intend it in normal operation before testing the power-up conditions.

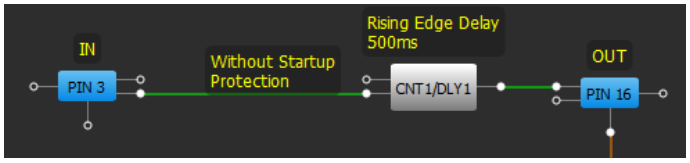

Figure 1. GPAK Delay Circuit

Programming the Chip

From the GreenPAK designer software, start the Emulation Tool by pressing the 

button on the ribbon.

From the Emulator Window, program the device by pressing the "Program" button found in the top right of the window.

The software will notify you that the chip can be programmed only once, continue by clicking the "Yes" button. After a few moments, the software will notify you if the programming was a success.[1]

Test Mode

Once the chip has been programmed in NVM, you can enter Test Mode without performing Emulation. Emulation drives the register bits on power-up, so you cannot get a true startup response in Emulator mode. Enter Test Mode by pressing the Test Mode button found in the top right of the Emulation Window. The Test Mode button will highlight orange to show the board is in Test Mode.[2]

Configuring the Signal Generator

Click the Edit button next to the VDD Signal Generator PIN1 (Figure 2) in the Emulation Window. You will see the signal wizard appear, it will be similar to Figure 3.

Figure 2. Signals' Interface from Emulation

On the left hand side of the signal wizard (Figure 3), you may choose to Globally Link the signal.

[1] *Note: If the chip has already been programmed, you must replace the chip on the evaluation board with a chip that has never been programmed.*

[2] *Note: The Emulation button should not be highlighted.*

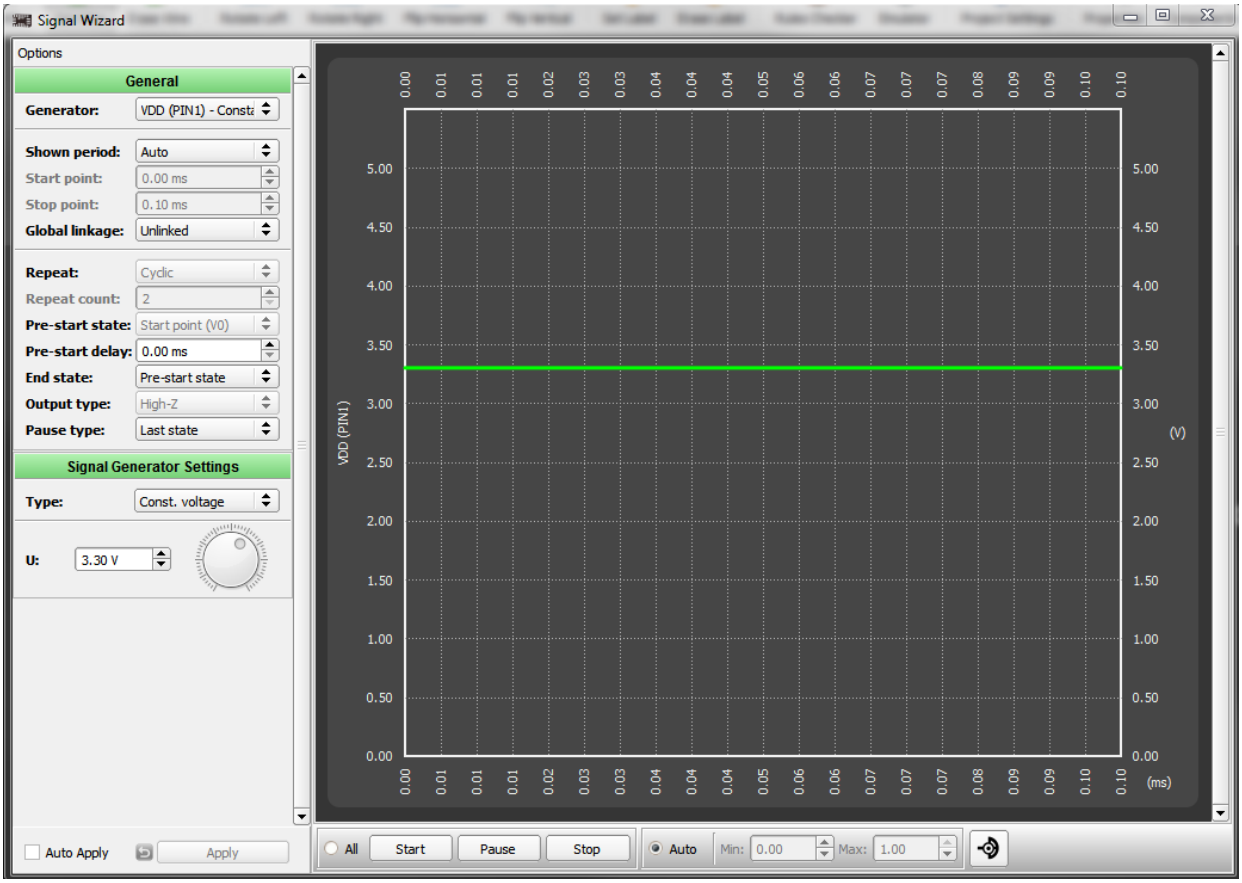

Figure 3. Signal Wizard

Global linkage causes all linked signals to start, pause and stop together when using Start Gens, Pause Gens, and Stop Gens buttons at the bottom of the emulator window.

By default, all generators except for VDD are globally linked.[3]

For this example, we will Globally Link VDD. In order to simulate power-up conditions, we will be pausing and starting VDD, thus in the signal wizard window select the Pause Type to be “0.00 V” from the drop down menu.

In order to simulate the input being HIGH while the VDD is powered up, we will create a logic generator on the input and have it start HIGH at the same time as VDD. This is done by right-clicking on PIN2 in the emulator window and selecting “Logic Generator”.

Choose Edit by PIN2 to bring up the Signal Wizard. Insert two more logic levels and configure the settings like those shown in Figure 4.[4]

Since the two signals are linked, you can power down the device by pressing the button “Pause Gens” and repower the device be pressing “Start Gens”.

This also starts the Logic Generator on PIN2, which will simulate the case in which the input is engaged as VDD powers on.

[3] *Note: any Signal or Logic Generator can be Globally Linked/Unlinked by pressing the “G” in the signals’ interface, Figure 2.*

[4] *Note: Don’t forget to hit Apply*

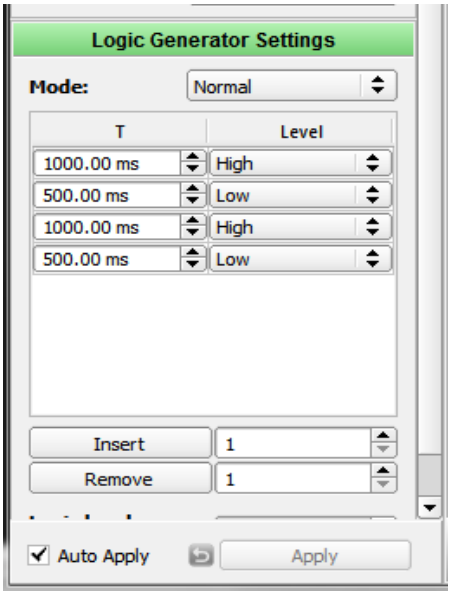

Figure 4. Logic Generator Settings

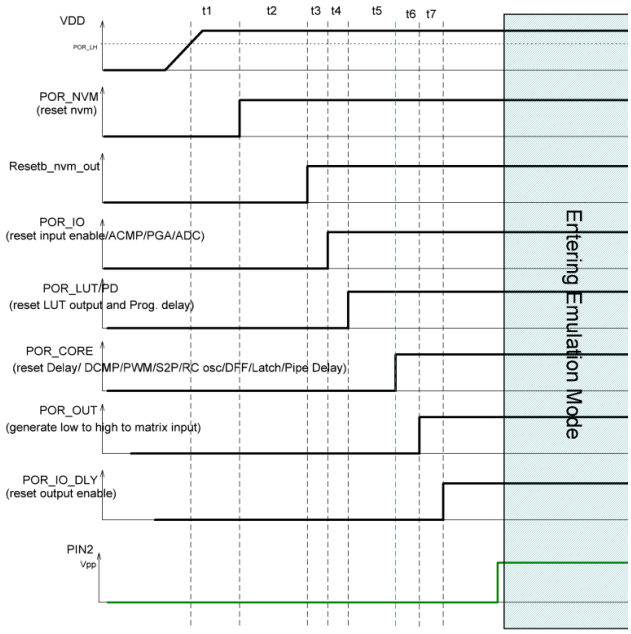

Figure 5. GPAK2 Startup

The waveform in Figure 6 shows both VDD and IN simultaneously rising.

Power-up Sequence on GPAK

The GPAK has a specific power-up sequence for powering each block. The startup sequence is shown in Figure 5. POR_IO, POR_LUT/PD and POR_CORE show the order in which blocks are powered up and enabled. The POR_IO is the first power signal applied to blocks and it enables the IO inputs, ACMP, PGA, and ADC. After those have been powered on, POR_LUT/PD is applied. LUTs will produce their outputs and the Prog delay is powered up. POR_CORE is powered last and includes all other blocks. On power-up, delay blocks pass the input to the output without enforcing any delay. Thus, when a logical HIGH is applied at startup, the delay will not force a delayed signal, but the delay block will immediately output HIGH (Figure 6).

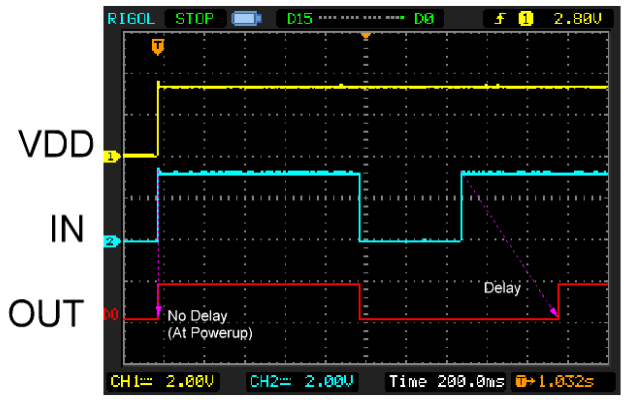

Figure 6. No Startup Logic

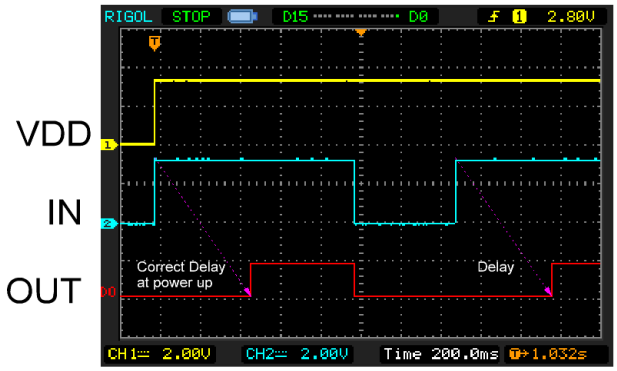

Figure 7. With Startup Logic

Solving the Problem

If the design needed the delay to occur even if IN is HIGH when VDD goes HIGH, you can add a LUT with the POR block to solve the problem. As referenced in Figure 5, the POR signal stays LOW until all other blocks have been powered up.

A LUT added to the input of the Delay block can enforce a LOW signal until the POR signal has been set. Figure 8 contains the new design. 2-bit LUT4 will be configured as an AND gate, which will keep the input to the delay block LOW until POR has been set. Once POR is set, the delay block will enforce delays and work as expected. The waveform of the new design is shown in Figure 7.

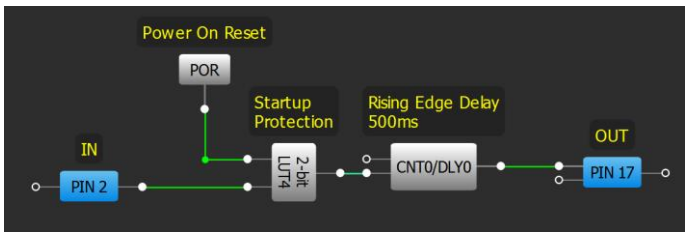

Figure 8. Circuit with Startup Logic

Conclusion

The GPAK Evaluation Board is an effective tool for testing and designing Silego GreenPAK chips. The Test Mode is an essential feature to testing power-up conditions and can be combined with global linkage to see a design's response to different inputs when power is applied.

Related Files

Programming code for **GreenPAK Designer**.

About the Author

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A	Luke Thomas	10/22/2014	New application note

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