AN-1060
GreenPAK Macro Circuit Design: Linear to Exponential Converter

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Introduction

This application note demonstrates how to design a simple linear to exponential voltage converter using a GreenPAK CMIC IC. Exponential properties of this PWM based design can compensate unwanted logarithmic characteristics of various devices.

Linear to Exponential Converter Circuit Design

The screen capture of ADC that controls the PWM can be seen in Figure 4. The ADC is connected to PIN8 which is configured as Analog Input. PWM period is defined by the period of CNT1. The 3-bit LUT0 is configured as MUX. IN+ for the PWM0 is an 8-bit data string that is sourced from ADC. IN- for the PWM0 and DCMP1 is an 8-bit data string that is sourced from CNT1. PWM output duty cycle ranges from 0% to 99.61% and can be determined as: Output Duty Cycle = IN+/256 (IN+ = 0: output duty cycle = 0/256 = 0%; IN+ = 255: output duty cycle = 255/256 = 99.61%).

Note: The PWM block is configurable with two duty cycle range options: 0% to 99.61%, and 0.39% to 100%. This application note uses the first option. The DCMP output is high, when IN+ > IN-.

The counters in GPAK are down counting. So, the first clock cycle of PWM output is 0, since CNT1=255>=ADC Data. To vary the PWM duty cycle from 30% to 100% within 0.7V-1V (30% of the input range), the counter has to count from 255 down to 179 (30% of the input range) with a clock source from CNT2. In contrast, counting from 255 down to 179 (30% of the input range) with a much slower clock(CNT0) causes the Duty Cycle to change from 100% to 30% (70% of the output range). So CNT2 should count 70% of the time from 255 to 179, while CNT0 counts the 30% of the time from 179 to 0. This creates a dual slope exponential approximation of the total range.

$$\begin{cases} 70\%(\text{time}) = (255 - 179) \times \text{CNT2} \\ 30\%(\text{time}) = 179 \times \text{CNT0} \end{cases} \rightarrow$$

$$\frac{\text{CNT2}}{\text{CNT0}} = \frac{70\% \times 179}{30\% \times (255 - 179)} = 5.5$$

As can be seen in Figure 4, output of PWM0 is connected to PIN12. Output Exp is configured to be a 1x Push Pull.

Figure 3 is a timing diagram of the circuit shown in Figure 4.

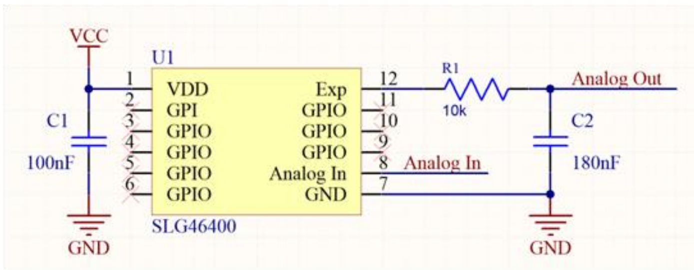

Figure 1. Linear to exponential converter Typical Application Circuit

Linear to Exponential Converter Circuit Analysis

Figure 2 shows the operation of the Linear to Exponential Convertor design.

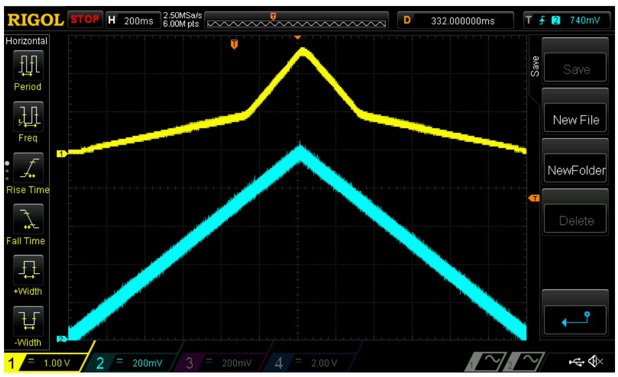

Figure 2. Linear to Exponential Converter Waveform. yellow is "Analog Out" output, blue is PIN8 "Analog In" input

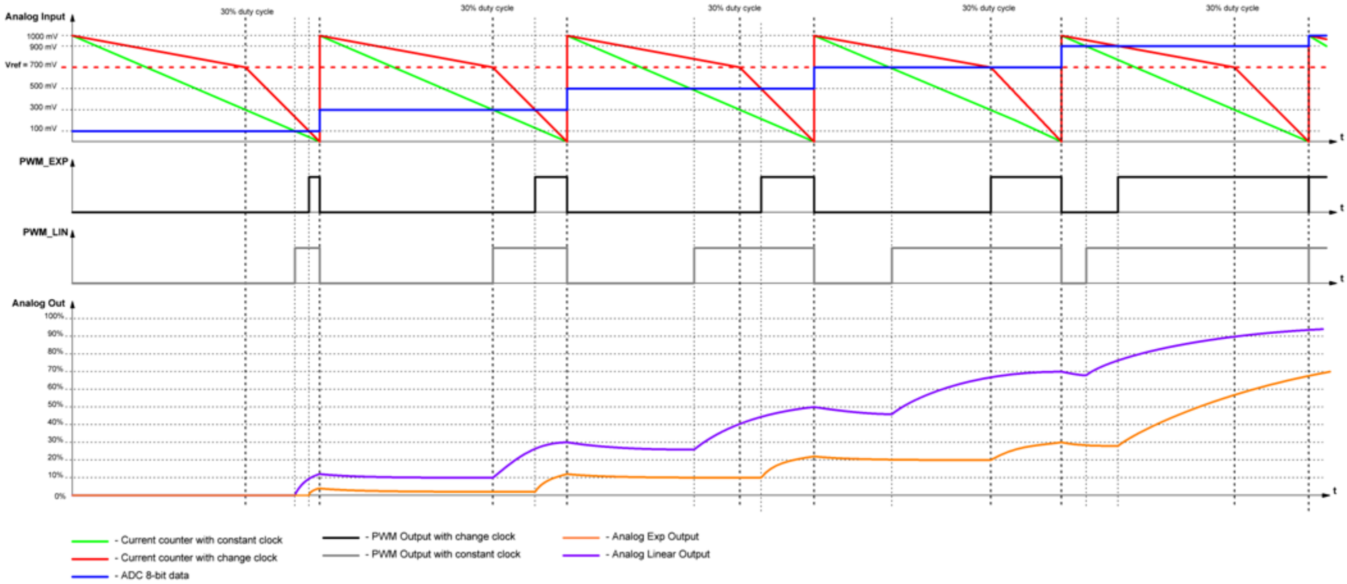

Figure 3. Linear to Exponential Converter Timing Diagram

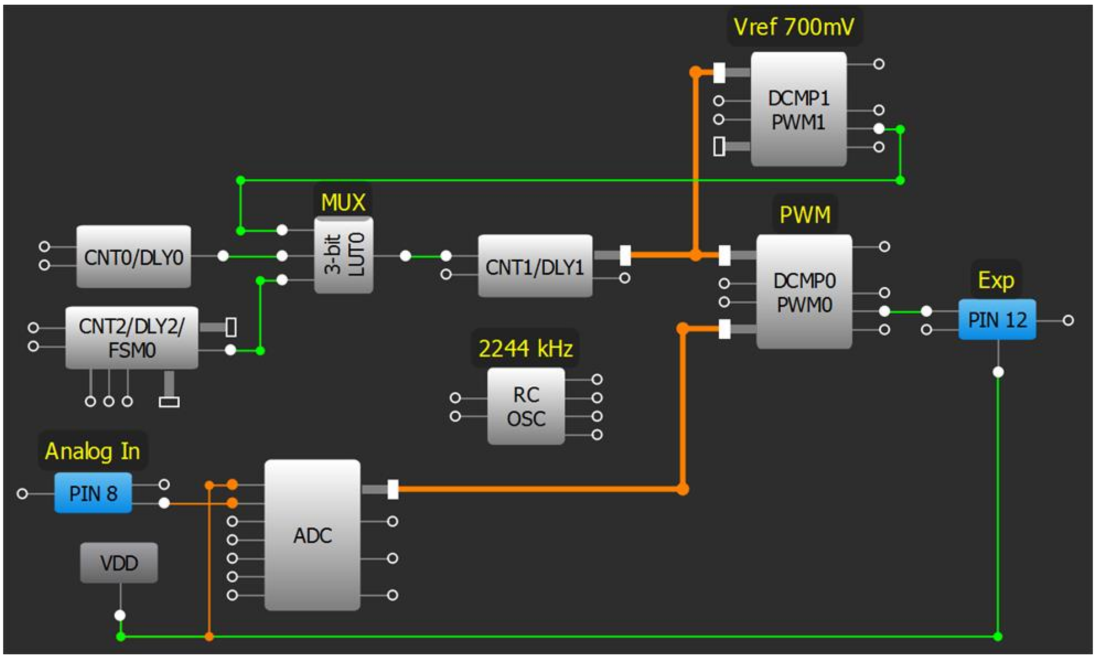

Figure 4. Linear to Exponential Converter Block Diagram

If the Analog input voltage increases from 0 to 0.7V, PIN12 "Exp" output will generate PWM signal with changing duty cycle from 0% to 30% linearly (the Analog Out voltage range is from 0% to 30%).

When the Analog input voltage increases from 0.7 to 1V, PIN12 "Exp" output will generate a PWM signal with duty cycle changing from 30% to 99.61% linearly (the Analog Out voltage range is from 30% to 99.61%).

Conclusion

The converter shown in this application example produces a piecewise linear conversion of input linear voltage to a dual slope exponential approximation of the total range. The combination of R1, C2 acts to filter the PWM digital output into slowly changing voltage which then represents the exponential output. This scheme can be useful for certain sensing, detection, or monitoring circuitry.

Generally, the PWM circuit is a standard block used in many devices and systems. The ease of the use and configurability of this block in GreenPAK CMIC devices makes it ideal for replacing larger, more complex, and costly microcontrollers.

About the Author

Name:	Bogdan Holod
Background:	Bogdan Holod graduated from Lviv Polytechnic National University in 2011 and received a Master's Degree in Radio engineering devices, systems, and complexes. Since 2012 he has been working as a design engineer with experience in low power analog systems, developing digital and analog electronic CMIC circuits, and providing design guidelines.
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Document History

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Revision	Orig. of Change	Submission Date	Description of Change
A	Bogdan Holod	02/06/2015	New application note

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