AN-1056 Macro circuit design ADC PWM

This application note provides a working design example of a PWM using ADC to control the output duty cycle. While this design uses only a fraction of the SLG46620V GreenPAK™ available resources, this example can speed successful completion of more complex designs.

ADC PWM

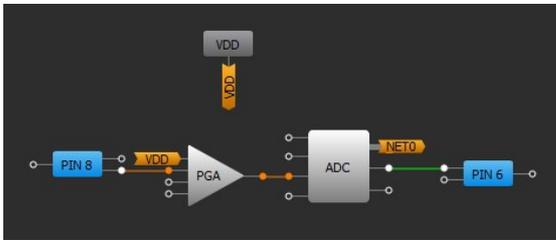Detail ADC operation within the SLG46620V is as follows:

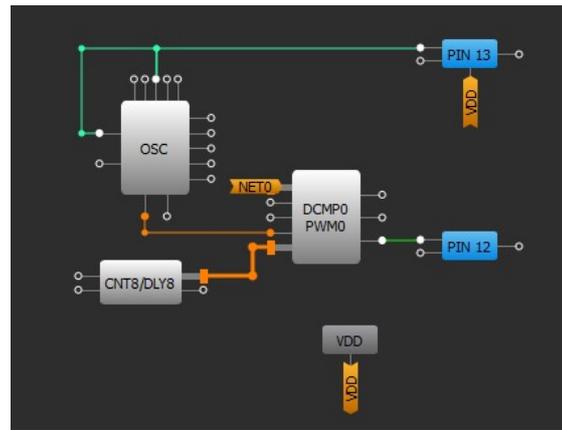Figure 1. ADC block configuration in GreenPAK Designer software

Figure 2. PWM block configuration in GreenPAK Designer software

After ADC power down signal goes LOW, the ADC becomes active and receives clock signals from the Oscillator block. It takes 6 falling edges for the ADC to make a conversion. After that, the ADC outputs 8 bits of serial data (bits change on the falling edge of the clock). Then, parallel data will appear on the 13th clock (rising edge) and will be stored until the next conversion cycle.

On the 16th clock the ADC will output an interrupt signal of 1 clock cycle width. After that a new conversion cycle starts and will continue until the ADC power down signal goes HIGH.

This whole conversion process is summarized by the timing diagram shown in figure 3.

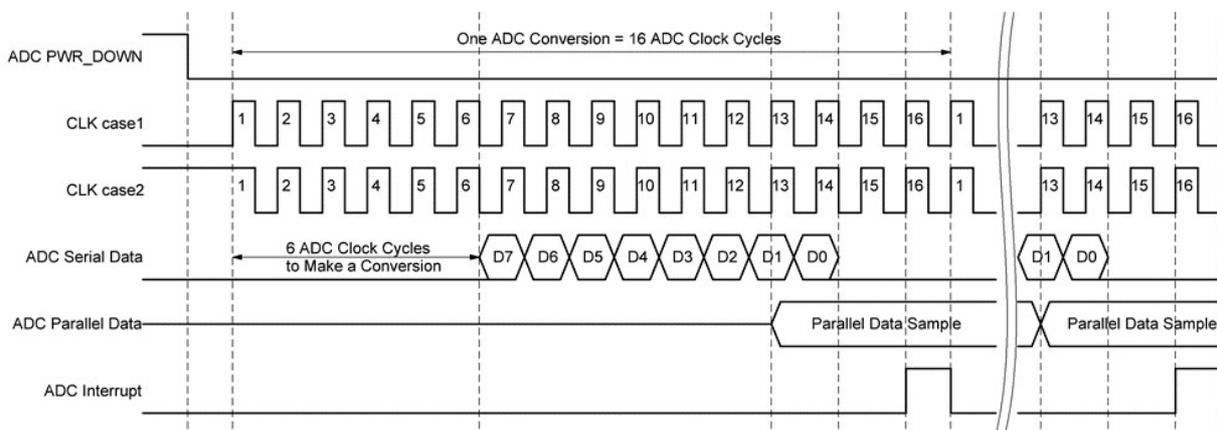Detail of creating the PWM signal is as follows:

Figure 3. ADC operation timing diagram

The PWM generator is similar to a digital comparator except that the data on one of the inputs is cycling and changes linearly. So, to create a PWM signal, we need a PWM ramp source. This is a counter that counts from 255 down to 0 or vice versa. Another source of data for the DCMP/PWM

block should be parallel data that is stable for at least for 1 PWM signal period (PWM ramp counter period). It could be data from SPI, ADC, FSM blocks, or from an internal register. PWM generation is summarized by the timing diagram shown in figure 4.

As can be seen from Figure 4, it takes 1 clock cycle for the DCMP to make a comparison, so the shift of one clock period appears.
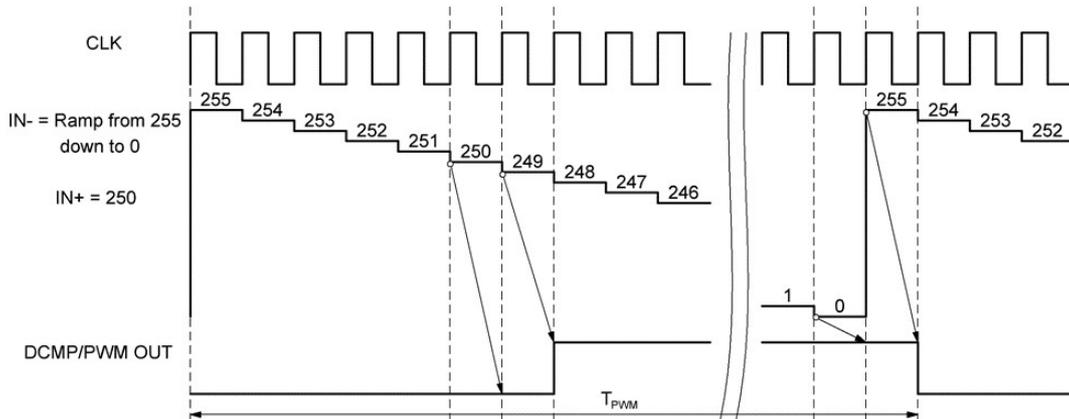

Figure 4. PWM signal formation timing diagram

Summarizing the previous description:

- There are various configurations and combinations of the ADC/PWM design due to a big variety of separate ADC and DCMP/PWM block configuration options.

- The main consideration in building correct ADC/PWM designs is assuring the correct clock synchronization.

To achieve this, proper clock sources should be chosen. Since each block could conceivably be powered on dynamically at different times, synchronization to one clock source should be used. Let's build up a design that will accommodate all the recommendations described. In this example, the PWM generator will be set to its maximum output frequency.

This can be achieved by using the Ring OSC as a clock source for the ADC and DCMP/PWM blocks.

Figure 5 shows the configuration setting of each block used in ADC/PWM circuit. The maximum output PWM frequency is:

$$\frac{F_{RING\_OSC}}{\left(PWM\_Ramp\_Counter\_Data+1\right)}$$
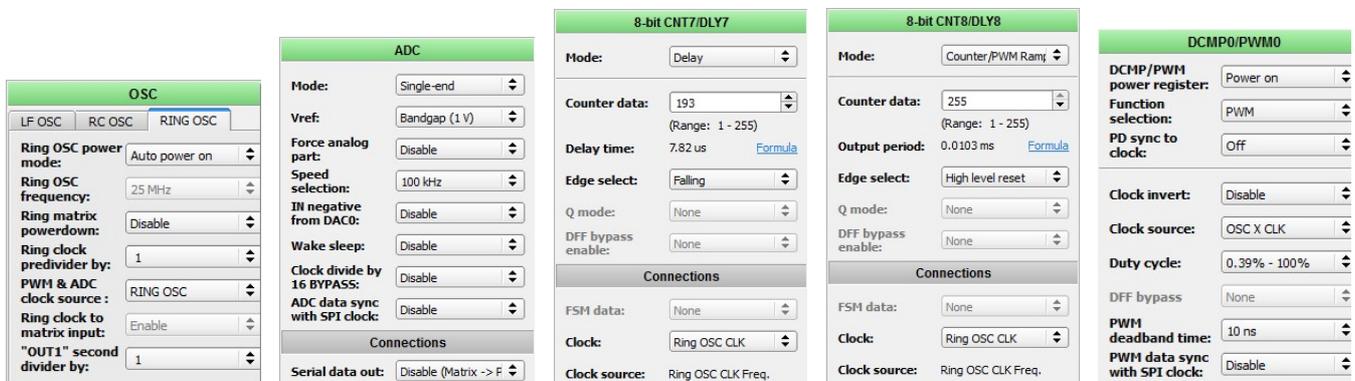
(26MHz/(255+1)≈101kHz).

Figure 5. OSC, ADC, CNT7, CNT8, PWM0 block properties configuration in the GreenPAK Designer software

First, configuring the ADC is straightforward. Turn on the ADC by connecting PWRDN to a LOW signal, or to a PIN to control the ADC operation externally (such as PIN8 configured as an Analog Input). Next, turn on and configure the PWM generator. This is done by turning on the Power register, setting the Function Selection to PWM, set connections configuration of IN+ as ADC[7:0] and IN- of CNT8->Q[7:0]. As for the clock source, the same clock that is used by ADC will be used

in this example (OSC X CLK configuration). The last configuration is to connect CNT8 parallel output to the IN- input of PWM generator.

The next step will be configuring CNT8: set mode to Counter/PWM Ramp, set Counter Data to 255 choose the clock source to Ring OSC (which makes PWM operate at the maximum frequency). The last step is to correctly configure the clock signal source for this application – OSC block. The OSC will produce clocks from its Ring Oscillator. So, the PWM&ADC source should be set to Ring OSC and enable Clock to matrix input of the Ring OSC.

Resolving reset and timing latency

For correct and synchronous PWM operation and to have the first data correct (first PWM period), it needs to be reset. PIN2 is used for the reset and dynamic on/off. When it is HIGH, the ADC, PWM and DLY7 will be turned off. When it is LOW, ADC, PWM and DLY7 will be in normal operation mode. With ADC & PWM dynamically on/off, they must be reset at the off state. DLY7 is used to compensate the startup time (latency) of the ADC, so in this case the Counter Data in it should be "193" (12 ADC clocks * 16 Ring OSC clocks + ~4 Ring OSC clocks for ADC to start up – 3 clocks due to delay structure).

Because the CNT8 is reset to 0, but PWM ramp startups at "255", it has one clock delay from "0" to "255". So, there will be a glitch at the time when ADC & PWM are starting.

Two DFFs have to be added to filter out this glitch. The clock source for these DFFs will be a Ring OSC. The final design configuration is shown in Fig.6.
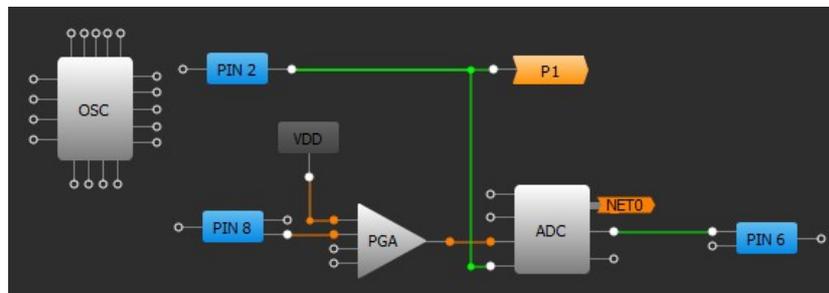

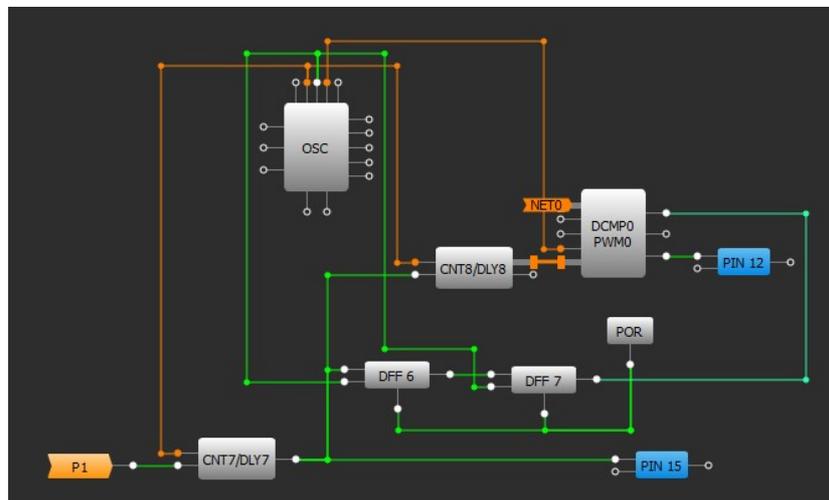Figure 6. Schematic view of Matrix0 pane

Figure 7. Matrix1 pane in the GreenPAK Designer Software

Figure 8. PWM generator turns on   Figure 9. PWM generator turns off

Channel 1 (yellow/top line) – PIN#2
Channel 2 (light blue/2nd line) – PIN#8
Channel 3 (magenta/3rd line) – PIN#6
Channel 4 (blue/bottom line) – PIN#12

Conclusion

The GreenPAK4 SLG46620V IC is a versatile device with many possibilities. Being universal also puts some restrictions on device use. For correct and precise operation of the high speed PWM block in your GreenPAK4 design, one should keep in mind that some additional blocks may be required. The detail presented in this application note is intended to show a working example in order to speed the design process.

About the Author

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Background: Roman Yankevych graduated from Lviv Polytechnic National University in 2009, studying at the Department of Radioelectronic Devices and Systems. He designs with Configurable Mixed Signal ICs (CMICs) and provides engineering support for their application. Additionally, he has over 5yr experience with signal processing in radar and communication systems.

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Files

- AN-1056 Macro circuit design ADC PWM.GP4- (75 KB)
- AN-1056 Macro circuit design ADC PWM.pdf- (567 KB)
- AN-1056.zip- (522 KB)

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