

Introduction

Level Shifters are often used when designing in a mixed supply voltage environment. GreenPAK IC's incorporate a separate configuration for inputs to accommodate some level shifting, namely, the Low Voltage Digital Input (LVDI). It works well, but sometimes a higher frequency of operation is desired from the input stage.

This application note details a High speed level shifter external circuit that is edge triggered.

Circuit example

The LVDI falling edge propagation delay time is typically 700ns, giving a frequency limit of approx. 1.5MHz. Leaving margin for good signal integrity and stable delays, the practical limit is slightly lower than that. For 1MHz or lower, LVDI is simple to use and low power. Higher frequencies require a higher speed level shifter, as follows.

This high speed level shifter circuit consists of an external differentiator along with Digital input with Schmitt trigger (DIST) inside the GreenPAK IC (See Fig. 1 and Fig.2).

If the voltage on Digital input doesn't change, then the voltage on differentiator output is set by the voltage divider from resistors R1 and R2. The R1, R2 ratio is set to the middle of the hysteresis range of the DIST, and represents the steady state value. With a signal edge applied to Digital input, the resulting DIST waveform appears as a voltage spike which then switches the DIST. Because of hysteresis, DIST output remains in the corresponding logic state while the input returns to steady state value. When the signal edge returns back to the opposite polarity, then the opposite differentiated spike will in turn set the DIST logic level. It is necessary to ensure the differentiator output levels will exceed the DIST input thresholds with margin. Characterization data for voltage range of 3.0V to 3.6V and -20C to +85C temperature range is shown in Table 1.

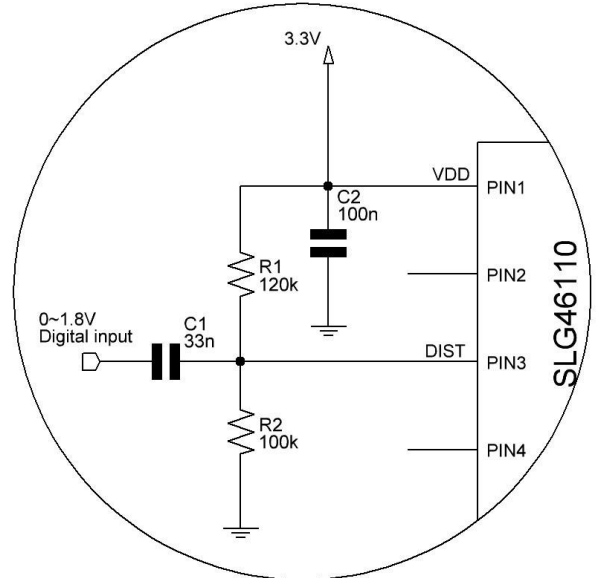


Figure 1. Fast Level Shifter schematic

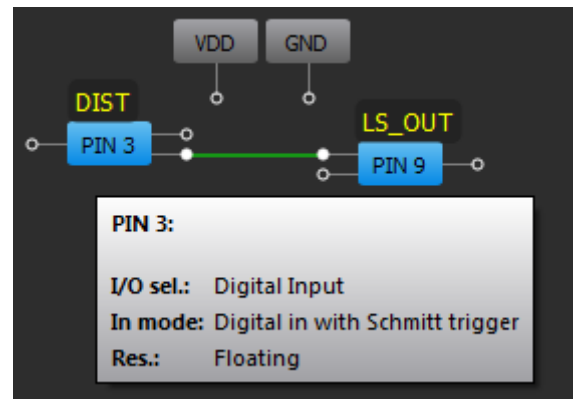


Figure 2. Fast Level Shifter Design

| VDD[V] | 3.0 | 3.3 | 3.6 |
|-------------|-----------|-----------|-----------|
| VIH[mV] | 1608-1748 | 1761-1909 | 1913-2069 |
| VIL[mV] | 987-1085 | 1103-1200 | 1218-1316 |
| VSpmax[mV] | >1748 | >1909 | >2069 |
| VSpmmin[mV] | <987 | <1103 | <1218 |
| VCOM[mV] | 1346.5 | 1480.5 | 1614.5 |
| Vhyst[mV] | 554-729 | 590-767 | 628-812 |

Table 1. DIST characterization data

V_{IH} = DIST HIGH-Level Input Voltage. V_{IL} = DIST LOW-Level Input Voltage. V_{Spmax} = rising spike voltage on differentiator output ($>V_{IH}$). It is necessary for the guaranteed switching of DIST. V_{Spmin} = falling spike voltage on differentiator output ($<V_{IL}$). V_{COM} = steady state DIST input voltage which is set by the divider from resistors R1 and R2. V_{hyst} = hysteresis value of DIST. Based on Table 1, we can calculate the resistor divider ratio and resistor values. Also, the acceptable ramp rate of an input signal which can propagate through the differentiator depends on resistor and capacitor values used (see Figs 16-18).

It is necessary to pay attention to the VDD range and the differentiator input voltage range.

Because of the divider, V_{COM} voltage will be set within the DIST hysteresis range. With this circuit, the minimum input amplitude to the differentiator then becomes $(V_{IH} - V_{IL})/2$ if V_{COM} was perfectly centered. Of course we must allow additional margin to allow for some offset.

As a result, the functionality waveforms of the Fast Level Shifter are shown below for the schematic from Fig.1.

Waveforms definition:

Channel 1 (yellow line) – PIN#1 (VDD)

Channel 2 (light blue line) – Input of differentiator

Channel 3 (magenta line) – PIN#3 (DIST)

Channel 4 (green line) – PIN#9 (LS_OUT)

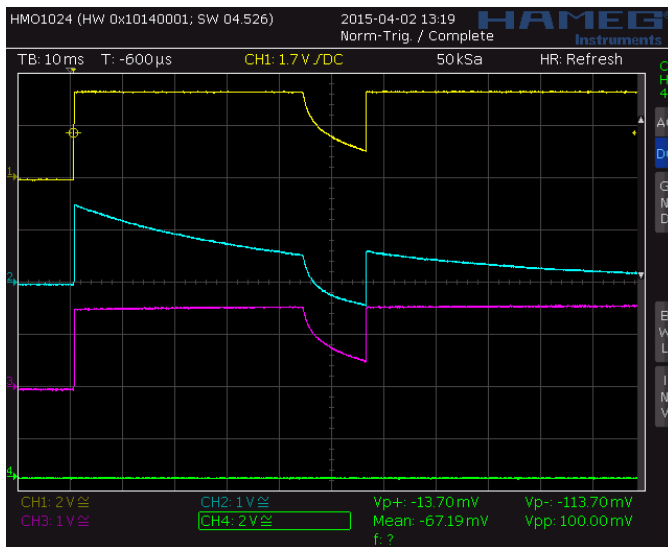


Figure 3. VDD is applied. Differentiator input is in Hi-Z state. LS_OUT remains unchanged. Small timebase

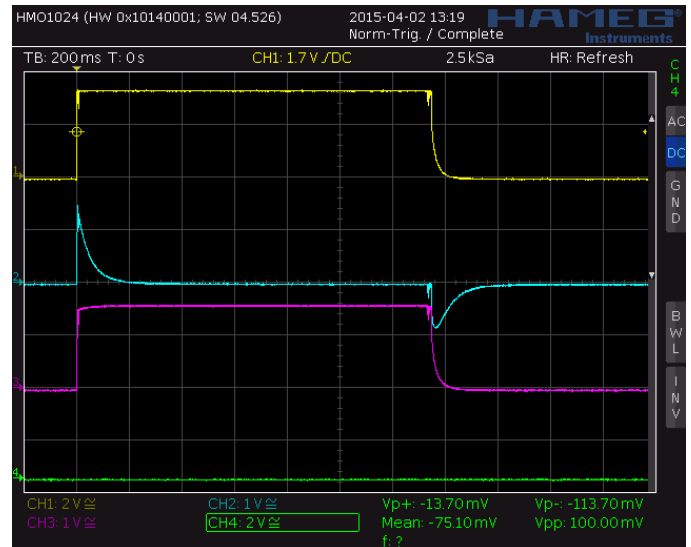


Figure 4 VDD is applied. Differentiator input is in Hi-Z state. LS_OUT remains unchanged. Long timebase

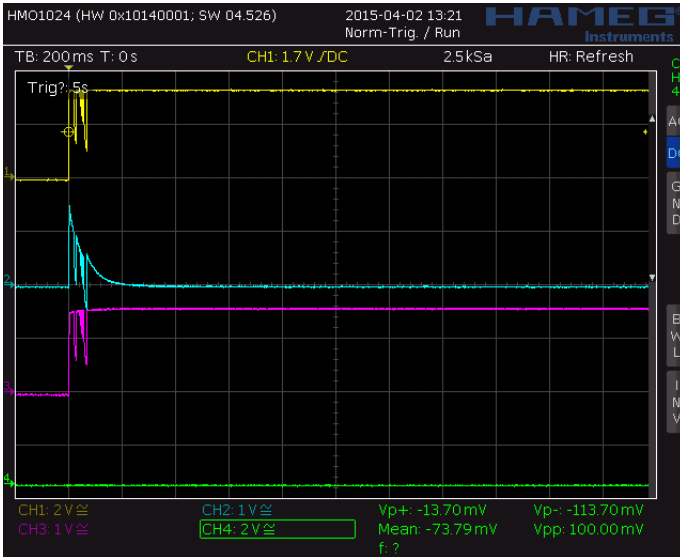


Figure 5. VDD noise. Differentiator input is in Hi-Z state. LS_OUT remains unchanged.

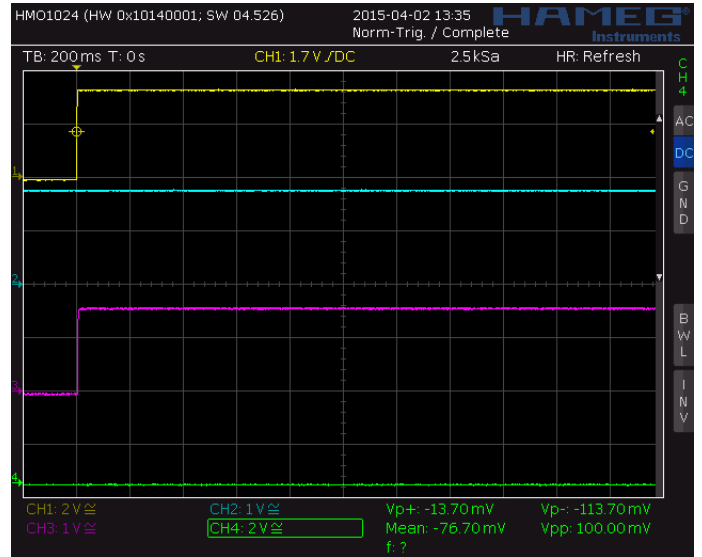


Figure 7. HIGH level on differentiator input comes before VDD. LS_OUT remains LOW

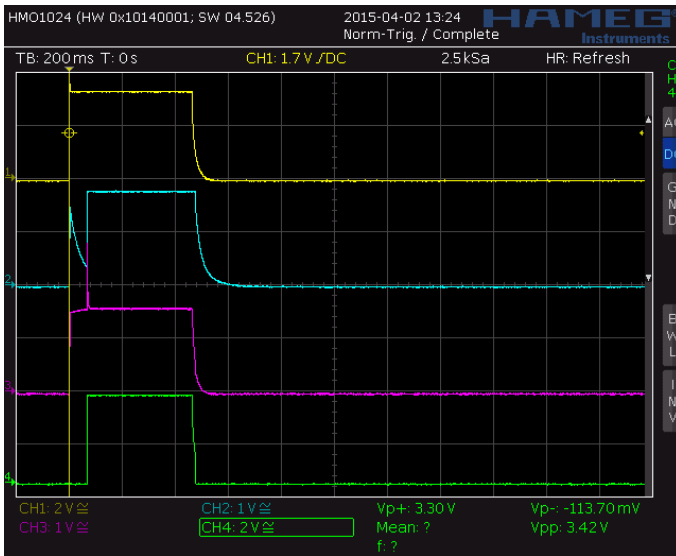


Figure 6. HIGH level on differentiator input comes after VDD. LS_OUT now goes HIGH

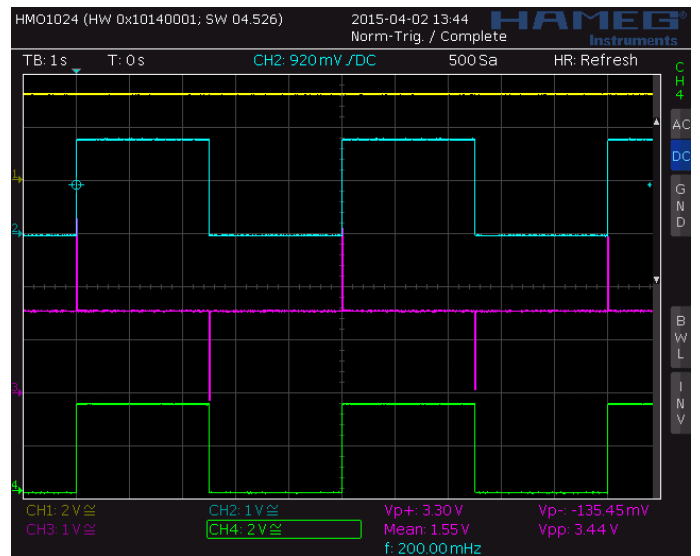


Figure 8. Fast Level Shifter operation. Period of Input signal is 5 seconds

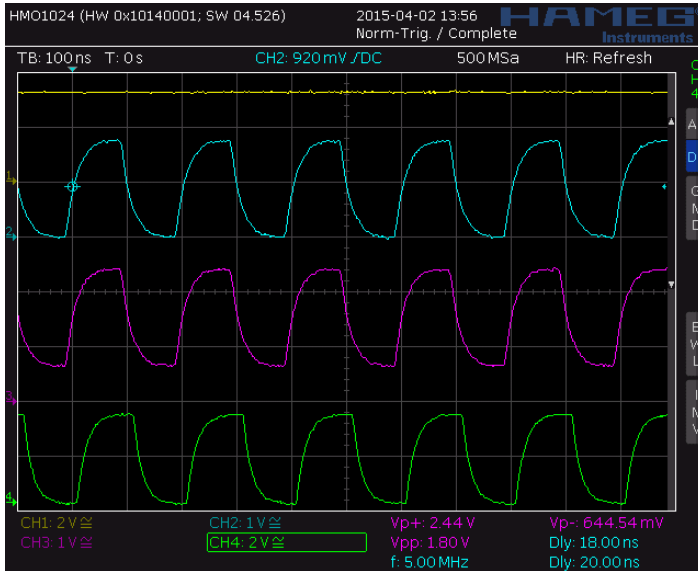


Figure 13. Fast Level Shifter operation. Input signal period is 200 ns (5 MHz). Waveform is limited by oscilloscope probes and parasitic capacitances. Also, pin-to-pin propagation delay influence is visible.

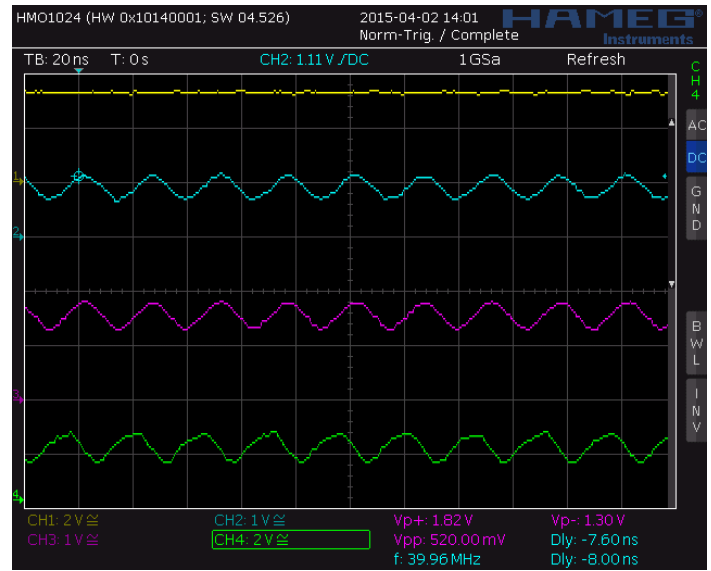


Figure 15. Fast Level Shifter operation. Input signal period is 25 ns. Waveforms are probe bandwidth limited.

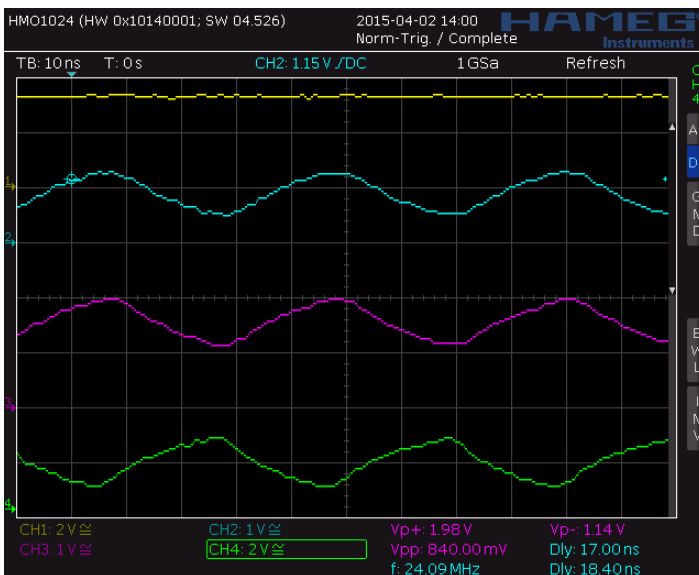


Figure 14. Fast Level Shifter operations. Period of Input signal is 42 ns. Propagation delay time creates effect of phase shift for 180 degrees. The delay time effect is VDD dependent.

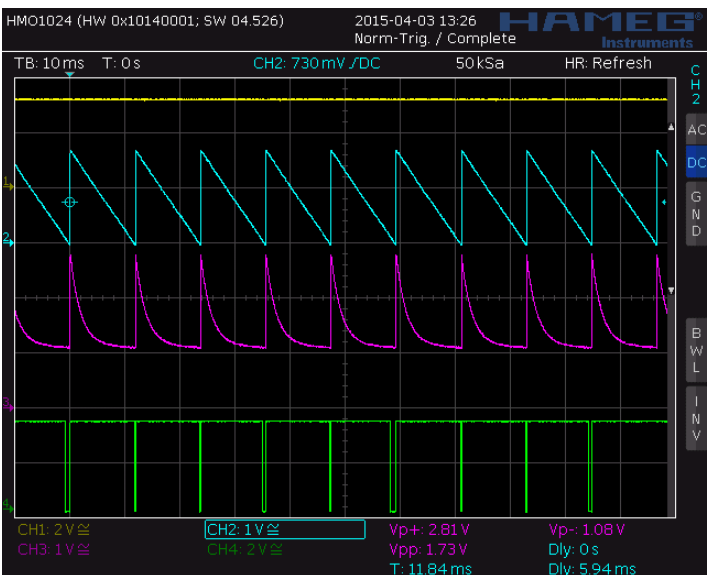


Figure 16. Maximum falling edge ramp rate on differentiator input.

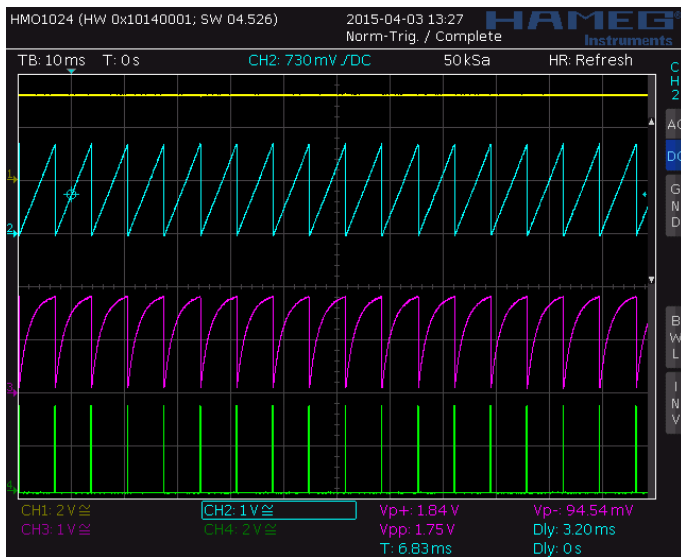


Figure 17. Maximum rising edge ramp rates on differentiator input.

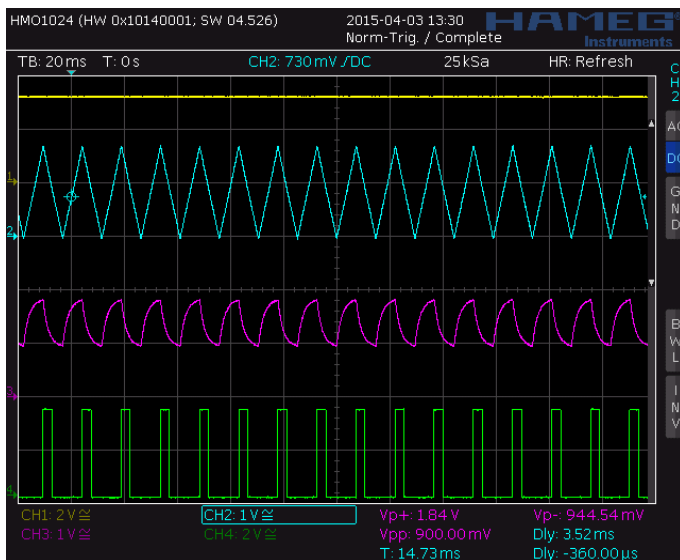


Figure 18. Maximum rising-falling edge ramp rates on differentiator input

The design configuration may be found in Appendix 1. The full schematic of the Fast Level Shifter may be found in Appendix 2.

Conclusion

The Fast Level Shifter can be used as a level shifter in designs where higher frequency of operation is desired. In such cases, it is a good replacement for the usual schematic with the Low Voltage Digital Input. Flexibility and simplicity of this circuit allows use in specific designs that allow edge triggering.



Appendix 1

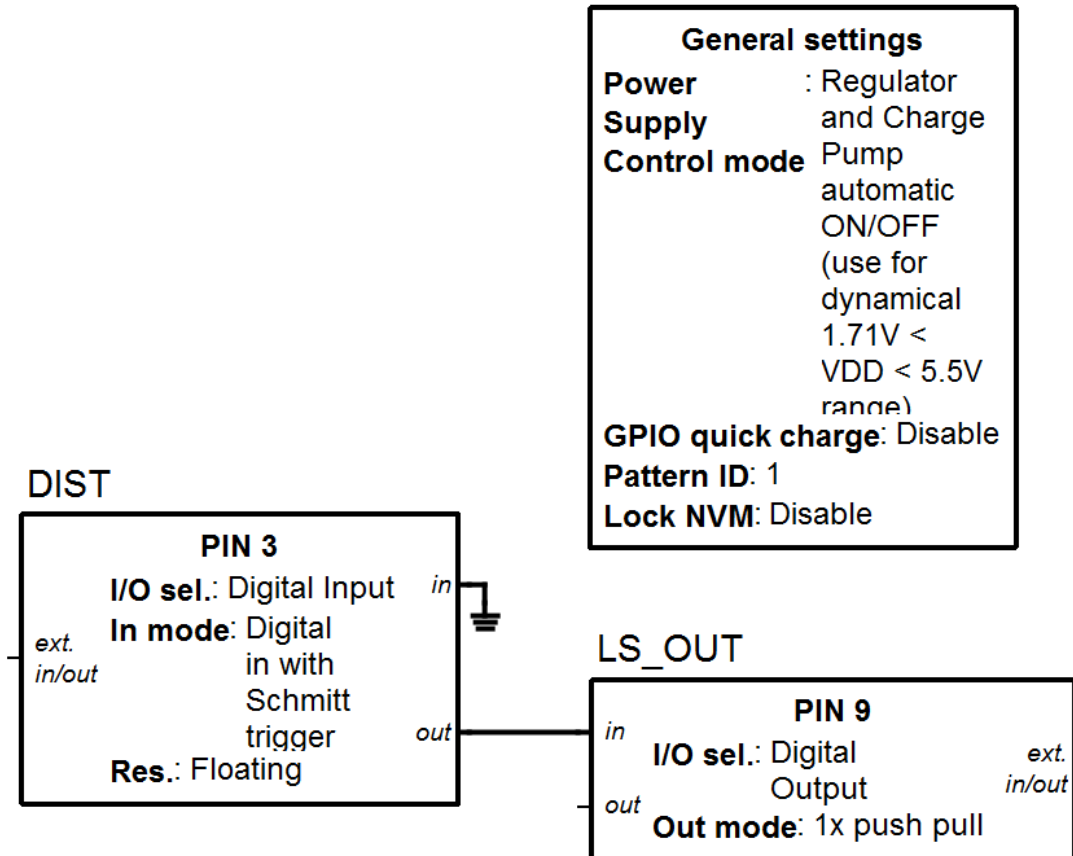
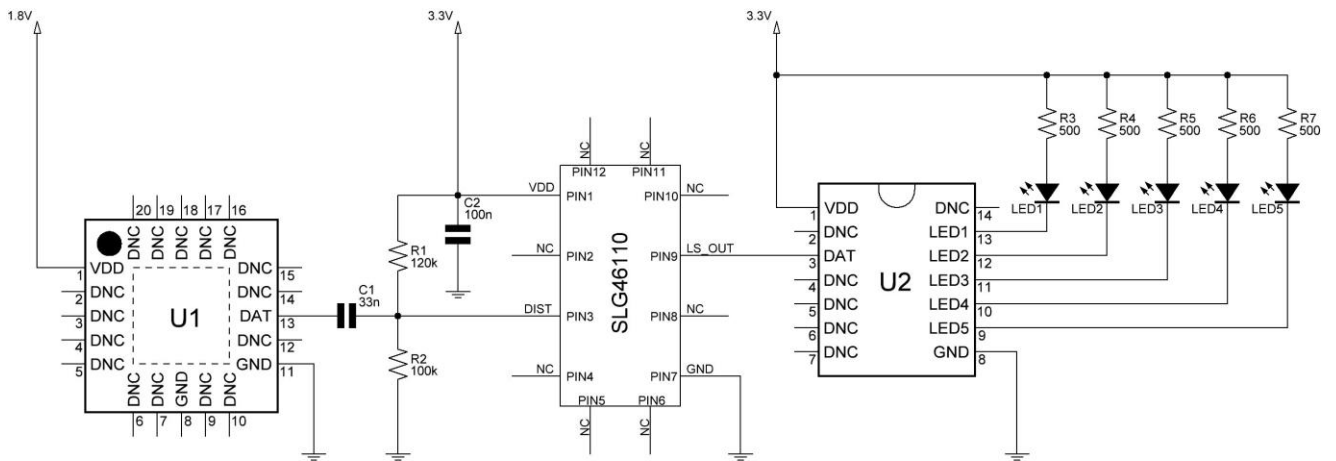


Figure 1.1. Block Diagram for Design

Appendix 2

Figure 2.1. Fast Level Shifter schematic



About the Author

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Background: Serhiy Prykhodko joined Silego in 2012, working as a design engineer with experience in low power analog systems, developing digital and analog custom CMIC circuits, and providing design guidelines. Prior to that he designed high reliability and secure smart home systems at Melask and Cenitec.

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|----------|------------------|-----------------|-----------------------|
| A | Serhiy Prykhodko | 04/09/2015 | New application note |

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