POR Operation in GreenPAK IC's

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Introduction

All Silego GreenPAK IC's incorporate power-on reset (POR) blocks to ensure correct device initialization and internal cells operation. Quite often, user designs can be sensitive to power up timing and the state of pins. This application note details the GreenPAK POR block and chip behavior during power up. With this description, the user can create robust designs more quickly.

GreenPAK general operation

The GreenPAK IC is guaranteed to be powered down and nonoperational when the VDD voltage (voltage on PIN1) is less than 0.6V, (but > -0.6V). Another requirement for the IC to be truly powered down is that no PIN has a voltage greater than VDD applied to it. For example, if VDD voltage is 0.3V, applying more than 0.3V to any other PIN can lead to incorrect behavior. (see Note 1)

Note 1. While the ESD protection diode to VDD does have a 0.6V forward voltage, it still has some small leakage current below 0.6V.

To initiate the power up sequence of the GreenPAK IC, the voltage applied to VDD should be higher than the Power_ON threshold (see Note 2). The full operational VDD range for GreenPAK IC's is 1.71V – 5.5V (1.8V ±5% - 5V±10%). The VDD voltage should ramp up to full operating voltage, but the power up sequence will actually start earlier, after crossing Power_ON threshold. After the power up sequence has started, the GreenPAK IC will be ready and completely operational after 0.5ms (typical).

Note 2. The Power_ON threshold can vary by PVT, but typically it is 1.3V.

To power down the IC, the VDD voltage should be lower than the Power_ON threshold, and to guarantee power down it should be less than 0.6V.

When the IC is powered down, or during power up sequence, POR sets all PINs to high impedance state. After the IC has powered up, the PIN's state is defined by the design programmed or emulated into the IC. It was mentioned before that no PIN has a voltage greater than VDD applied to it. This also applies when the IC is fully powered up.

Part Number	Power_ON Threshold, V	Power Up Time, µs	Power_OFF Threshold,V
SLG46110	1.35	270	0.92
SLG46120	1.35	310	0.92
SLG46721	1.35	300	0.95
SLG46722	1.35	295	0.95
SLG46140	1.3	870	1.1
SLG46620	1.3	1400	1.1

Table 1. Power_ON and Power_OFF Thresholds

POR Sequence

The POR system generates a sequence of signals that enables certain blocks. The sequence itself is shown in Fig.1.

As can be seen from Fig.1, after VDD has started ramping up and crossed Power_ON threshold, then NVM is reset. After that, the IC reads the data from NVM and configures its blocks. The third step is to reset input pins and enable them. After that, LUT's are reset and become active. After the LUT's, the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all blocks are initialized does the internal POR signal (POR block output) go from LOW to HIGH. The last step of initialization is enabling the output PIN's.

The entire chip initialization process takes 0.5ms typical, and depends on many factors such as: VDD slew rate, VDD value, temperature, and chip to chip variation (process variation).

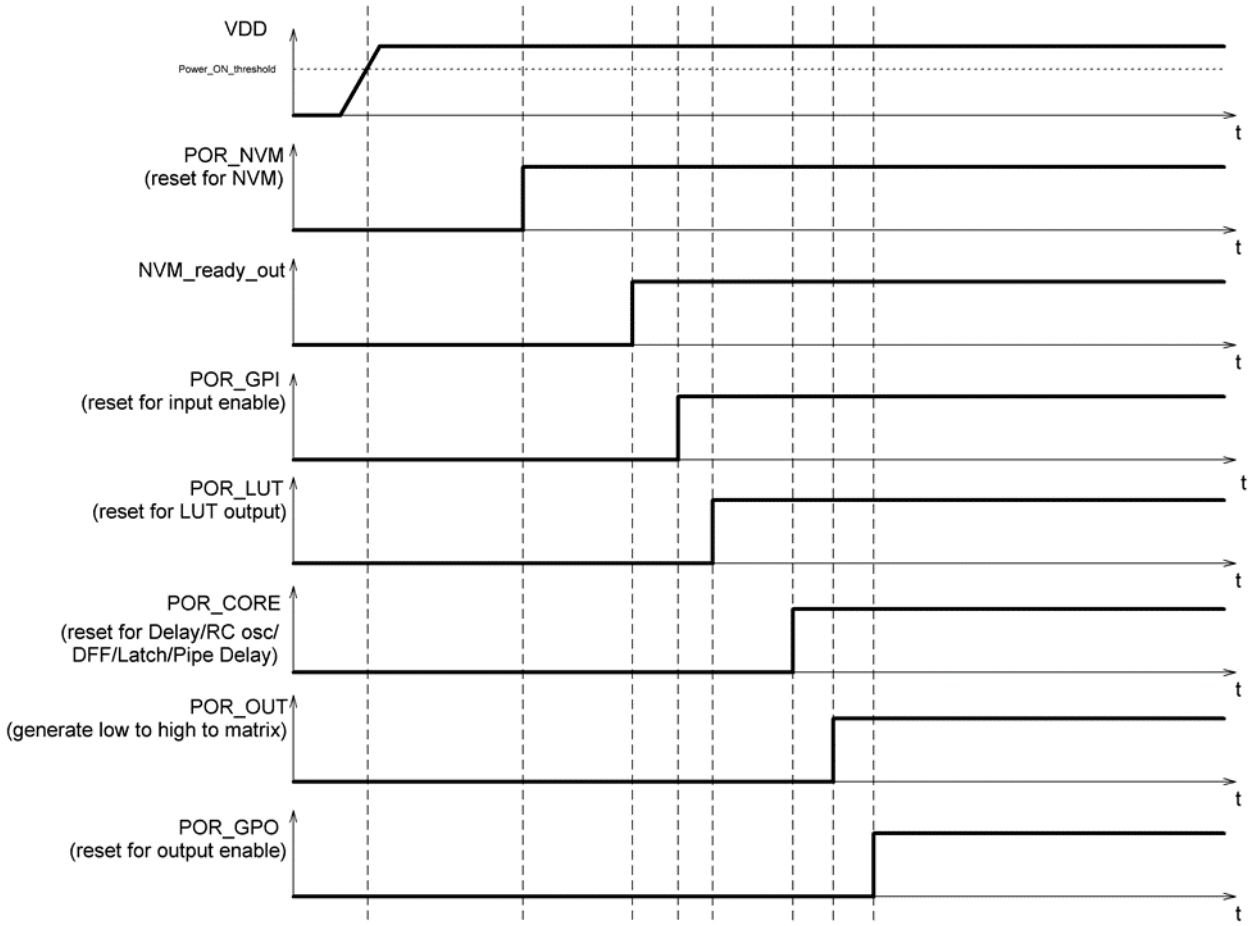

Fig.1. POR Sequence

Blocks Output States during POR Sequence

In a further description of the GreenPAK IC operation during power up and POR sequence, let's overview the blocks output states during the POR sequence. (Fig.2 describes the output signals states).

Before the NVM has been reset, all internal blocks output states are logic LOW (except the output PINs which are tri-stated). Next the NVM initializes. Until the NVM is completely initialized and reset, all blocks output states are still unsettled (except the output PINs which are tri-stated). So next in the sequence: input pins output state set to LOW; LUT's outputs set to LOW. (Only P DLY block configured as edge detector becomes active at this time).

After that, the input PINs are enabled. Next, only the LUT's are configured. After that, all other blocks are initialized. After the internal blocks are initialized, POR matrix signal switches from LOW to HIGH. Last to be released are output PINs that become active and output states are determined by all the preceding input signals.

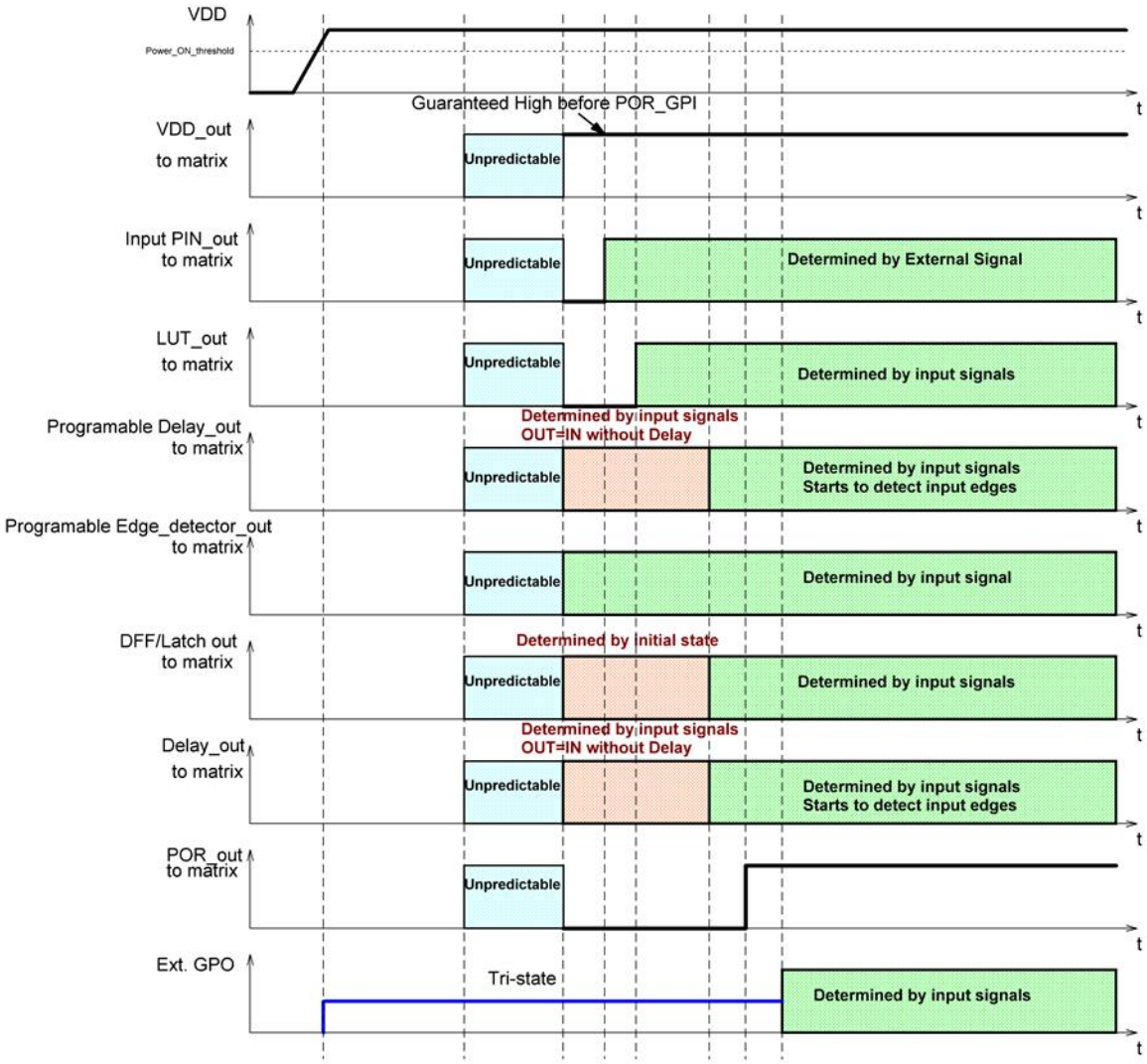

Fig. 2. Internal Blocks States during POR Sequence

Conclusion

A detailed understanding of the GreenPAK POR sequence and internal blocks output states has been presented. It is intended to avoid common design pitfalls, and speed the construction of user designs that are robust.

About the Author

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Background: Roman Yankevych graduated from Lviv Polytechnic National University in 2009, studying at the Department of Radioelectronic Devices and Systems. He designs with Configurable Mixed Signal ICs (CMICs) and provides engineering support for their application. Additionally he has over 5yr experience with signal processing in radar and communication systems.

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A	Roman Yankevych	02/24/2015	New application note

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