Introduction

This circuit can be used when it is desired to stretch an input pulse width. The resulting output pulse duration is determined by multiplying an oscillator pulse width by a fixed multiplier Tout=Tin*N, where N – integer, which can be set by the user in the configuration parameters.

Pulse Width stretcher circuit design

An external input pulse is applied to Pin2. CNTR2 is used to set the output signal and it is able to count up or down and to be reset with a HIGH-level signal. CNTR3 provides the RC OSC frequency division.

CNTR3 Data determines the multiplication factor of output pulse duration. Pin10 provides the stretched pulse output.

Schematic and configuration settings are shown in figures 1-6.

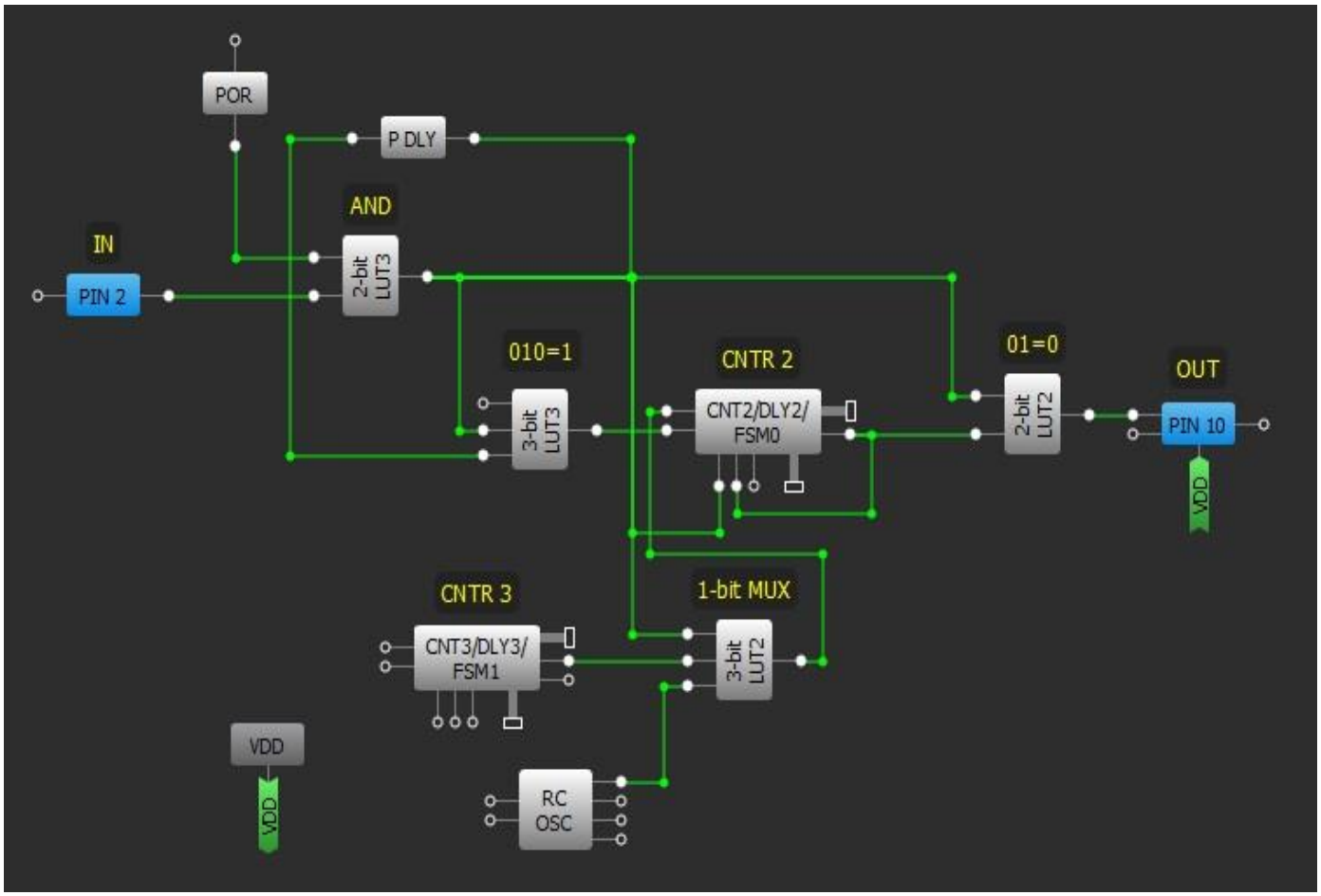

Figure 1. Pulse Width Stretcher circuit

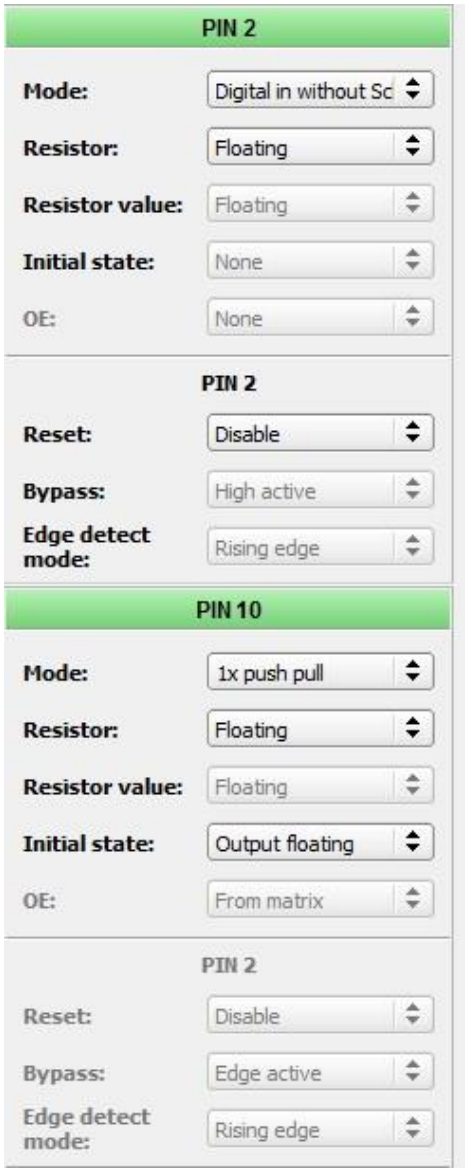

Figure 2. Pin2 and Pin10 properties

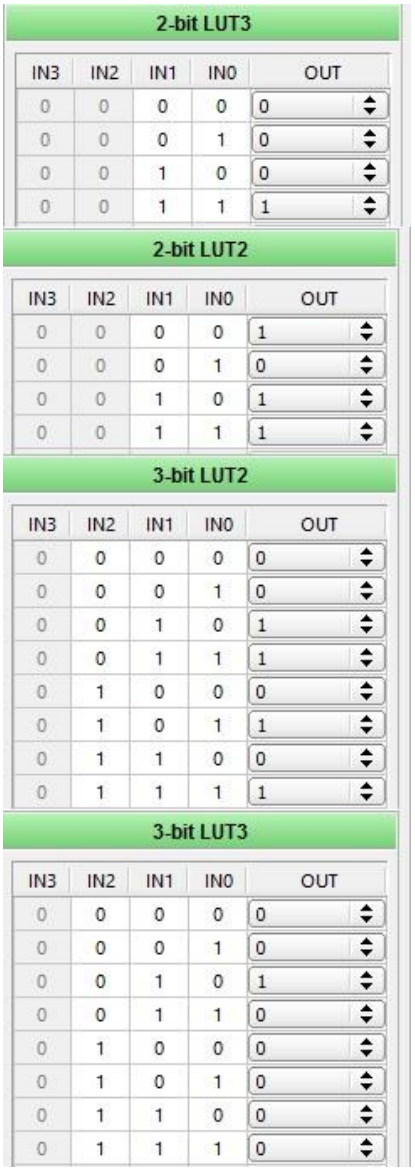

Figure 3. LUTs properties

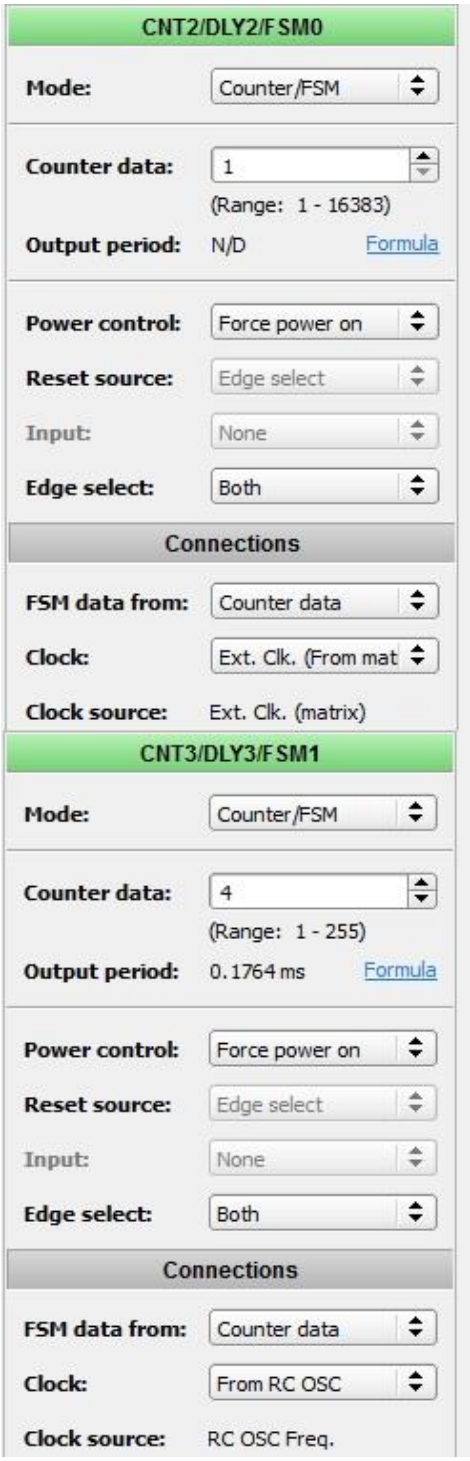

Figure 4. CNTRs properties

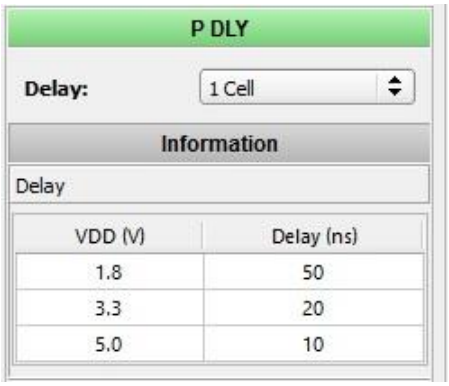

Figure 5. PDly properties

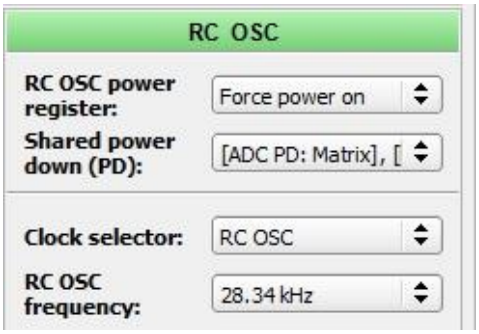

Figure 6. RC OSC properties

Pulse Width Stretcher circuit analysis

2-bit LUT3 IN1 is connected to the POR block, IN0 – to Pin2, which provides the input pulse to other blocks when chip is completely powered on (preventing incorrect output while the chip is still powering up).

CNTR2 is an UP/DOWN counter with UP count when UP/DOWN input is HIGH, and DOWN count when UP/DOWN input is LOW.

Using a 1-bit MUX (constructed with 3-bit LUT2) changing the CNT2 CLK frequency is possible. When input is HIGH, CNT2 CLK frequency = RC OSC frequency; when input is LOW, CNT2 CLK frequency is divided by the (CNT3 Data +1) value.

As soon as CNT2 finishes counting, a pulse on its output will appear, which is directly fed into CNT2 KEEP input, which keeps the high level on its output. This high level won`t change until the reset pulse comes. The reset pulse is generated by rising edge detector, created using 3-bit LUT3 and PDLY block.

There are 4 timing cases to consider:

1) Tmin<Tin<Tmax – normal mode;
2) Tin>Tmax;
3) Tin<Tmin;
4) Input pulse period is less than output pulse duration.

In each case the output pulse duration will be counted using different formulas.

Tmin and Tmax values are determined by RC OSC frequency and CNT2 bitrate.

Tmin = 1/Fosc

Tmax = 2^{14}/Fosc

First case

If Fosc = 28,34 kHz, then

Tmin = 35us;

Tmax = 578ms;

Tin = 10ms;

CNT3 Data = 5;

In this case

Tout = Tin × (CNT3 Data + 2).

Tout = 10ms × (5+2) = 70ms;

Second case

If Fosc = 8196,09 kHz, then

Tmin = 0.13us;

Tmax = 2ms;

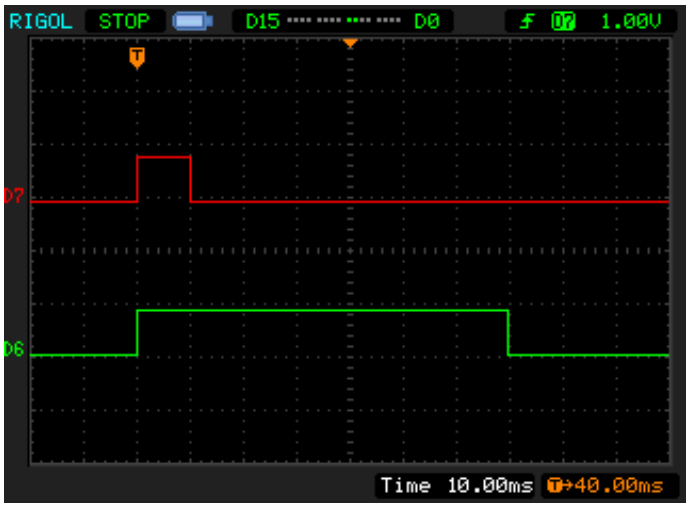

Figure 7. Pulse stretcher functional diagram (First case)

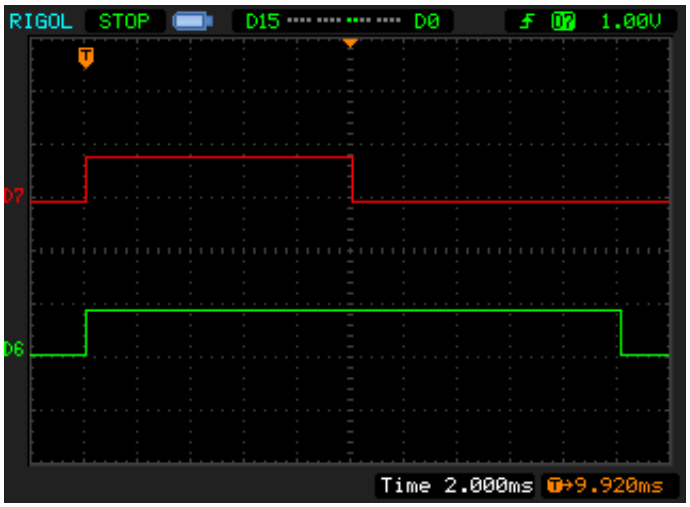

Figure 8. Pulse stretcher functional diagram (Second case)

Tin = 10ms;

CNT3 Data = 4;

Tout = Tin + CNT2 bitrate × (CNT3 Data + 1) / Fosc.

Tout = 10ms+16384 ×(4+1)/8196,09kHz = 20ms;

Third case

If Fosc = 28,34 kHz and CLOCK/12 output is used instead of RS OSC output, then

Tmin = 423us;

Tmax = 6.9s;

Tin = 100us;

Tout = Tin.

Fourth case

If Fosc = 28,34 kHz,

Tin = 10ms;

CNT3 Data = 3;

Tout had to be 50ms, but input pulses period is 30ms;

In this case the output pulse duration can be counted using the next formula:

$$T_{out} = T \times (N-1) + T_{in} \times (CNT3\ Data + 2),$$

where T – input pulses period, N – number of pulses.

Tout = 30ms × (2-1)+10ms × (3+2) = 80ms.

Conclusion

A simple pulse stretcher can be implemented within the SLG46400 IC and is easily modifiable by use of a multiplier setting.

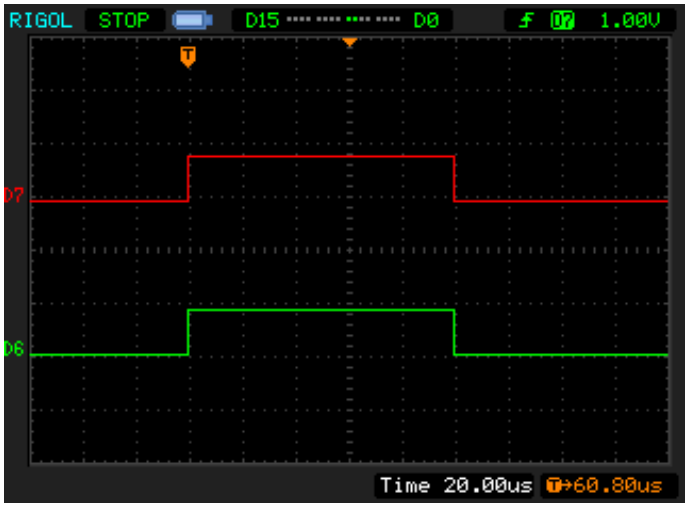

Figure 9. Pulse stretcher functional diagram (Third case)

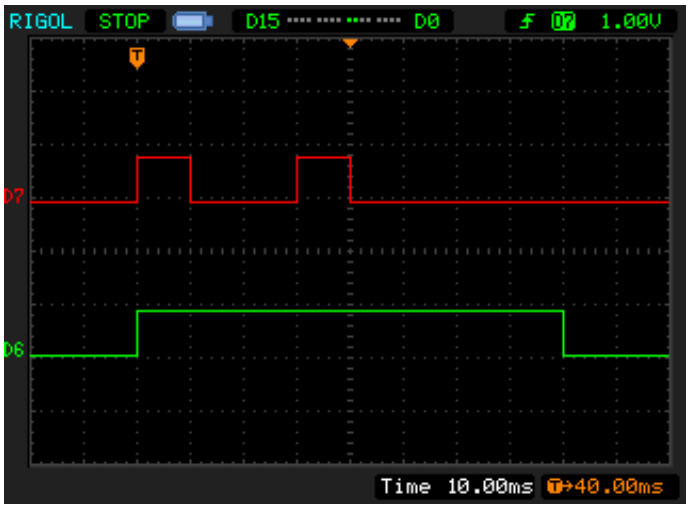

Figure 10. Pulse stretcher functional diagram (Fourth case)

About the Author

Name: Yurii Shchebel

Background: Yurii Shchebel graduated from Ivan Franko Lviv National University in 2015, studying at the Department Electronics. Presently he is working with Configurable Mixed Signal ICs (CMICs) and their applications. He has additional interest designing audiophile grade amplifiers.

Contact: **appnotes@silego.com**

Document History

Document Title: Pulse Width Stretcher

Document Number: AN-1064

Revision	Orig. of Change	Submission Date	Description of Change
A	Yurii Shchebel	4/20/2015	New application note

Worldwide Sales and Design Support

Silego Technology maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at **Silego Locations**.

About Silego Technology

Silego Technology, Inc. is a fabless semiconductor company headquartered in Santa Clara, California, with operations in Taiwan, and additional design/technology centers in China, Korea and Ukraine.

SILEGO TECHNOLOGY

Silego Technology Inc.
1715 Wyatt Drive
Santa Clara, CA 95054

Phone : 408-327-8800
Fax : 408-988-3800
Website : ww.silego.com