Delay cell calculations for GreenPAK3 CMIC's

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Introduction

When using a delay cell in a GreenPAK design, one must consider the accuracy of the delay cell. This is because the GreenPAK IC delay time depends on the clock frequency and counter data. If the counter data is a fixed value, the clock frequency can vary, especially if internal RC OSC is used. That is why the accuracy of the delay cell is determined by the OSC inaccuracy. This application note offers a way to calculate the accuracy of the delay cell in a GreenPAK3 IC in different cases such as: 25kHz or 2MHz RC OSC used, different VDD voltages or ranges, different temperatures, different combinations of the delay cells connections.

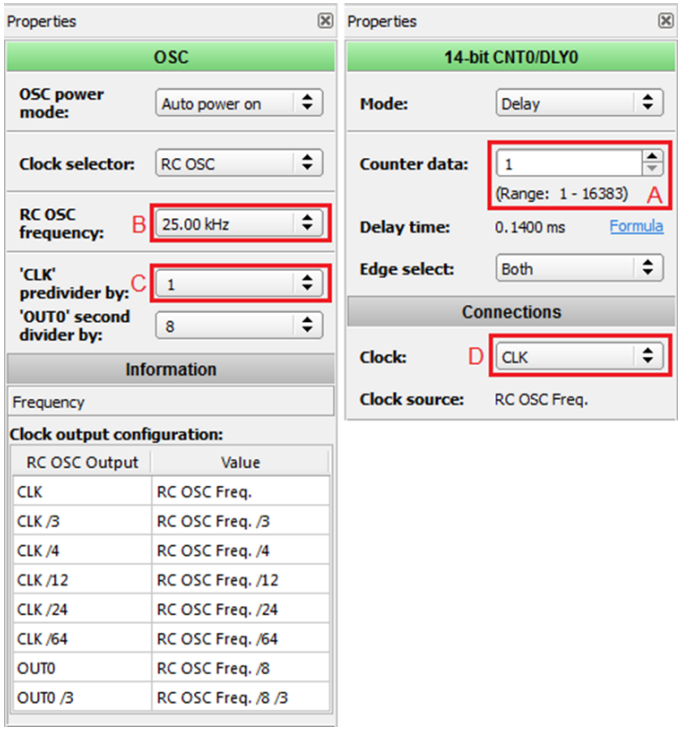

Fig.1. View of OSC and Delay blocks properties windows for SLG46721 in GreenPAK Designer

25kHz RC OSC Frequency Setting

A 25kHz RC OSC setting is the most stable and accurate setting within the GreenPAK3 family IC's. This setting is most common in GreenPAK designs, and is why understanding how to calculate the best accuracy for this setting is crucial.

In the case where separate delays are used and RC OSC is not active before the delay operation, the functional waveforms are shown in Fig. 2a. In the case where this is the first delay in a series connection of delays, the functional waveforms are shown in Fig. 2b.

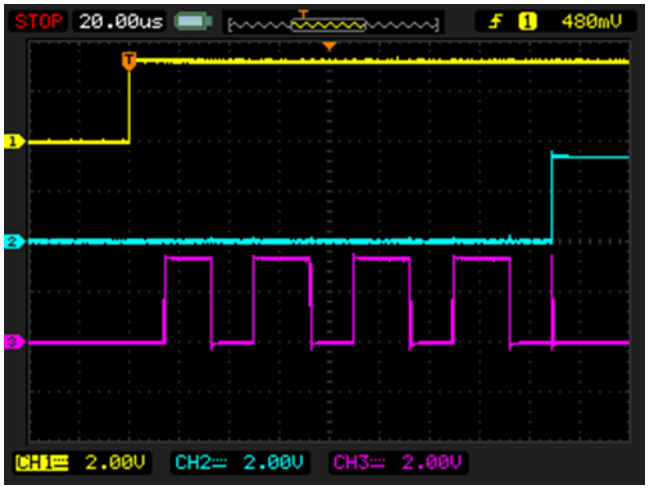

Fig. 2a. Separate delay

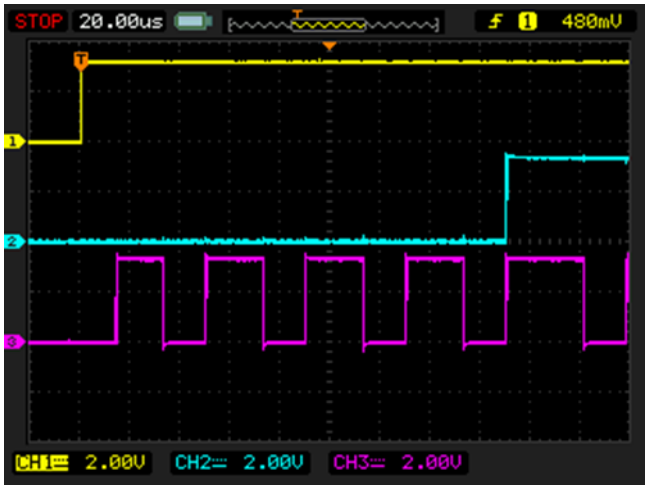

Fig. 2b. First delay in a series of delays

Calculation of the delay timing can be made using the following formulas:

$$T_{\min} = \frac{Counter\_Data + 2}{\frac{F_{osc}}{pre\_div \cdot clk\_div} \cdot (1 + \mathrm{var}_{\max})}$$

$$T_{typ} = \frac{Counter\_Data + 2.5}{\frac{F_{osc}}{pre\_div \cdot clk\_div}}$$

$$T_{\max} = \frac{Counter\_Data + 3}{\frac{F_{osc}}{pre\_div \cdot clk\_div} \cdot (1 + \mathrm{var}_{\min})}$$

Description of variables:

$T_{\min}$ – minimum delay time;

T_{typ} – typical delay time;

$T_{\max}$ – maximum delay time;

$Counter\_Data$ – Counter data value of the delay cell (mark A on Fig.1);

F_{osc} – oscillator frequency, in this case it is a 25kHz (mark B on Fig.1);

pre_div – oscillator predivider (mark C on Fig.1);

clk_div – delay clock predivider (mark D on Fig.1);

$\mathrm{var}_{\max}$ – maximum value of the variable that depends on VDD voltage, temperature;

$\mathrm{var}_{\min}$ – minimum value of the variable that depends on VDD voltage, temperature.

Parameter	SLG46110/SLG46120		SLG46721/SLG46722		Conditions
	Min	Max	Min	Max	
RC OSC trim error	-2.5%	2.5%	-2.5%	2.5%	None
RC OSC variation with VDD	-0.95%	1.52%	-1.51%	1.37%	1.8V[1]
	-0.23%	0.16%	-0.26%	0.23%	3.3V[2]
	-0.91%	0.36%	-0.49%	0.64%	5V[3]
RC OSC variation with temperature	-11.5%	6.15%	-11.5%	6.15%	-20C - +45C
	-11.5%	9.09%	-11.5%	9.09%	-20C - +70C
	-14.88%	11.5%	-14.88%	11.5%	-40C - +85C
	-6.3%	9.2%	-6.3%	9.2%	0C - +70C
	-6.3%	10.9%	-6.3%	10.9%	0C - +80C
	-10.3%	10.9%	-10.3%	10.9%	-20C - +80C

Table 1. GreenPAK3 Additional variation tolerance (25kHz Frequency Option)

[1] means that chip is trimmed at VDD=1.8V and VDD operation range is 1.71V to 1.89V

[2] means that chip is trimmed at VDD=3.3V and VDD operation range is 3V to 3.6V

[3] means that chip is trimmed at VDD=5V and VDD operation range is 4.5V to 5.5V

var_{max} and var_{min} consist of the following components:

RC OSC trim error;

RC OSC variation with VDD;

RC OSC variation with temperature;

Settling time with 25kHz option is not considered as this time is too small compared to the minimum possible delay time.

By summing all chosen min or max error values we get var_{min} or var_{max} that can be substituted into the formulas.

If the delay cell is inside the series connection of delay cells and it is not the first one (as shown in Fig.3), the delay time calculation will be different. Such a connection is very frequently used in power rail sequencing designs. Fig.4 shows the resulting delay time waveforms where the first cell has a shorter delay time than an inside one, even though their settings are the same.

Visible in Fig.4 is the additional RC OSC clock latency for the inside delays connection. Therefore, the following formulas should be used for min, max and typical delay times calculation.

$$T_{min} = \frac{Counter\_Data + 2 + N_{var}}{\frac{F_{osc}}{pre\_div \cdot clk\_div}} \cdot (1 + var_{max})$$

$$T_{typ} = \frac{Counter\_Data + 2.5 + N_{var}}{\frac{F_{osc}}{pre\_div \cdot clk\_div}}$$

$$T_{max} = \frac{Counter\_Data + 3 + N_{var}}{\frac{F_{osc}}{pre\_div \cdot clk\_div}} \cdot (1 + var_{min})$$

where var_{min} and var_{max} parameters are calculated in the same way as for the previous formulas.

N_{var} – additional delay variable that appears in the case of inside delays connection. $N_{var} = 0..1$.

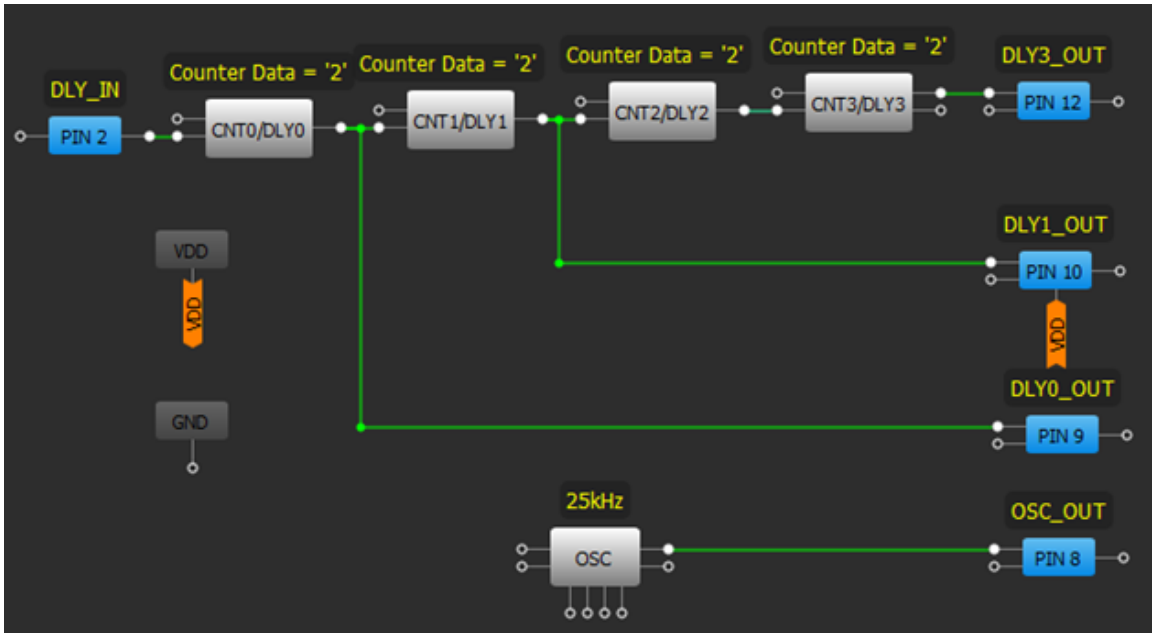

Fig. 3. Series Connection of Delay Cells (25kHz Frequency Option)

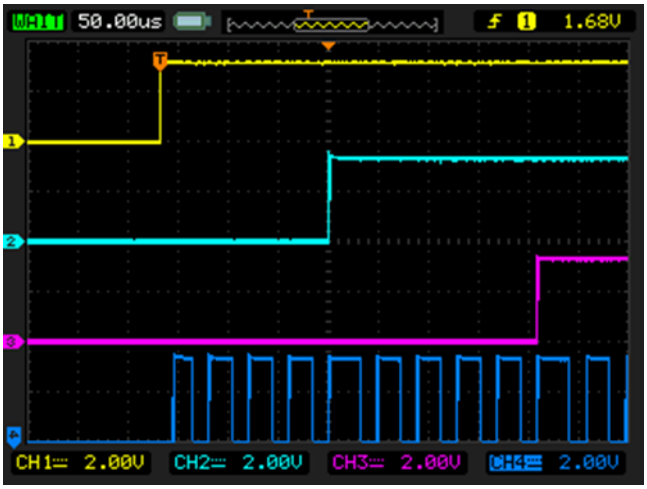

Fig. 4. Series Connection of Delay Cells waveforms (blue=RCOSC)

2MHz RC OSC Frequency Setting

The delay timings calculation for 2MHz option is pretty much the same as for the 25kHz frequency setting, with the only difference that in addition the settling time is taken into account in max time calculation.

$$T_{\min} = \frac{Counter\_Data + 2}{\frac{F_{osc}}{pre\_div \cdot clk\_div} \cdot (1 + \mathrm{var}_{\max})}$$

$$T_{typ} = \frac{Counter\_Data + 2.5}{\frac{F_{osc}}{pre\_div \cdot clk\_div}}$$

$$T_{\max} = \frac{Counter\_Data + 3}{\frac{F_{osc}}{pre\_div \cdot clk\_div} \cdot (1 + \mathrm{var}_{\min})} + T_{settle}$$

where T_{settle} – maximum RC OSC settling time.

Of course, if you are calculating the delay time while the RC OSC is already operational (Forced Power On, or another delay is operating, etc.) there is no settling time to account for. So, in this case the first three formulas should be used for calculations.

The 2MHz RC OSC frequency option differs from 25kHz option not only by the clocking frequency, but with different tolerance for VDD and temperature variation.

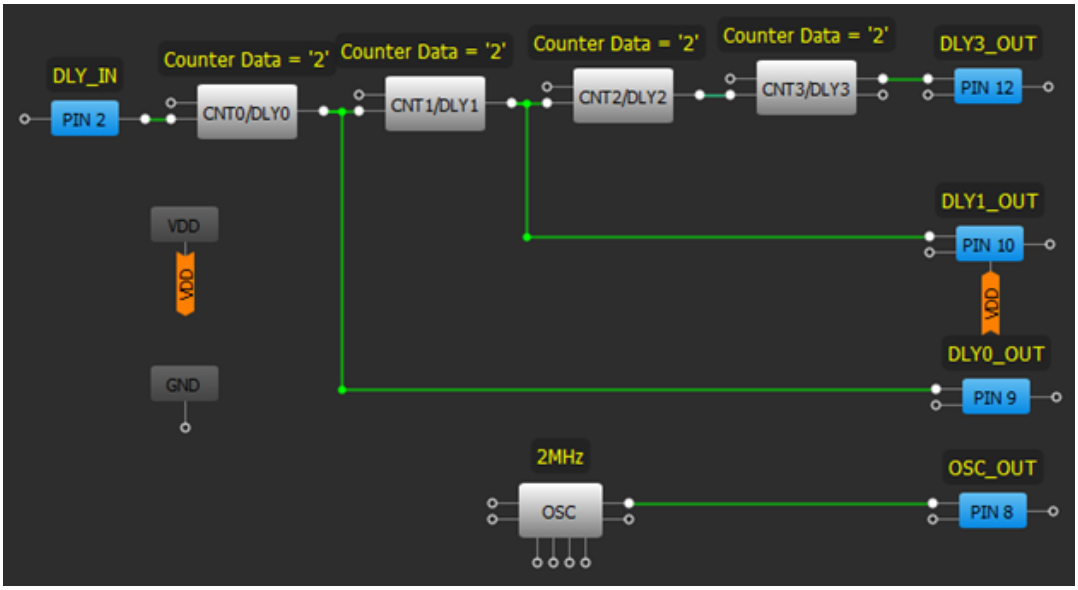

Fig. 5. Series Connection of Delay Cells (2MHz Frequency Option)

The var_{min} and var_{max} parameters are calculated in the same way as for previous cases. Table 2 shows the frequency variation percentage depending on different parameters as well as maximum RC OSC settling time.

If the delay cell is inside the series connection of delay cells and it is not the first one (as shown in Fig.5), the delay time calculation will be different. Such a connection is very frequently used in power rail sequencing designs. Fig.6 shows the resulting delay time waveforms where the first cell has a shorter delay time than an inside one, even though their settings are the same.

Visible in Fig.6 is the additional RC OSC clock latency and settling time for the inside delays connection. Therefore, the following formulas should be used for min, max and typical delay times calculation.

$$T_{\min} = \frac{Counter\_Data + 2 + N_{var}}{\frac{F_{osc}}{pre\_div \cdot clk\_div} \cdot (1 + var_{max})}$$

$$T_{typ} = \frac{Counter\_Data + 2.5 + N_{var}}{\frac{F_{osc}}{pre\_div \cdot clk\_div}}$$

$$T_{\max} = \frac{Counter\_Data + 3 + N_{var}}{\frac{F_{osc}}{pre\_div \cdot clk\_div} \cdot (1 + var_{min})} + T_{settle}$$

The var_{min} and var_{max} parameters are calculated in the same way as for previous formulas. As in the case of 25kHz frequency option N_{var} is a variable in range of 0 to 1.

Parameter	SLG46110/SLG46120		SLG46721/SLG46722		Conditions
	Min	Max	Min	Max	
RC OSC trim error	-5%	5%	-5%	5%	None
RC OSC variation with VDD	-1.68%	1.03%	-2.86%	2.1%	1.8V[1]
	-0.47%	0.45%	-1%	0.37%	3.3V[2]
	-1.31%	0.65%	-1.18%	0.77%	5V[3]
RC OSC variation with temperature	-21.75%	7.5%	-21.75%	7.5%	-20C - +45C
	-21.75%	11.32%	-21.75%	11.32%	-20C - +70C
	-27.36%	12.66%	-27.36%	12.66%	-40C - +85C
	-12.9%	12%	-12.9%	12%	0C - +70C
	-12.9%	13.1%	-12.9%	13.1%	0C - +80C
	-21.9%	13.1%	-21.9%	13.1%	-20C - +80C
Settling time	--	9.680 µs	--	9.625 µs	1.8V[1]
	--	5.698 µs	--	5.524 µs	3.3V[2]
	--	5.451 µs	--	5.122 µs	5V[3]

Table 2. GreenPAK3 Additional Variation tolerance and Settling Time. 2MHz Frequency Option

[1] means that chip is trimmed at VDD=1.8V and VDD operation range is 1.71V to 1.89V

[2] means that chip is trimmed at VDD=3.3V and VDD operation range is 3V to 3.6V

[3] means that chip is trimmed at VDD=5V and VDD operation range is 4.5V to 5.5V

Conclusion

Using the given formulas and tolerance variation data will aid in calculating accurate delay times of the delay cell in GreenPAK designs. Also presented was the effect on delay time of possible cell connections. For more specific tolerance variation and settling time data please contact Silego (**greenpak@silego.com**). Also, further detail may be found in errata sheets for GreenPAK3 devices. The information they contain describe the possible issues in delay time calculations and the workarounds for them.

About the Author

Name: Roman Yankevych

Background: Roman Yankevych graduated from Lviv Polytechnic National University in 2009, studying at the Department of Radioelectronic Devices and Systems. He designs with Configurable Mixed Signal ICs (CMICs) and provides engineering support for their application. Additionally he has over 5yr experience with signal processing in radar and communication systems.

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A	Roman Yankevych	05/20/2015	New application note

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