

Introduction

This application note shows how to use a single GreenPAK Configurable Mixed-signal IC to design a circuit to determine whether the input voltage is rising, falling, or constant in time.

Voltage slope direction determination circuit design

In this circuit, the ADC is connected to the SPI block. DCMP takes data from ADC and SPI. Signals from DCMP go to LUTs, DFF, P DLY, and DLYs, which are used to avoid glitches and form output signals.

Block configuration is presented in figures 2-10 below.

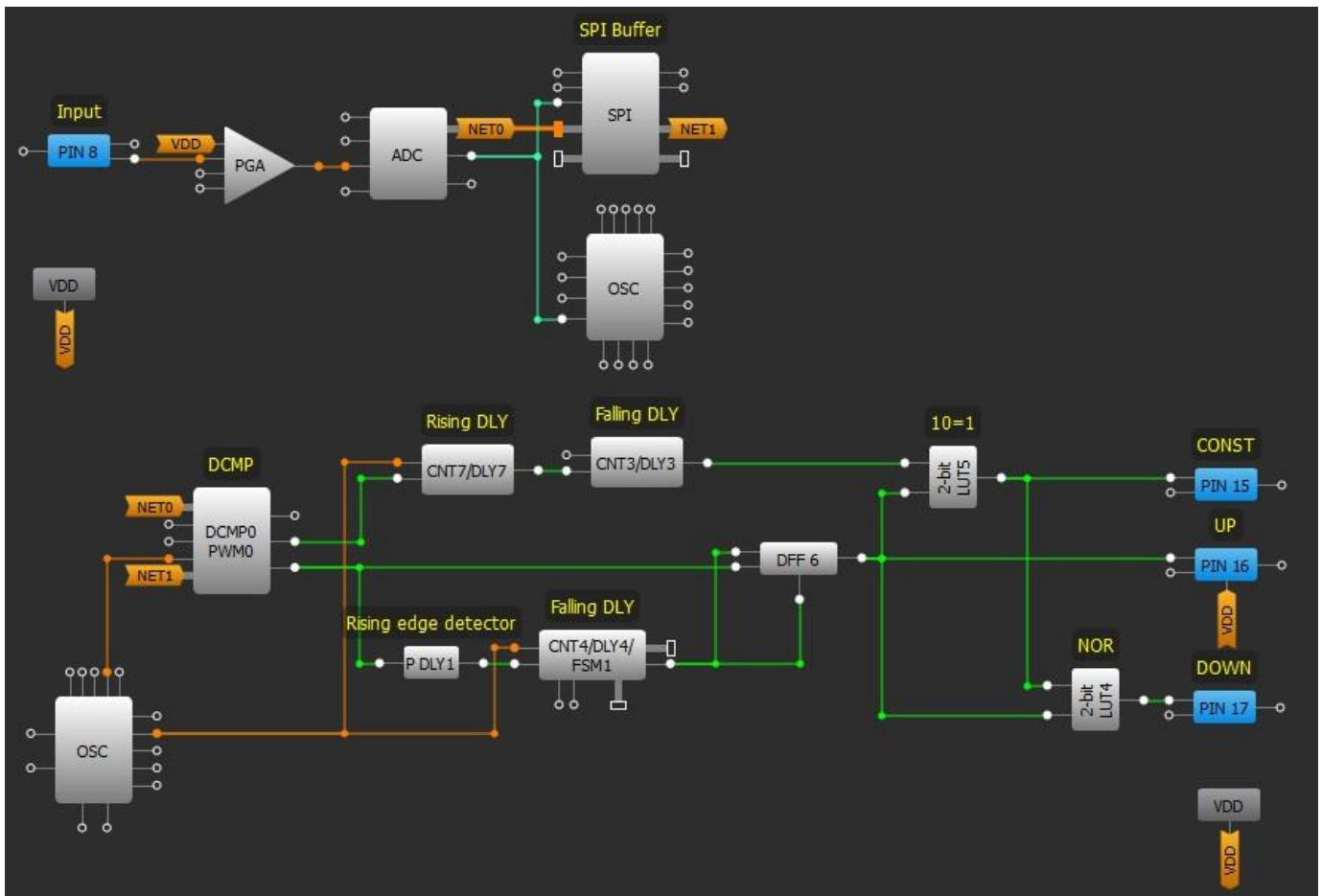


Figure 1. Voltage slope direction definer circuit schematic



PIN 8

I/O selection: Analog input/output

Input mode: Analog input
OE = 0

Output mode: Analog output
OE = 1

Resistor: Floating

Resistor value: Floating

PIN 15

I/O selection: Digital output

Input mode: None
OE = 0

Output mode: 1x push pull
OE = 1

Resistor: Floating

Resistor value: Floating

PIN 16

I/O selection: Digital output

Input mode: None
OE = 0

Output mode: 1x push pull
OE = 1

Resistor: Floating

Resistor value: Floating

PIN 17

I/O selection: Digital output

Input mode: None
OE = 0

Output mode: 1x push pull
OE = 1

Resistor: Floating

Resistor value: Floating

Figure 2. Pins properties

2-bit LUT5

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0

2-bit LUT4

IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0

Figure 3. LUTs properties

DFF/LATCH6

Mode: DFF

nSET/nRESET option: nRESET

Initial polarity: Low

Q output polarity: Non-inverted (Q)

Figure 4. DFF properties

PGA

Power on signal: Power on

Gain: x1

ADC mode: Single-end

Connections

Channel selector: VDD

IN+ Channel 1: PIN 8

IN+ Channel 2: None

IN- Channel: None

External output: Disable

Figure 5. PGA properties



ADC	
Mode:	Single-end
Vref:	Bandgap (1 V)
Force analog part:	Disable
Analog part speed selection:	5 kHz
Clock for ADC divide by:	16
ADC data sync with SPI clock:	Disable
PWM & ADC clock source :	RC OSC
Sample speed:	1.5625 kHz Formula

Figure 6. ADC properties

SPI	
Mode:	ADC/FSM buffer
Clock phase (CPHA):	0
Clock polarity (CPOL):	0
Byte selection:	[15:0]
ADC data sync with SPI clock:	Disable
PWM data sync with SPI clock:	Disable
FSM data sync with SPI clock:	Disable
Connections	
PAR input data source:	ADC
Serial data:	Disable (Matrix <->)

Figure 7. SPI properties

DCMP0/PWM0	
DCMP/PWM power register:	Power on
Function selection:	DCMP
PD sync to clock:	Off
Clock source:	OSC X CLK
Clock invert:	Disable
PWM & ADC clock source :	RC OSC
PWM data sync with SPI clock:	Disable
Duty cycle:	0% - 99.6%
PWM deadband time:	10 ns
Register 0: MTRX SEL: (0:0)	0
Register 1: MTRX SEL: (0:1)	0
Register 2: MTRX SEL: (1:0)	0
Register 3: MTRX SEL: (1:1)	0
Connections	
IN+ selector:	ADC [7:0]
IN- selector:	SPI [7:0]

Figure 8. DCMP properties

P DLY1	
Mode:	Rising edge detect
Delay:	4 Cells
Output mode:	Non-delayed

Figure 9. P DLY properties



14-bit CNT3/DLY3	
Mode:	Delay
Counter data:	1200 <small>(Range: 1 - 16383)</small>
Delay time:	48.1000 ms Formula
Edge select:	Falling
Q mode:	None
DFF bypass enable:	None
Connections	
FSM data:	None
Clock:	CLK
Clock source:	OSC Freq.
8-bit CNT4/DLY4/FSM1	
Mode:	Delay
Counter data:	200 <small>(Range: 1 - 255)</small>
Delay time:	32.4000 ms Formula
Edge select:	Falling
Q mode:	Reset
DFF bypass enable:	None
FSM data sync with SPI clock:	Disable
Connections	
FSM data:	Counter data
Clock:	CLK /4
Clock source:	CLK Freq. / 4
8-bit CNT7/DLY7	
Mode:	Delay
Counter data:	75 <small>(Range: 1 - 255)</small>
Delay time:	12.4000 ms Formula
Edge select:	Rising
Q mode:	None
DFF bypass enable:	None
Connections	
FSM data:	None
Clock:	CLK /4
Clock source:	CLK Freq. / 4

Figure 10. DLYs properties

Voltage slope direction determination circuit analysis

The Analog signal comes from Input 8 to the PGA block with 1x gain. It then goes to the ADC input. The ADC operates in single-ended mode and converts the analog signal to an 8-bit digital code. The ADC transfers the parallel signal to the SPI block, configured as ADC/FSM Buffer, where digital code can be stored and won't change until the next CLK clock comes to SPI SCLK input. The DCMP is used to compare current and previous ADC data, which is stored in the SPI block. SPI takes the CLK from ADC INT OUT, because only one pulse is needed to reload the SPI Buffer code and the DCMP for the 8-bit code comparison. In addition, the ADC INT OUT signal is coordinated in time with the ADC parallel data (see figure 11).

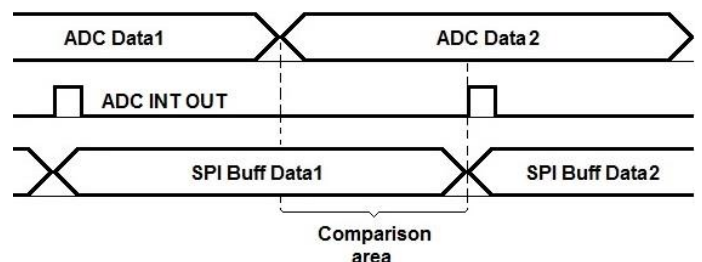


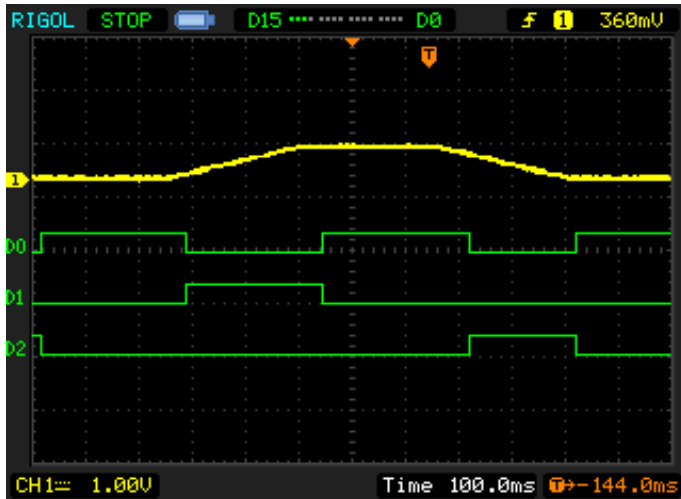
Figure 11. ADC and SPI Buffer timing diagram

If the voltage is rising, then the ADC Data2 8-bit code is greater than the ADC Data1 code (SPI Buffer Data1). In this situation we will receive pulses from the DCMP OUT+ (OUT+ will go high in Comparison area (see Figure 11)). Rising edge detector (P DLY), Falling edge DLY and DFF6 are used to check if pulses from DCMP are regularly repeated. If they are, UP output will go high.

If voltage is constant we will receive a high level signal from the DCMP EQ output. Rising edge DLY7 and Falling edge DLY3 are used to eliminate short pulses on this output. UP output priority is higher than CONSTANT output thanks to 2-bit LUT5. So if UP output is high, CONSTANT output will stay low.



If CONSTANT output is low and UP output is low, DOWN output goes high.



(CH1 – Input voltage; D0 – CONST;
D1 – UP; D2 – DOWN)

Figure 12. Voltage slope direction definer functional diagram (First case)

Conclusion

A simple device that can detect whether an input voltage is rising, falling, or constant can be easily implemented using ADC, SPI, DCMP, and some additional blocks, which helps to form the output signals. All this functionality is contained in a single SLG46620 IC.



About the Author

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Background: Yurii Shchebel graduated from Ivan Franko Lviv National University in 2015, studying at the Department Electronics. Presently he is working with Configurable Mixed Signal ICs (CMICs) and their applications. Additionally, he designs audiophile grade amplifiers.

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A	Yurii Shchebel	5/14/2015	New application note

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