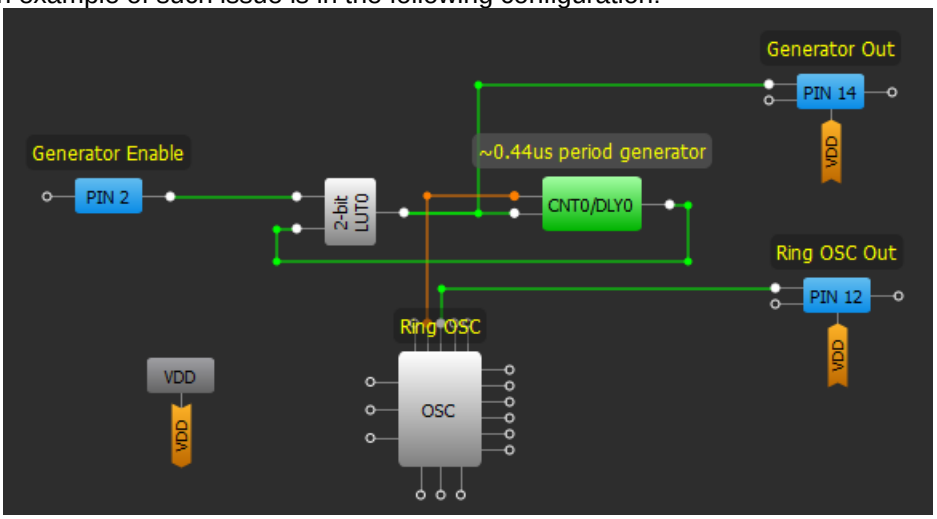
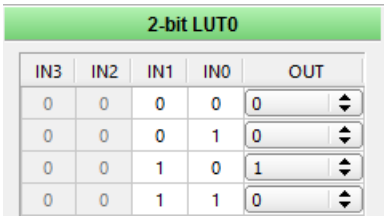
Errata disclaimer: This Errata applies to SLG46140 revisions LS and OA.

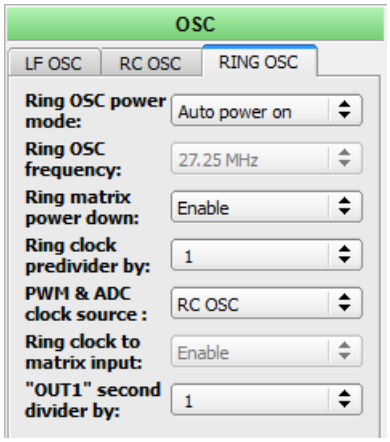
ISSUE 1: Long Ring OSC Settling Time
Functional Block Affected: Ring OSC, Delay, Counter

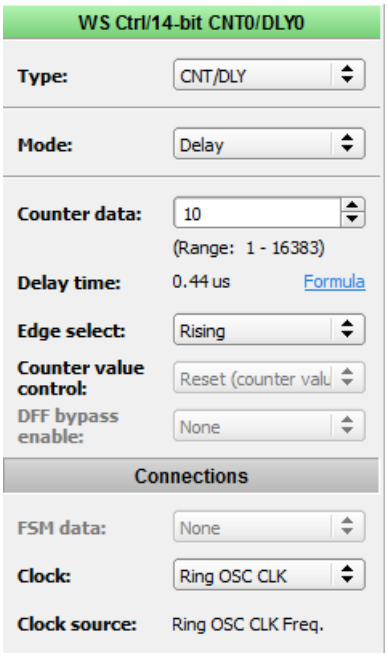
Description:

The Ring OSC has a longer settling time when configured as Auto Power On in the designs that have very short Ring OSC disable time. An example of such issue is in the following configuration:

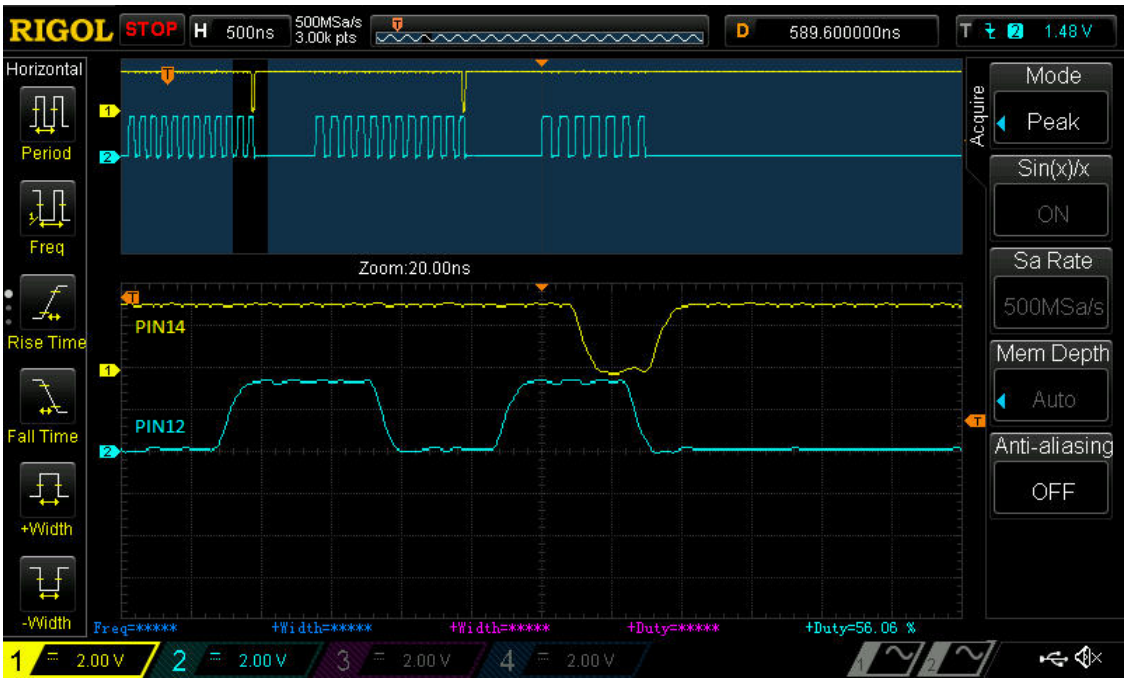








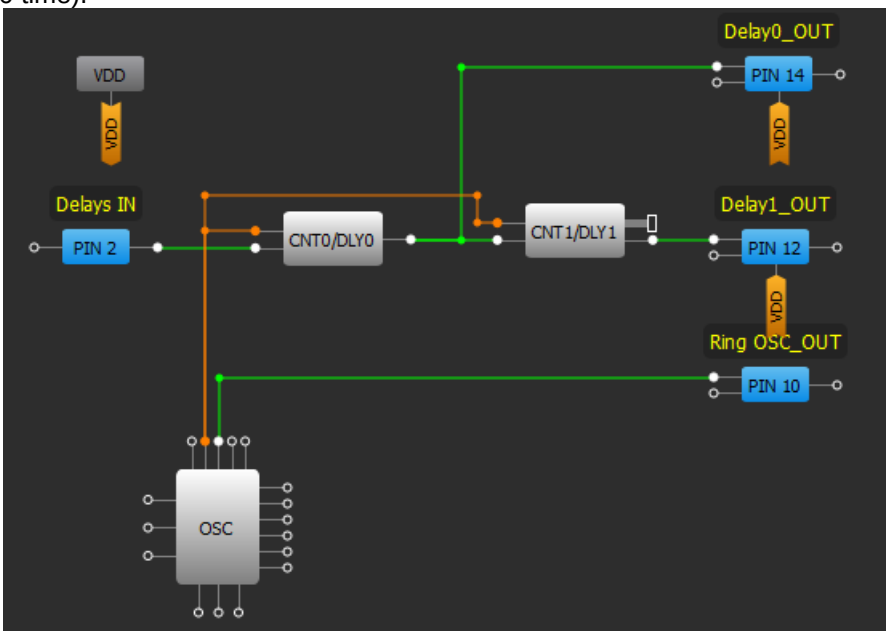
The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a high signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.



Channel 1 – 2-bit LUT0 output; Channel 2 – Ring OSC output

Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

A similar situation occur while using two connected delays (all edge detect types except for a pair “Rising edge DLY – Falling edge DLY”).
In the following example, Delay0 and Delay1 are configured in the same way. However, Delay0 time is 11.4us instead of expected 0.4us (Delay0 time).



Workaround:

- Set Ring OSC power mode to “Force Power On”
- Set Turn on by register option in BG (Band Gap) block as “Enable”

ISSUE 2: PGA has an Offset when loaded
Functional Block Affected: PGA, Vref

Description:

The PGA block has an offset when its output through the VREF is loaded. For reference, shown below is the table of the load vs PGA 4x gain.

Load, mA	Gain (ideal = 4x)
0	3.87
1	3.84
5	3.78
10	3.71
20	3.5
40	3
80	2.2
160	1.4

When the load current is higher than 10 mA the output offset is large and may influence the design operation significantly.

Workaround:

- Use external buffer to support high load

ISSUE 3: ACMP Long Turn On Time
Functional Block Affected: ACMP

Description:

ACMPs in SLG46140 chip may have a long (up to 3.5ms at low temperatures and 1.5ms at room temperature) power up time.

Workaround:

- Use ACMPs as always powered on.
- Consider this issue in the design

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