

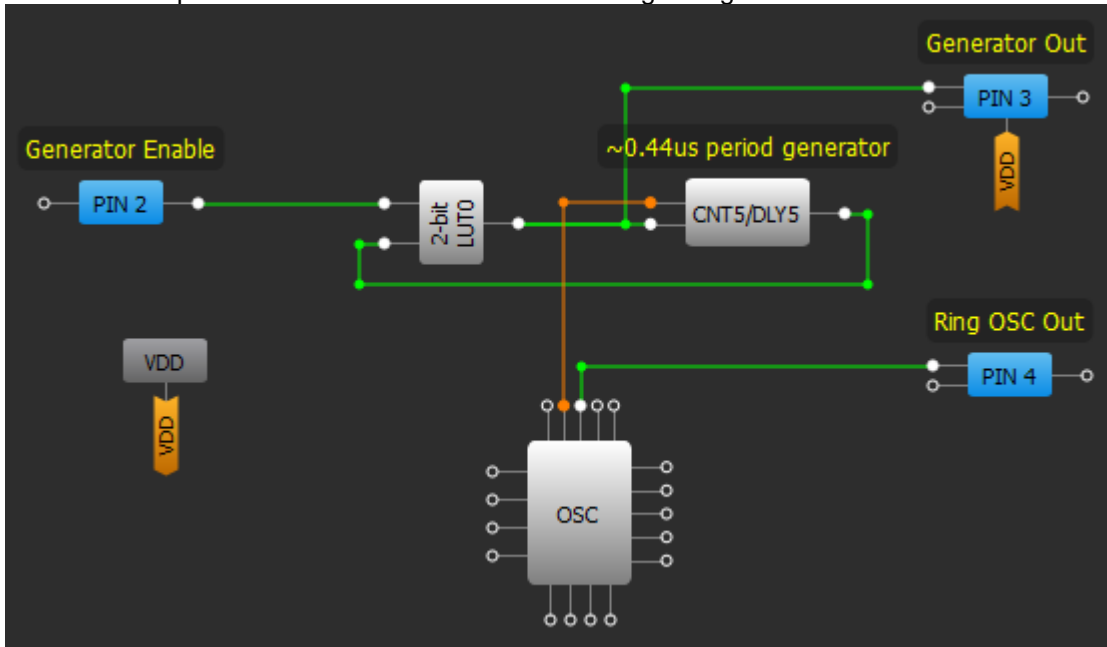


Errata disclaimer: This Errata applies to SLG46620B revision PA.

## ISSUE 1: Long Ring OSC Settling Time Functional Block Affected: Ring OSC, Delay, Counter

### Description:

The Ring OSC has a longer settling time when configured as Auto Power On in the designs that have very short Ring OSC disable time. An example of this issue is shown in the following configuration:



### 2-bit LUT0

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0

### OSC

LF OSC   RC OSC   **RING OSC**

Ring OSC power mode: Auto power on

Ring OSC frequency: 27.25 MHz

Ring matrix power down: Enable

Ring clock predivider by: 1

PWM & ADC clock source: RC OSC

Ring clock to matrix input: Enable

"OUT1" second divider by: 1

### 8-bit CNT5/DLY5

Mode: Delay

Counter data: 10  
(Range: 1 - 255)

Delay time: 0.44 us [Formula](#)

Edge select: Rising

Counter value control: None

DFF bypass enable: None

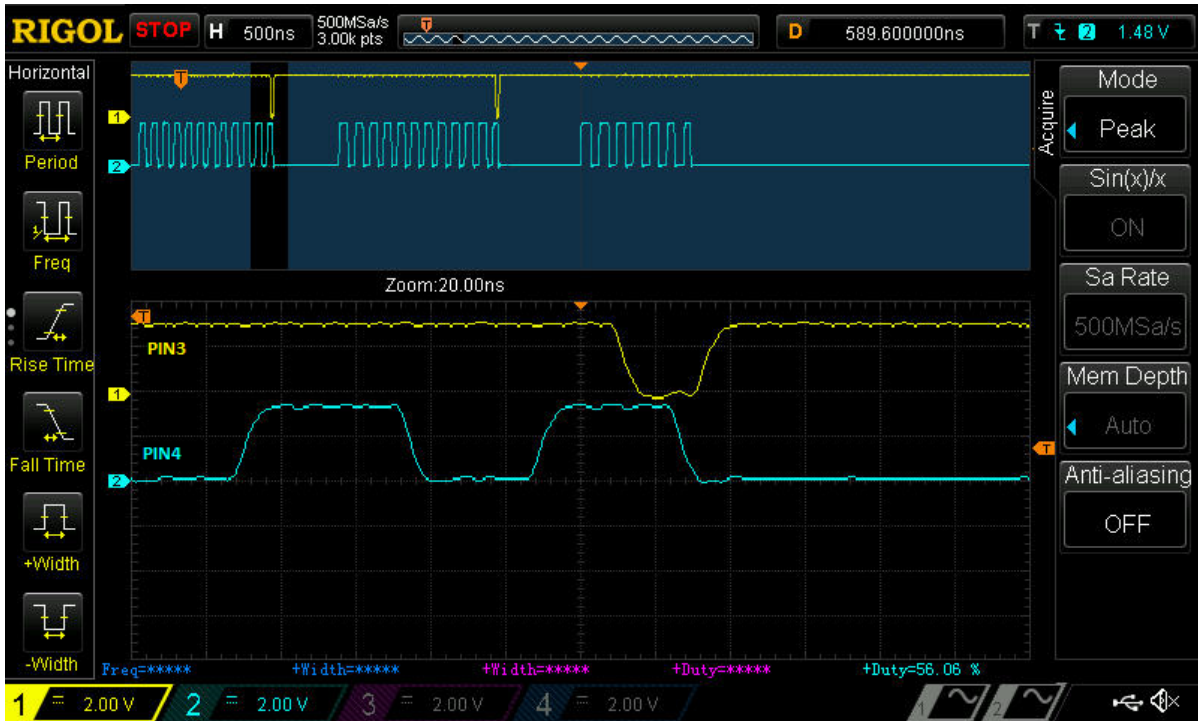
**Connections**

FSM data: None

Clock: Ring OSC CLK

Clock source: Ring OSC CLK Freq.

The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a high signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.

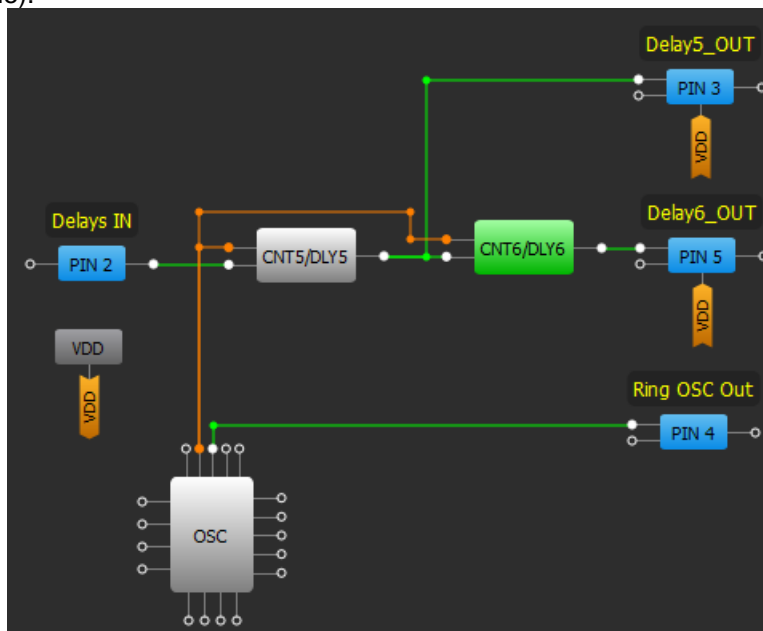


Channel 1 – 2-bit LUT0 output; Channel 2 – Ring OSC output

Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

A similar situation can occur while using two connected delays (all edge detect types except for a pair “Rising edge DLY – Falling edge DLY”).

In the following example, Delay0 and Delay1 are configured in the same way. However, Delay0 time is 11.4us instead of expected 0.4us (Delay0 time).





### Workaround:

- Set Ring OSC power mode to “Force Power On”
- Set Turn on by register option in BG (Band Gap) block as “Enable”

## ISSUE 2: PGA has an Offset when loaded

Functional Block Affected: PGA, Vref

### Description:

The PGA block has an offset when its output through the VREF is loaded. For reference, the table below shows the load vs PGA 4x gain.

Load, mA	Gain (ideal = 4x)
0	3.87
1	3.84
5	3.78
10	3.71
20	3.5
40	3
80	2.2
160	1.4

When the load current is higher than 10 mA the output offset is large and may influence the design operation significantly.



Workaround:

- Use an external buffer to support high load

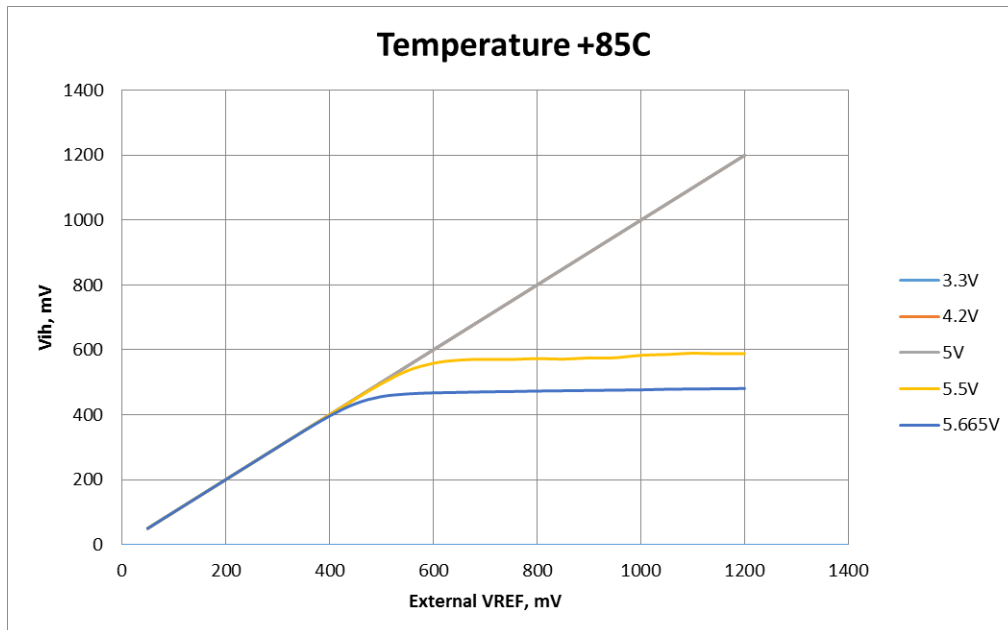
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### ISSUE 3: ACMP Output is Inaccurate when using External Vref at High VDD and Temperature

**Functional Block Affected: ACMP**

Description:

When using external Vref source, the ACMP comparison may happen at wrong threshold if the external Vref voltage is higher than a particular value (please see figure below) at high VDD values (> 5V) and high temperature.



Workaround:

- Avoid using ACMPs in such conditions.

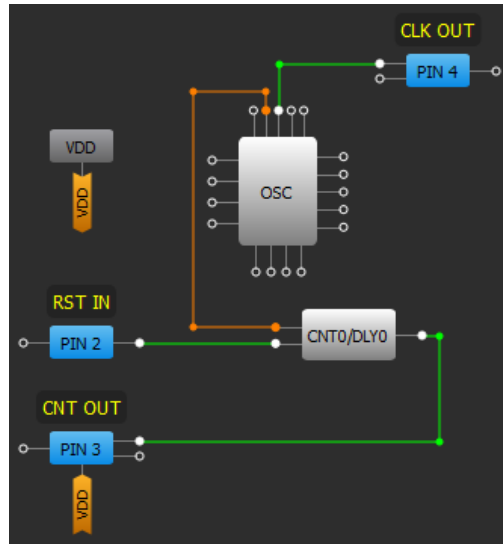
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### ISSUE 4: Incorrect Counter Operation after the Reset

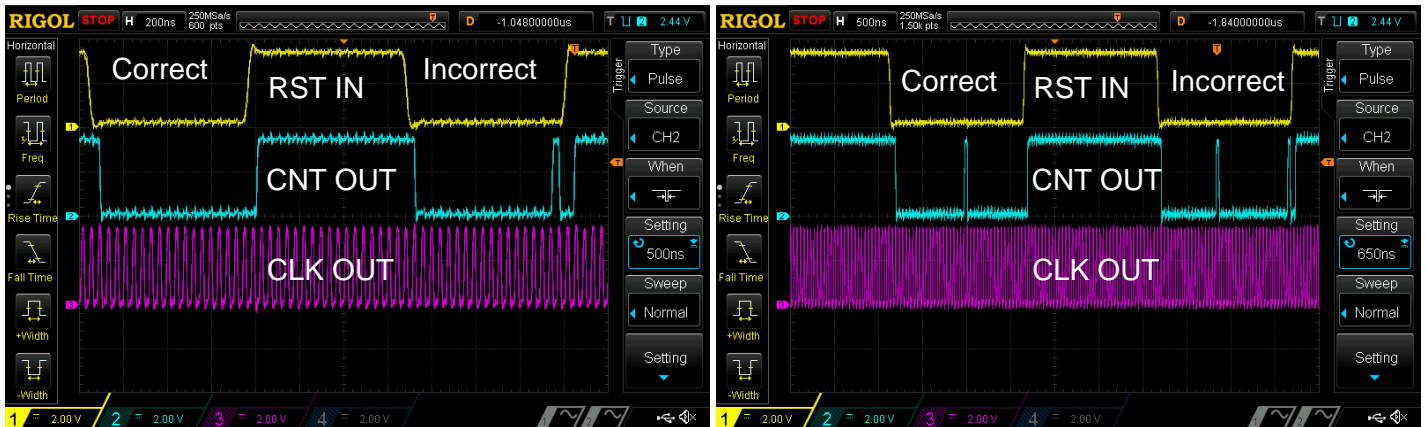
**Functional Block Affected: Counter**

Description:

If the Counter Reset occurs at a time very close to a rising edge of the clock signal during clock signal generation (for example OSC operation), there is a possibility that the Counter Data of the Counter is reset incorrectly and the counter end signal (HIGH pulse) may appear faster than expected. This phenomena appears more frequently the higher the clock frequency is.

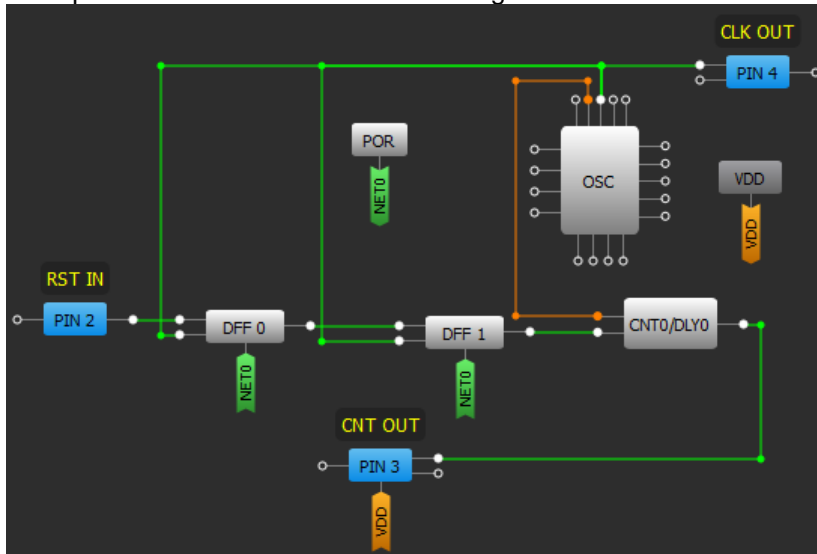


WS Ctrl/14-bit CNT0/DLY0	
Type:	CNT/DLY
Mode:	Counter
Counter data:	20 (Range: 1 - 16383)
Output period (typical):	0.78 us <a href="#">Formula</a>
Edge select:	High level reset
Counter value control:	None
DFF bypass enable:	None
Connections	
FSM data:	None
Clock:	Ring OSC CLK
Clock source:	Ring OSC Freq.
Clock frequency:	27000 kHz



### Workaround:

- Synchronize RESET input of the Counter with its CLK using 2 DFF cells as shown in the image below.



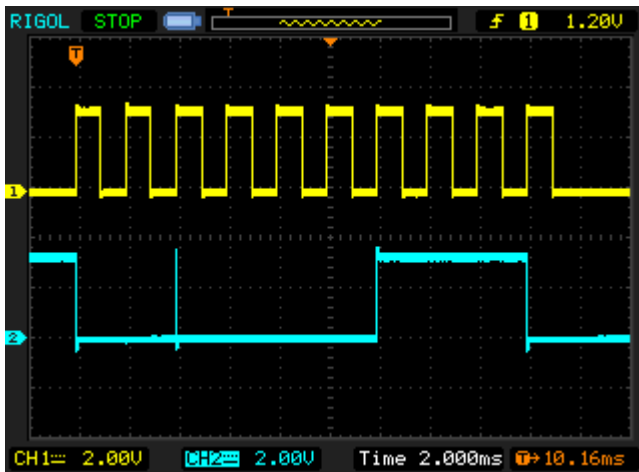
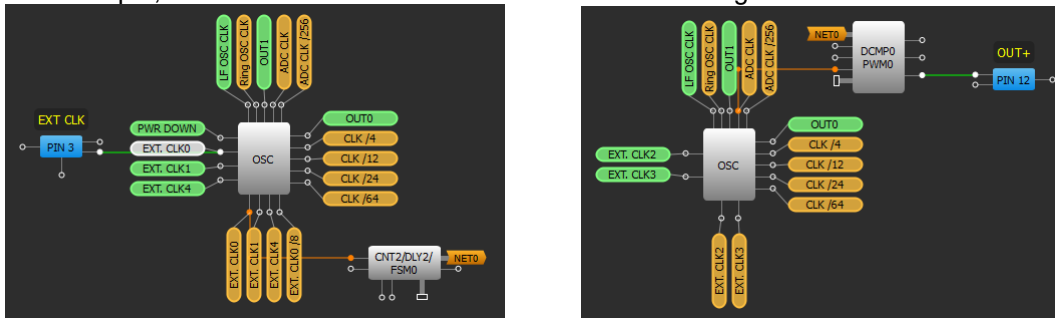


## ISSUE 5: DCMP OUT+ Output Glitch Functional Block Affected: DCMPs

### Description:

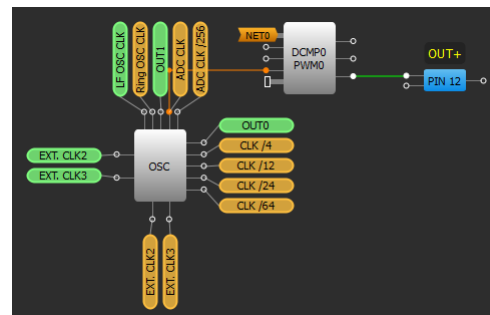
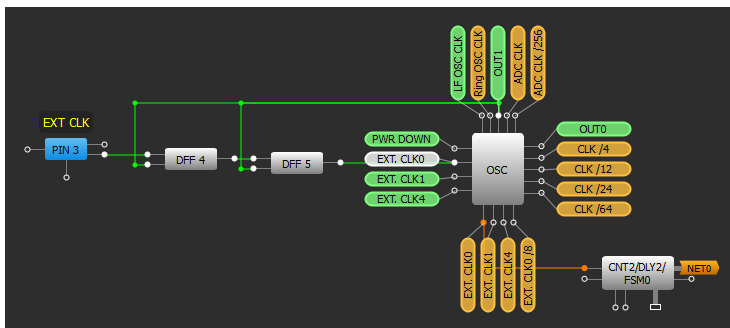
DCMP's OUT+ output may have a glitch when the input data is changed. This issue appears more frequently the higher DCMP clock is.

For example, DCMP IN+ sources from FSM0 and IN- from Register0. DCMP is clocked from the Ring OSC.



### Workaround:

- Synchronize the data source clock with the DCMP clock source using 2 DFF cells as shown in the images below.





# SILEGO

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## **Silego Technology**

### **Corporate Headquarters**

1515 Wyatt Drive  
Santa Clara, CA 95054  
USA  
Phone: 408-327-8800

### **Silego Taiwan Office (Hsin Chu)**

6F-12, Number 38, Tai Yuan Street  
Tai Yuan Industrial Park, Jhubei City  
Hsin Chu County, 30265, Taiwan  
Phone: +886-3-560-0313  
Fax: +886-3-560-0316

### **Silego Taiwan Office (Taipei)**

9F, No.10, Ln. 321, Yangguang St,  
Neihu District,  
Taipei City 114, Taiwan  
Phone: +886-2-2658-1038

### **Silego Japan Office**

20F Shinjuku i-Land Tower  
6-5-1 Nishi-shinjuku, Shinjuku-ku,  
Tokyo 163-1320  
Phone: 03-6830-5035  
Fax: 03-3348-7515

### **Silego Korea Office (Seoul)**

#402 Dongmun Building, 10,  
Dogok-ro 2-gil, Gangnam-gu,  
Seoul, Korea (Post code: 06258)  
Phone: +82-3453-7560 or  
+82-2-3453-7127

### **Silego Korea Office (Suwon)**

#101-801 Hanwha-Ggumegreen-Hyowon,  
1116-3 Ingye-dong, Paldal-gu,  
Suwon-si, Gyeonggi-do, Korea

### **Silego China Office (Hefei)**

Rm303, Building 2, No3 TianYuan Rd  
High-Tech Zone  
Hefei, China 230088  
Phone: +86-551-65368431  
Fax: +86-551-65368432

### **Silego Ukraine Office**

Business Center Intercity-Silego  
Chervonoi Kalyny ave., 62a, 5th Floor, Room 5.1  
Lviv, Ukraine  
Phone: +38(032)232-80-53

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