

## Introduction

This application note demonstrates how to design with the asynchronous state machine within the SLG46531 GreenPAK CMIC. This design controls an LED flashlight, and features numerous modes all controlled by a single button.

## General operating principle

The five operating modes are: disabled mode, low brightness (PWM with 30% duty cycle), moderate brightness (PWM with 70% duty cycle), maximum brightness (PWM with 100% duty cycle) and SOS signal mode (dots are 100ms, dashes are 300ms, pauses between dots and dashes are 100ms, pauses between characters are 300ms, and pauses between words are 700ms). This design also has a built-in detector which monitors battery discharge level in all modes except disabled mode.

## Single Button Selector

There are considerations to properly create the asynchronous state machine input signaling so that we switch only one state, with no influence on the other states. The approach presented gives guaranteed results with input signal processing of the single button selector.

The single button selector is at first a frequency divider (realized using a D flip-flop), rising edge detector and falling edge detector in order to separate signals for states switching. Its operation principles are as follows.

After the button is pressed the DFF1 switches to the LOW state and a rising edge appears at the output. After that a single pulse is created at the EDGE DET0 output that switches the Asynchronous State Machine (ASM) from «OFF» disabled mode to the "30% PWM" state (moderate brightness mode).

## 30% light brightness generation

In the state of "30% PWM", the RAM3 output goes HIGH, RAM4 output goes LOW, and these signals come to the IN2 and IN3 inputs of the 4-bit LUT0. IN1 receives a signal from CNT1 block with 70% duty cycle. From the 4-bit LUT0 output a signal with 70% duty cycle appears on the output PINs, configured as the NMOS open drain. The LED illuminates when the output is LOW, and off when output is HIGH.

After the next button press, DFF1 goes LOW and the detector's output pulse appears, which switches the ASM from "30% PWM" to "70% PWM" state.

## 70% light brightness generation

In the state of "70% PWM", the RAM3 output goes LOW, RAM4 output goes HIGH and these signals come to the IN2 and IN3 inputs of the 4-bit LUT0. IN1 receives a signal from CNT1 block with 70% duty cycle.



From the 4-bit LUT0 output the signal, which, being inverted, now has 30% duty cycle comes to the output PINS, configured as NMOS open drain.

After the next button press, DFF1 goes HIGH and the detector's output pulse appears, which switches the ASM from "70% PWM" to "100% PWM" state.

### **100% light brightness generation**

In the state of "100% PWM" the RAM3 output goes HIGH, RAM4 output goes LOW, RAM0 goes HIGH and these signals come to the IN3, IN2 inputs of 4-bit LUT0 and "Reset IN" input of CNT1 respectively. Because of that IN1 receives a LOW level signal from CNT1 block. The 4-bit LUT0 output LOW level signal appears at the output PINS.

After the next button press, DFF1 goes LOW, and the detector's output pulse appears, that switches the ASM from "100% PWM" to "SOS signal" state.

### **"SOS" signal generation**

For "SOS" signal generation, numerous on-chip resources are required: three Delay blocks, two DFFs, five LUTs, one Pipe Delay and three states of the ASM block.

After the "100% PWM" state, the ASM will be switched into «---» state of SOS signal mode that generates 700ms pause between repeating "SOS" words. After the DLY5 output goes HIGH, that switches the ASM from «---» into «S» state to generate the first letter "S" (three dots – Morse code).

It is generated by the DLY3 with negative feedback.

After three pulses ("S" letter), a transition into "O" state happens. Here the second letter – "O" (three dashes – Morse code) will be generated by the DLY4 with negative feedback and variable output pulses frequency (pulse width should be 300 ms and pause between pulses – 100 ms).

To do this a 3-bit LUT1 is used as a MUX for the signal with different frequencies, which can be supplied to DLY4 CLK input. This period consists of 3 dashes (300 ms each), 2 dash pauses (100 ms each), 2 letters pauses (300 ms each) and is equal to 1.7s. DLY6 calculates this time (1.7s), after that it generates a signal for transition into state "S2", where the third letter of the word "SOS" – "S" is generated, using the same blocks as for the first "S".

After the last "S" is generated, the signal, which switches ASM into «---» state (the pause between repeating "SOS" words) will be generated. This process repeats until the single button is once again pressed.

### **Battery discharge control**

A Li-ion battery (18650 type) is used for this flashlight power supply. Operating range for this battery is 3.0V – 4.2V. To protect the battery from excessive discharge, two voltage levels are detected. The first is equal to 3.6V and if the voltage is lower, it is recommended to recharge it. If the voltage is lower than 3.6V, then in case the ON/OFF button is pressed, BAT LOW indicator LED on the flashlight body will illuminate.



The second level is 3.0V. If the voltage is lower, ACMP0 will generate a signal which resets the ASM, which will turn the LED to the OFF state (disabled mode). This helps to preserve the battery "health", and also to retain the number of charge/discharge life cycles.

## Current limit function

In this design, current limit and stabilization techniques are implemented to avoid LED overcurrent.

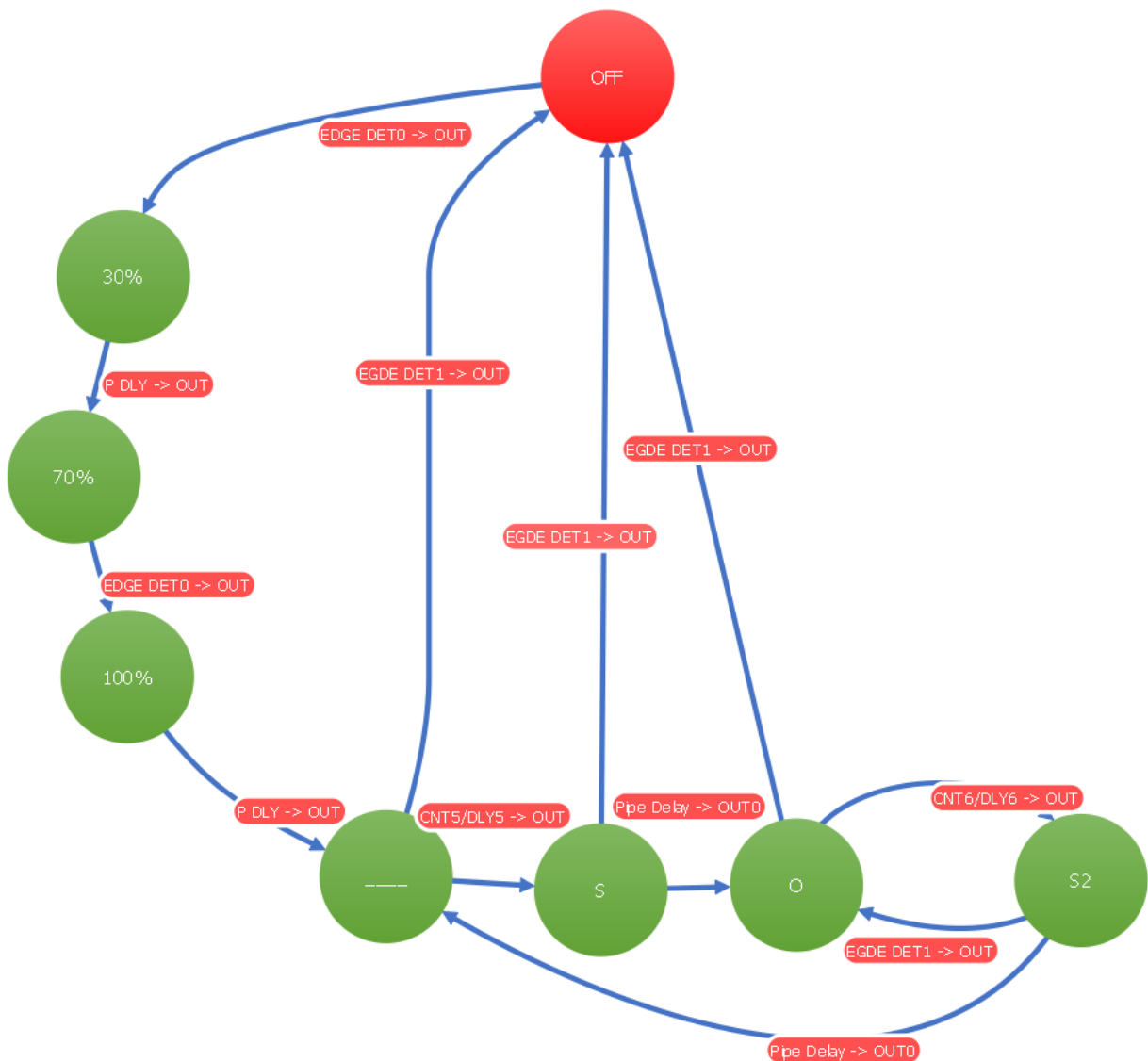
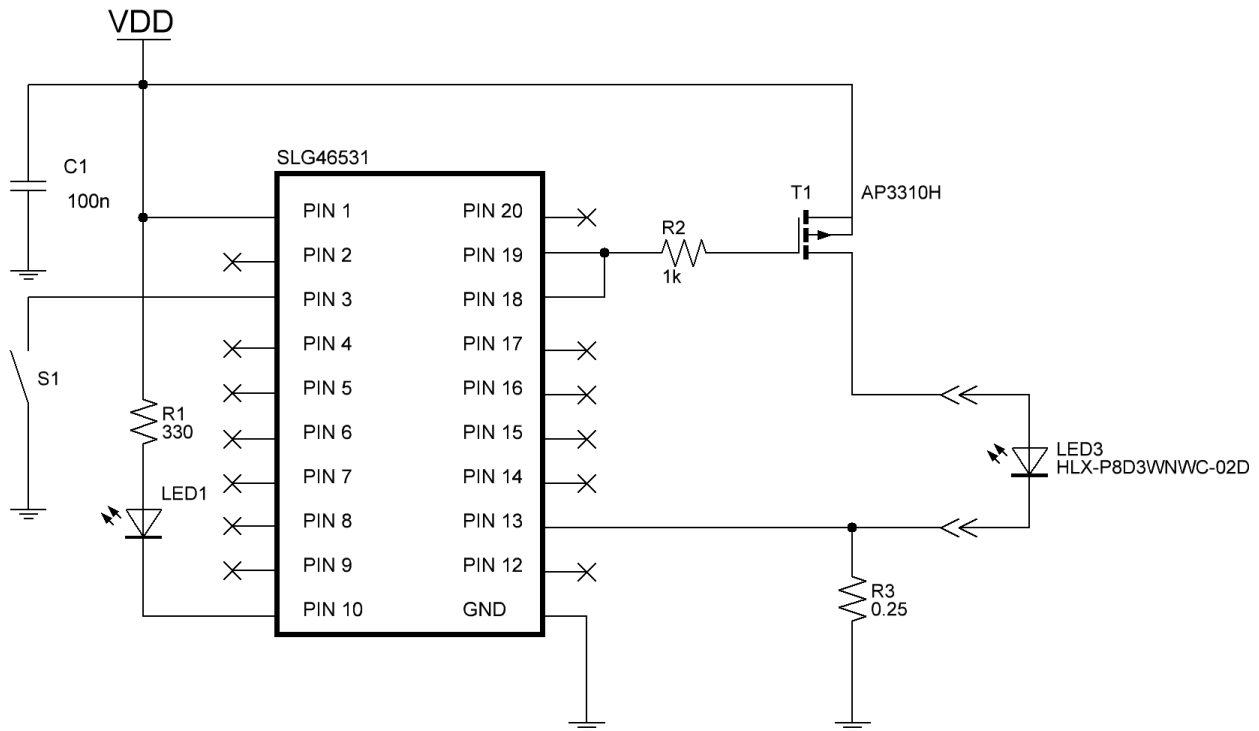


Figure 1. ASM state diagram design





**Figure 3. Flashlight circuit**

## Conclusion

This LED flashlight was quickly designed with within the GreenPAK asynchronous state machine, and is robust. Even with the numerous modes of operation, it features low power consumption and only a few external components.

## Related Files

Programming code for **GreenPAK Designer**.



## About the Author

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Background: Petro Levandovych joined Silego in 2012 and has more than 5 years experience in electronics, radio communication equipment, microcontrollers and automated information system. He began his career with State Enterprise LVIV RADIO ENGINEERING RESEARCH INSTITUTE (SE LRERI), working as System Developer Engineer. Petro has graduated from the Lviv Polytechnic University as a specialist in Radio Communication Equipment Engineering in 2009.

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A	Petro Levandovych	10/02/2015	New application note

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