



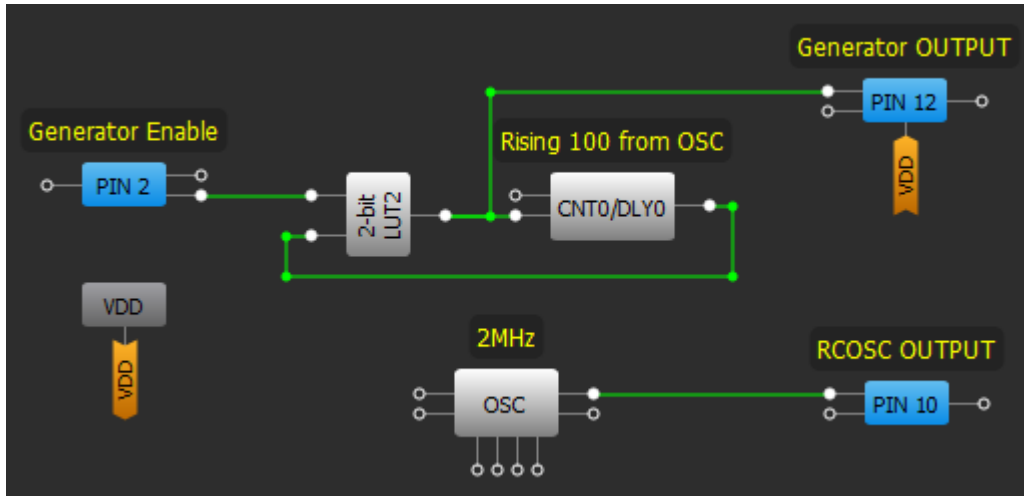
Errata disclaimer: This Errata applies to SLG46117 revision YA.

ISSUE 1: Long RC OSC Settling Time Functional Block Affected: RC OSC, Counter, Delay

Description:

The RC OSC has a longer settling time when configured as 2 MHz with Auto Power On in the designs that have very short RC OSC disable time.

An example of such issue is in the following configuration:

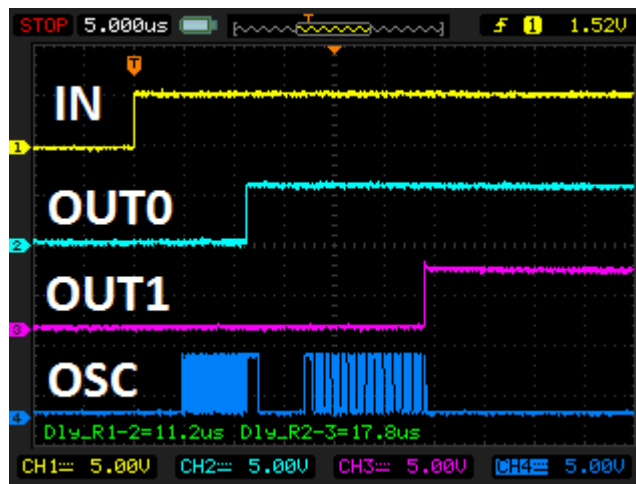
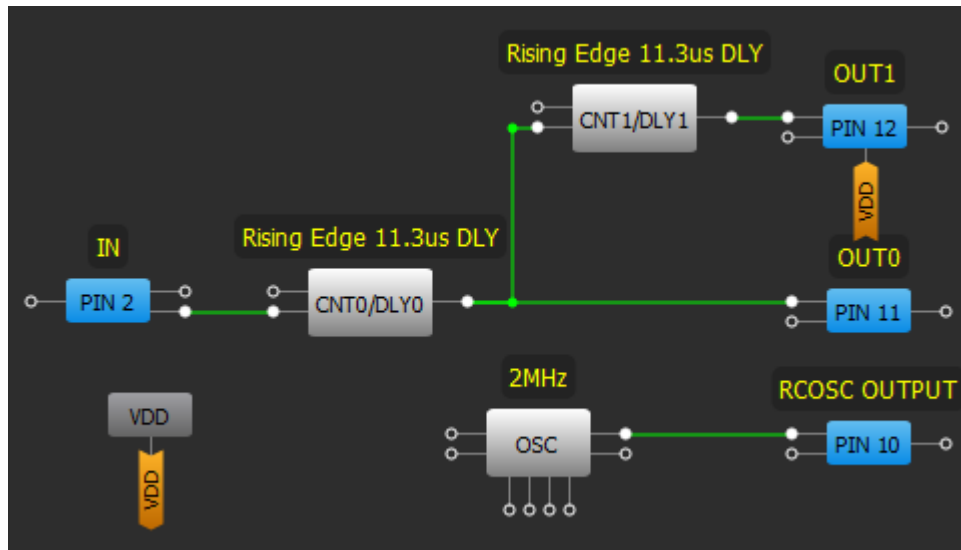


2-bit LUT2				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0

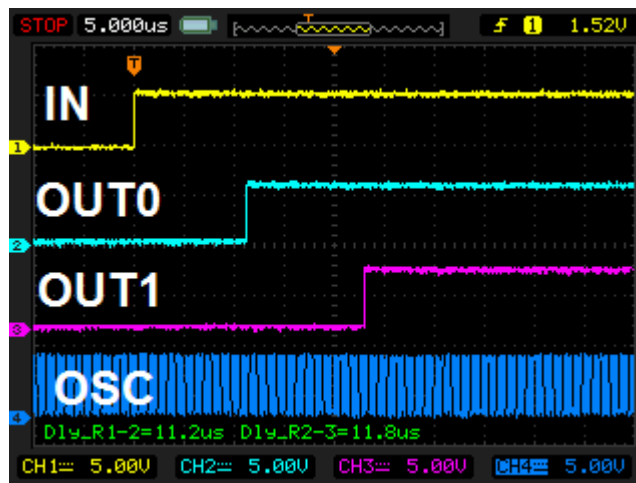
RC OSC	
RC OSC Power register:	Auto Power On
Clock selector:	RC OSC
RC OSC Frequency:	2000.00 kHz

14-bit CNT0/DLY0	
Mode:	Delay
Counter data:	100 (Range: 1 - 16383)
Delay time:	0.0512 ms Formula
Edge select:	Rising

The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a HIGH signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.



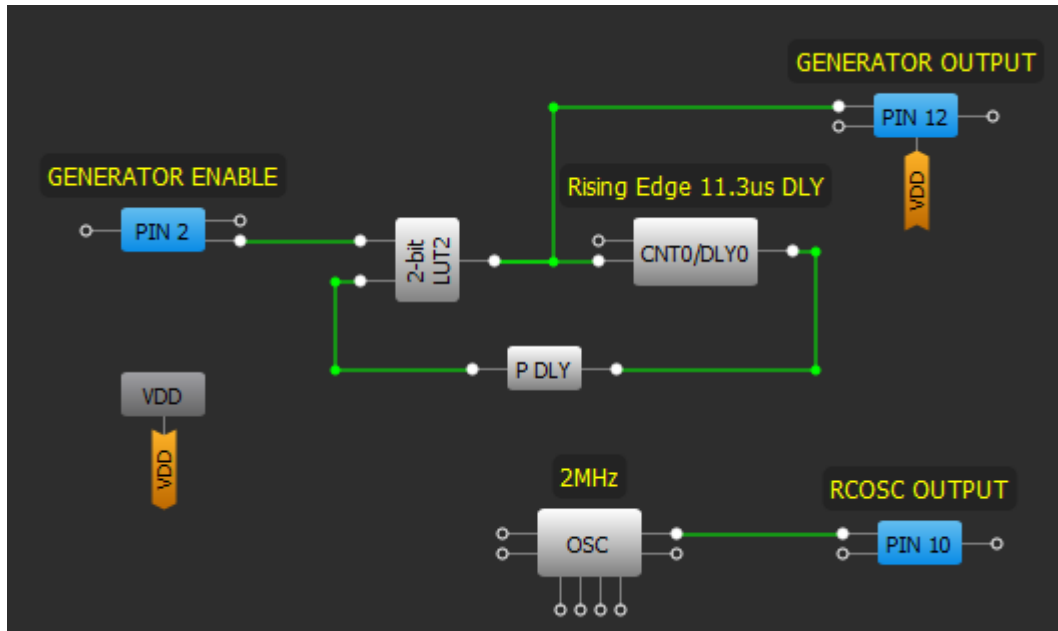
If there are some inner blocks which use RC OSC at the moment or RC OSC is forced power on when such error appears, RC OSC will be operational and delay value will be proper.

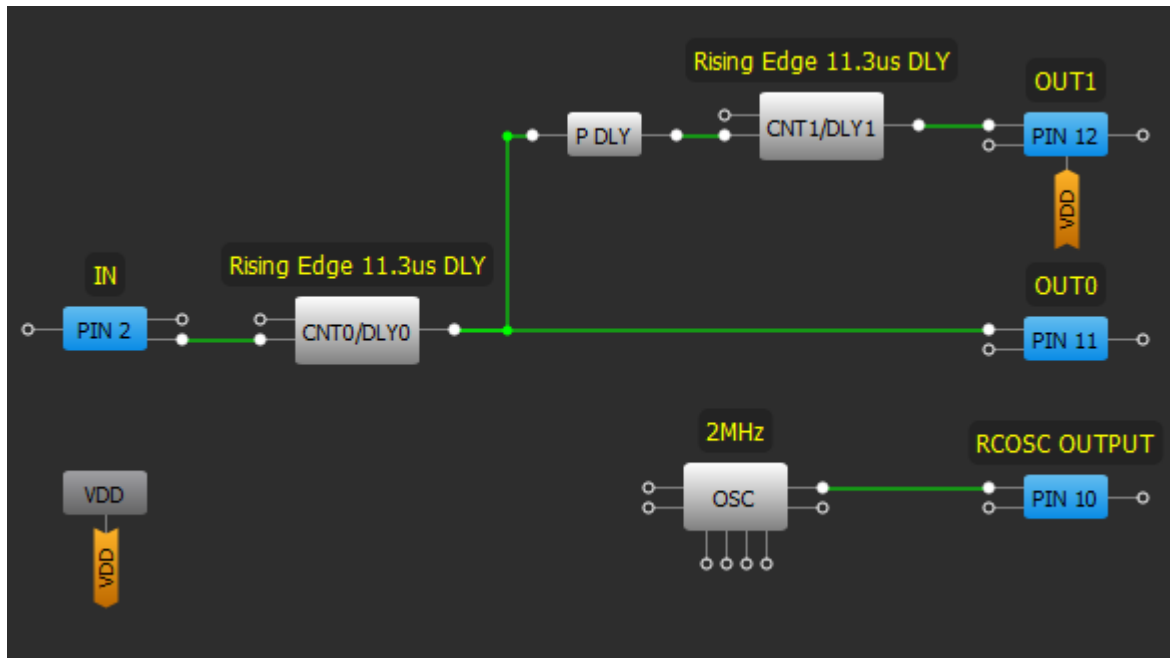




Workaround:

- In first case use block with longer propagation time.





- Use the “Force power on” RC OSC power control option to make the RC OSC operate at all times.

ISSUE 2: Glitches on ACMP output

Functional Block Affected: ACMP

Description:

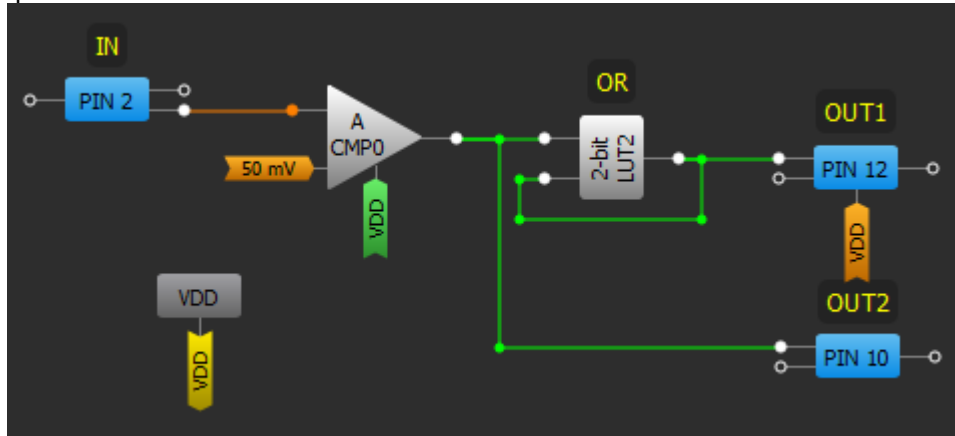
In some cases, ACMP may have short high-level glitches on its output (even if IN+ voltage is less than IN- voltage) after GreenPAK chip being powered up. Such cases may appear when using ACMP with Low Bandwidth mode enabled and Power Up is connected directly to the VDD.

Conditions of glitches appearing are determined by IN- voltage, VDD value and VDD Ramp (see example tables below).

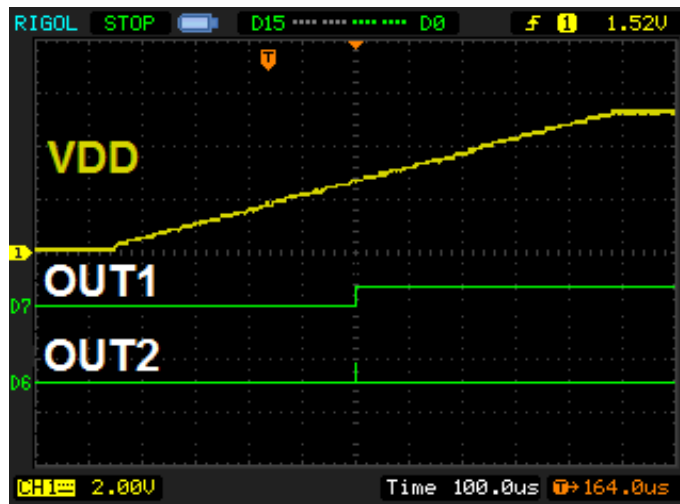
IN- Voltage, mV	VDD, V	VDD Ramp Time	Glitch presence for
50	1.8	10 us	+
50	1.8	1 s	-
50	3.3	10 us	+
50	3.3	1 s	+
50	5.5	10 us	+
50	5.5	1 s	+
600	1.8	10 us	-
600	1.8	1 s	-
600	3.3	10 us	+
600	3.3	1 s	-
600	5.5	10 us	+
600	5.5	1 s	-
1200	1.8	10 us	-
1200	1.8	1 s	-
1200	3.3	10 us	-
1200	3.3	1 s	-
1200	5.5	10 us	+
1200	5.5	1 s	-



In order to detect such glitches, scheme with additional LUT was used. This LUT detects high level on ACMP output and stays high until chip powers down.

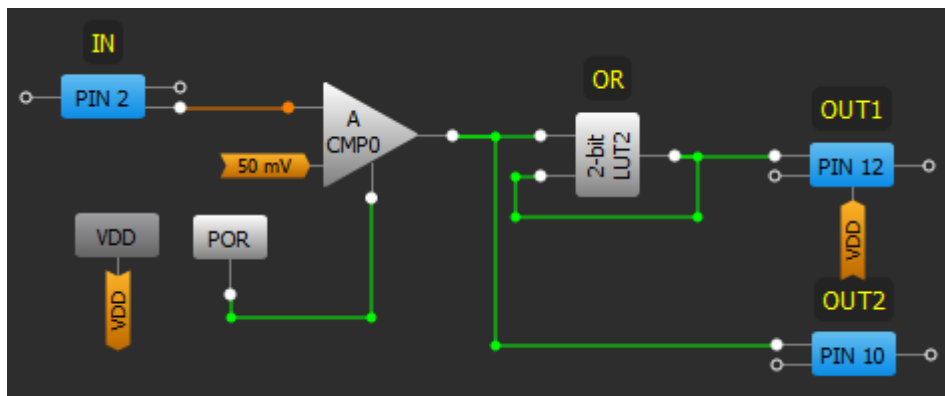


ACMP IN+ is connected to the Ground.



Workaround:

- Use POR block, connected to the ACMP's Power Up pin. However, in this case ACMP will start working with low level output and will be able to go high only after POR goes high + ACMP power on time.



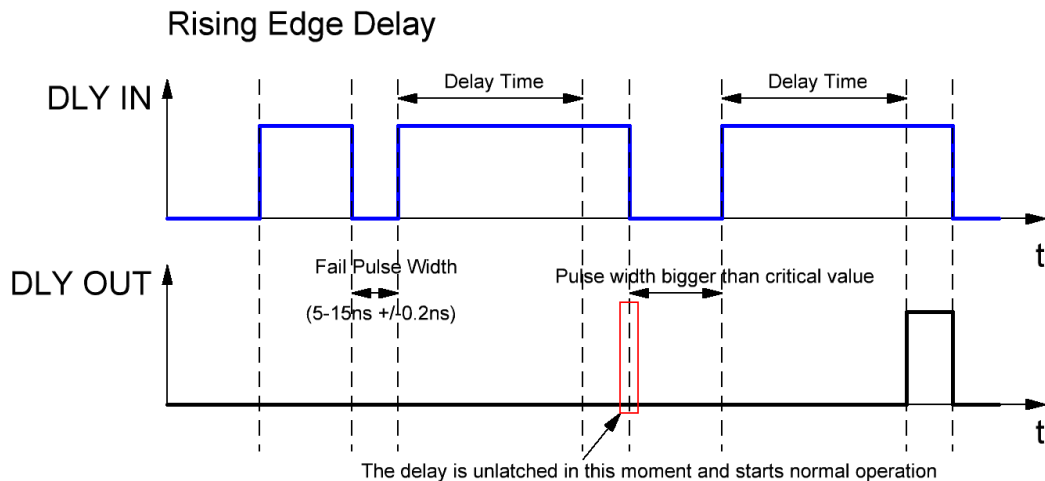
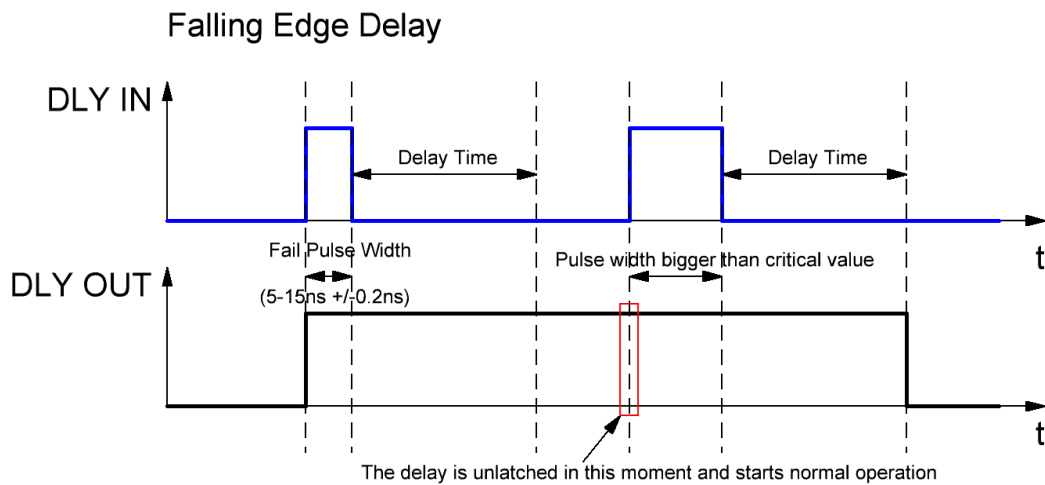


ISSUE 3: Delay Lock-up by a Short Pulse Functional Block Affected: Delay

Description:

The delay output could be latched despite the input change when a short pulse is input. For example, if the delay cell is configured as a falling edge delay, the short pulse (see NOTE) appears on its input the delay cell output will switch from LOW to HIGH but may not switch from HIGH to LOW even after the delay time has passed.

NOTE: The pulse width varies from chip to chip and with different VDD voltage. It is in range of 5-15ns and in the window $\pm 0.2\text{ns}$, so it should be very precise for issue happen.



Also, note that both edge delays does not have such issue.

Workaround:

- Use P DLY/FILTER block configured as a both edge delay or FILTER.



ISSUE 4: Device Damage by High Input Voltage on External Vref PIN of ACMP

Functional Block Affected: ACMPs

Description:

The device may be damaged by the voltage higher than 2V applied to IN- of ACMP as an external reference voltage.

Workaround:

- There is no workaround to this issue, avoid applying more than 2V on IN- of ACMP used as external voltage reference



SILEGO

Silego Technology**Corporate Headquarters**

1515 Wyatt Drive
Santa Clara, CA 95054
USA
Phone: 408-327-8800

Silego Taiwan Office (Hsin Chu)

6F-12, Number 38, Tai Yuan Street
Tai Yuan Industrial Park, Jhubei City
Hsin Chu County, 30265, Taiwan
Phone: +886-3-560-0313
Fax: +886-3-560-0316

Silego Taiwan Office (Taipei)

9F, No.10, Ln. 321, Yangguang St,
Neihu District,
Taipei City 114, Taiwan
Phone: +886-2-2658-1038

Silego Japan Office

20F Shinjuku i-Land Tower
6-5-1 Nishi-shinjuku, Shinjuku-ku,
Tokyo 163-1320
Phone: 03-6830-5035
Fax: 03-3348-7515

Silego Korea Office (Seoul)

#402 Dongmun Building, 10,
Dogok-ro 2-gil, Gangnam-gu,
Seoul, Korea (Post code: 06258)
Phone: +82-3453-7560 or
+82-2-3453-7127

Silego Korea Office (Suwon)

#101-801 Hanwha-Ggumegreen-Hyowon,
1116-3 Ingye-dong, Paldal-gu,
Suwon-si, Gyeonggi-do, Korea

Silego China Office (Hefei)

Rm303, Building 2, No3 TianYuan Rd
High-Tech Zone
Hefei, China 230088
Phone: +86-551-65368431
Fax: +86-551-65368432

Silego Ukraine Office

Business Center Intercity-Silego
Chervonoi Kalyny ave., 62a, 5th Floor, Room 5.1
Lviv, Ukraine
Phone: +38(032)232-80-53

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