

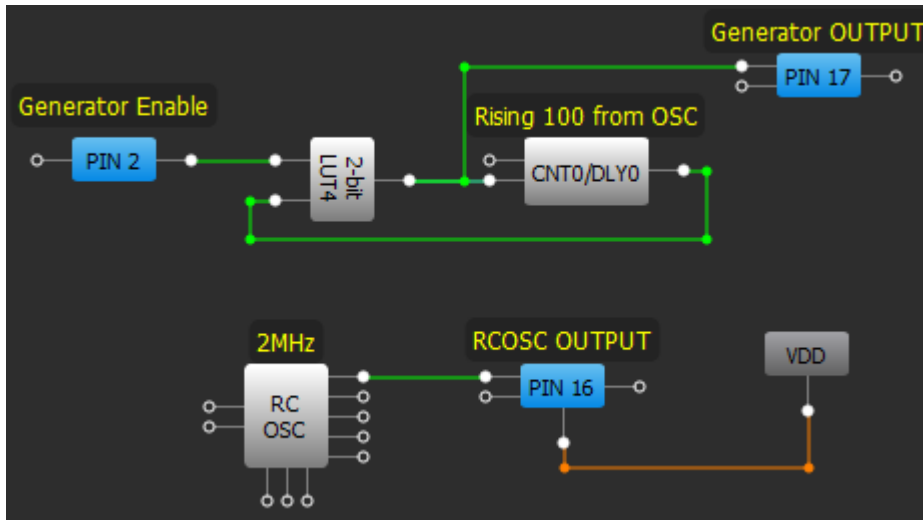


Errata disclaimer: This Errata applies to SLG46722 revision 5XE.

ISSUE 1: Long RC OSC Settling Time Functional Block Affected: RC OSC, Counter, Delay Description:

The RC OSC has a longer settling time when configured as 2 MHz with Auto Power On in the designs that have very short RC OSC disable time.

An example of such issue is in the following configuration:

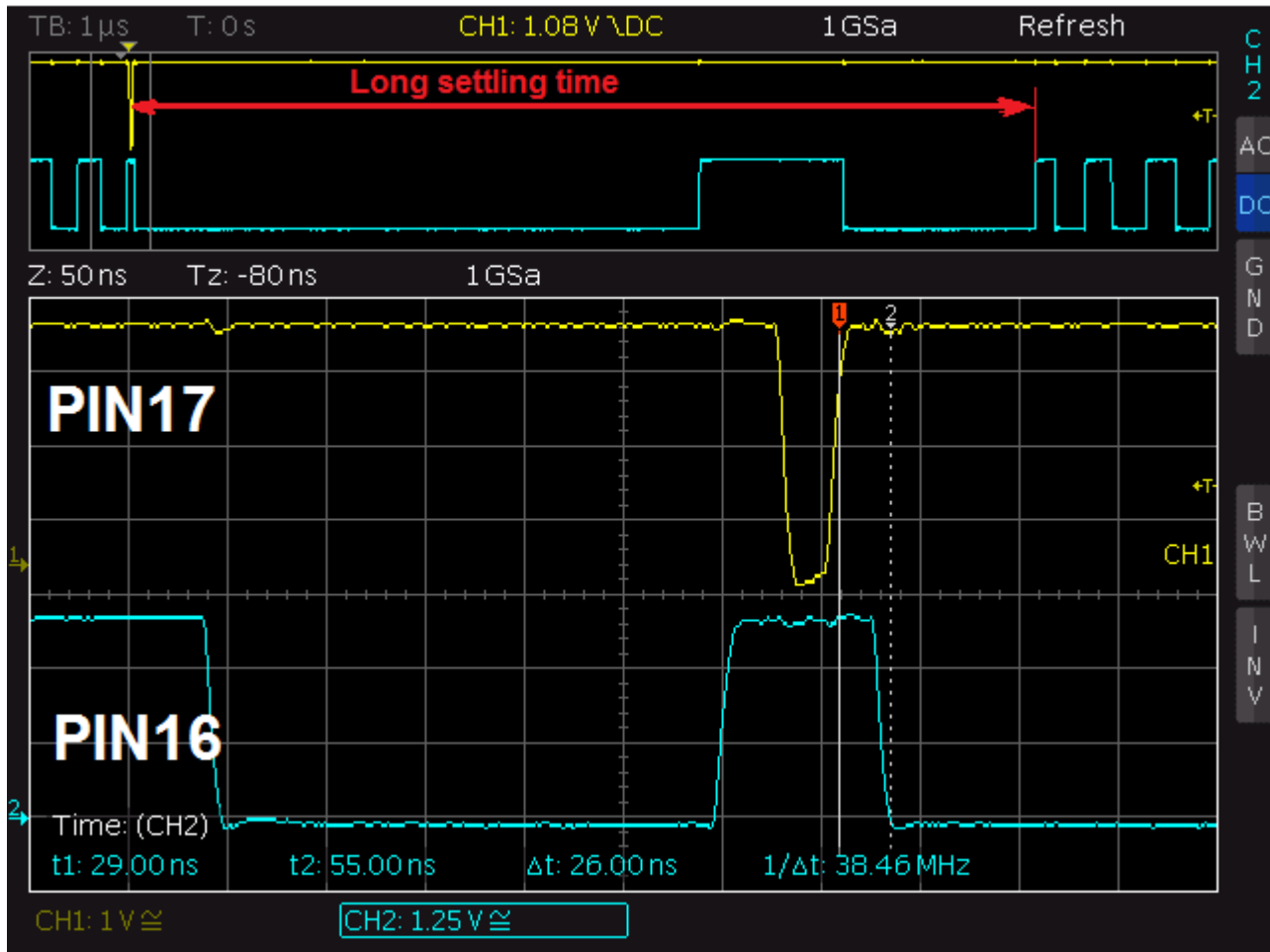


2-bit LUT4		
IN1	IN0	OUT
0	0	0
0	1	0
1	0	1
1	1	0

RC OSC	
RC OSC Power register:	Auto Power On
Clock selector:	RC OSC
RC OSC Frequency:	2000.00 kHz

14-bit CNT0/DLY0	
Mode:	Delay
Counter data:	100 (Range: 1 - 16383)
Delay time:	0.0512 ms Formula
Edge select:	Rising

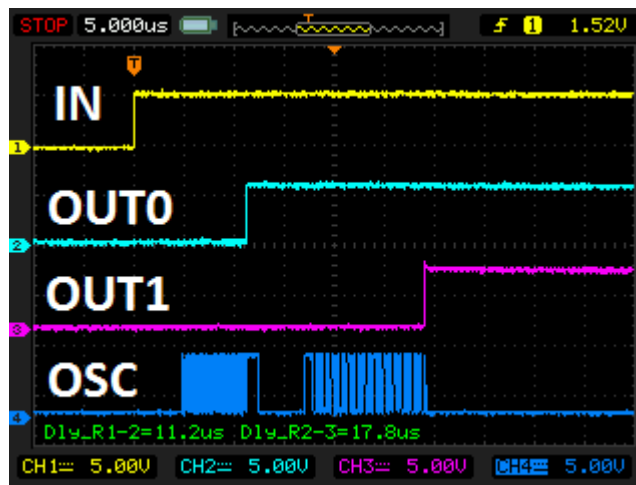
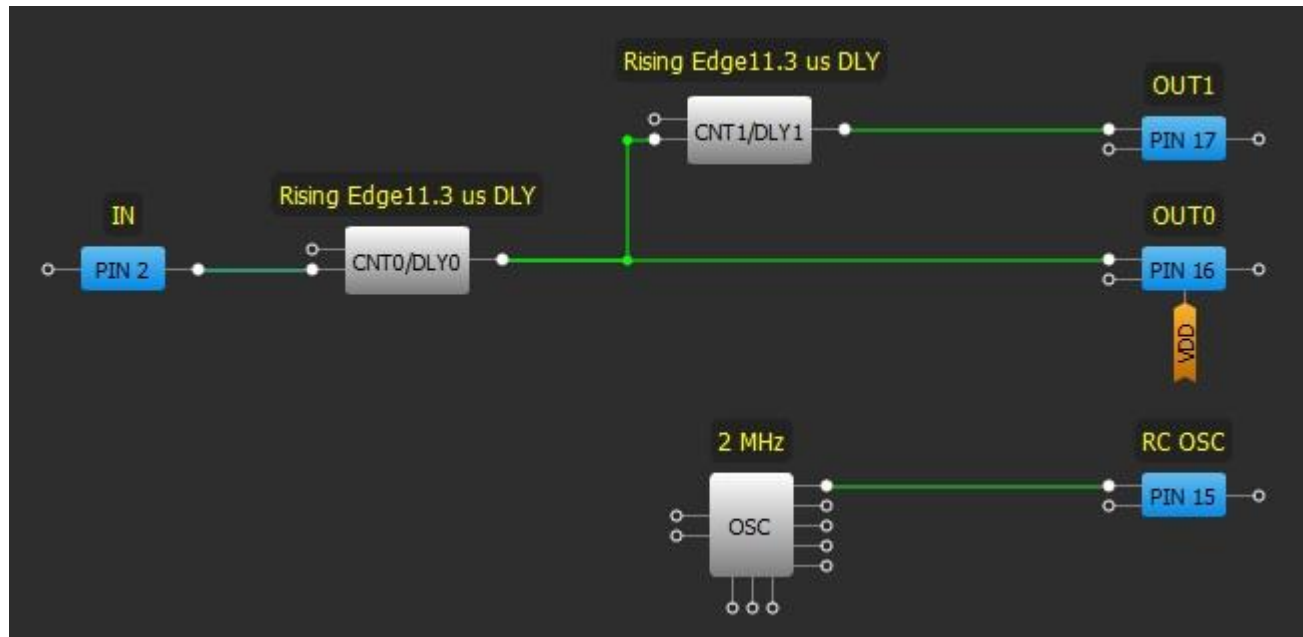
The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a high signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.



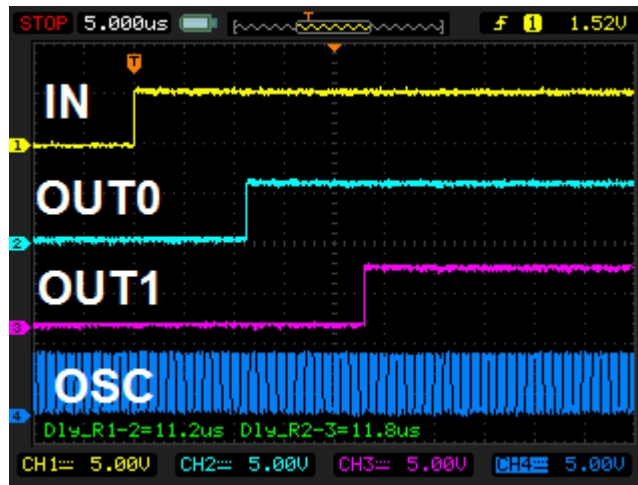
Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

The same situation occur while using two connected delays (all edge detect types except for a pair “Rising edge DLY – Falling edge DLY”).

In the following example, Delay0 and Delay1 are configured in the same way. However, Delay1 time is 17.8us instead of expected 11.3us (Delay0 time).

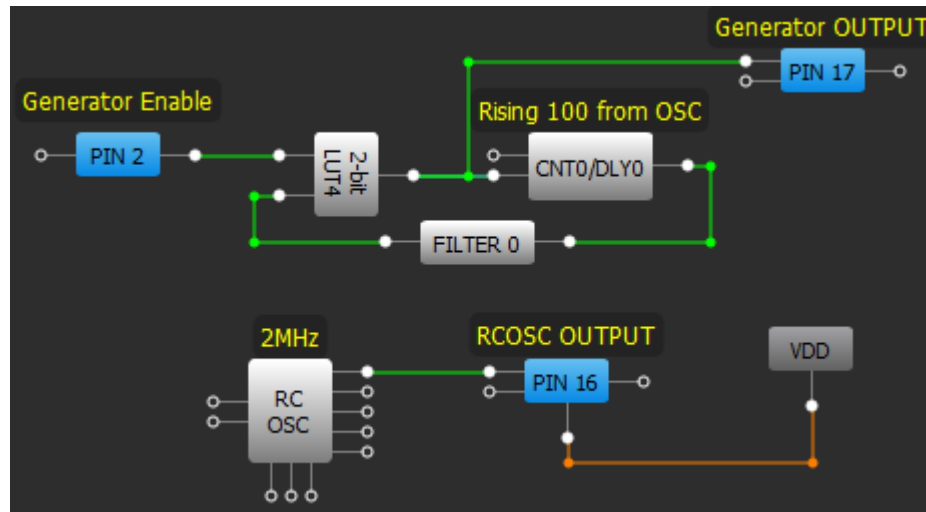


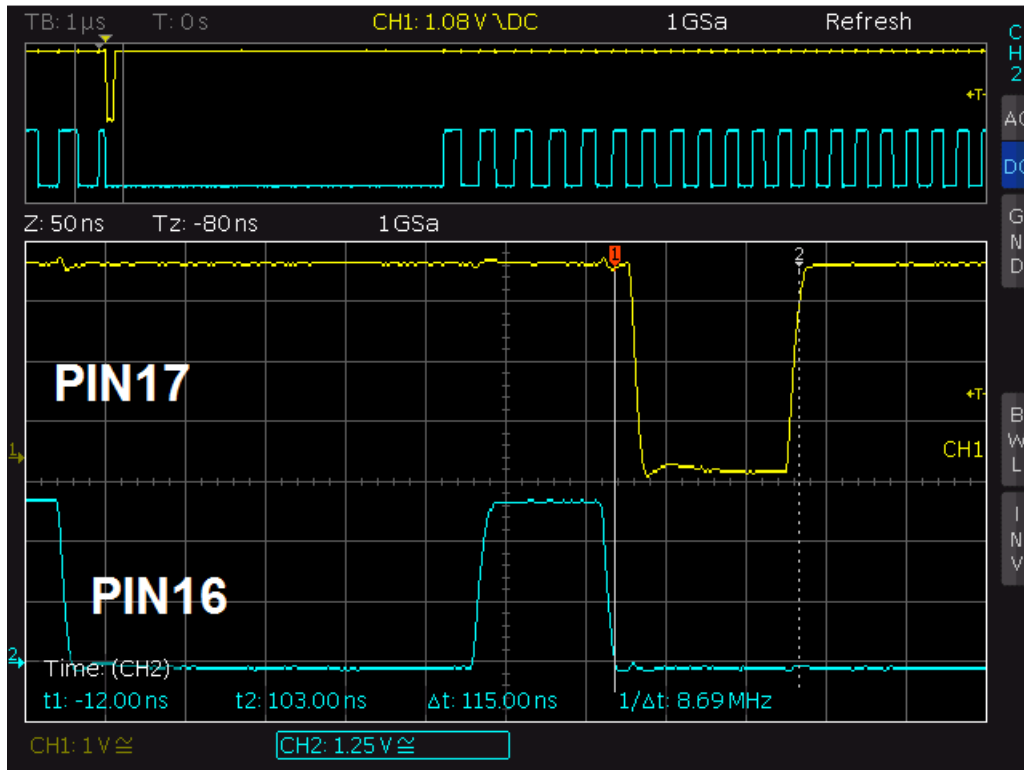
If there are some inner blocks which use RC OSC at the moment or RC OSC is forced power on when such error appears, RC OSC will be operational and delay value will be proper.



Workaround:

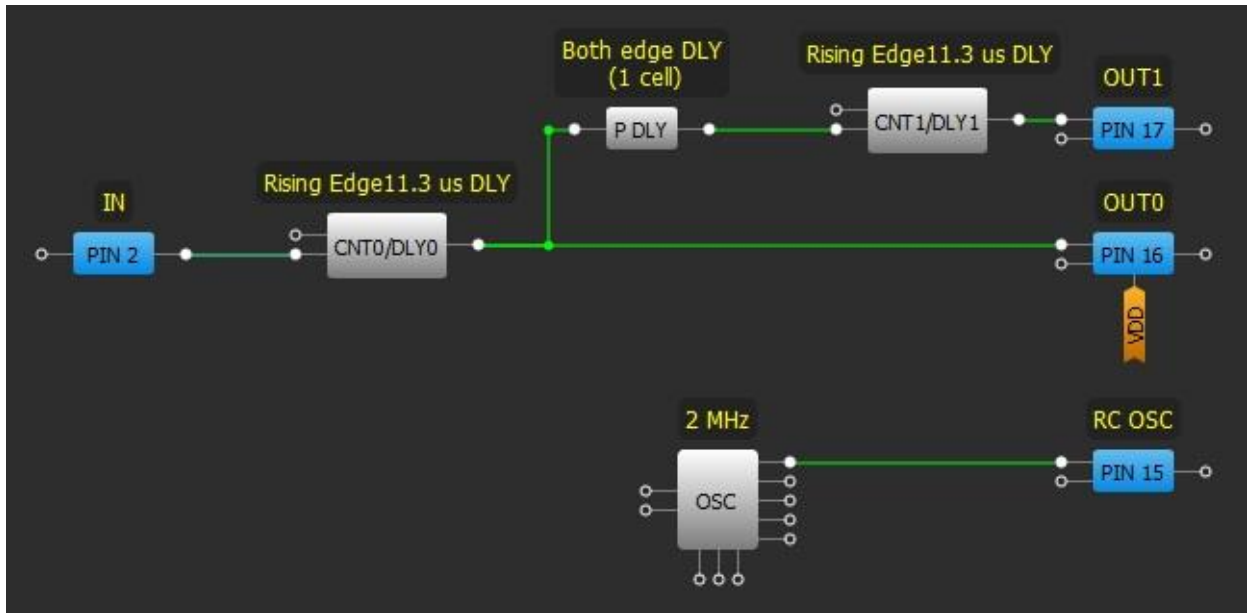
- In first case use block with longer propagation time. For example a Filter cell with an inverted output. Using two Filters in series or P DLY blocks in both edge delay mode (Delay time is 1 cell) for low power supply value (<3.3V) will result in a longer disable RC OSC time.





Channel 1 – 2-bit LUT4 output; Channel 2 – RC OSC output

- Using two delays in series (except for a pair “Rising edge DLY – Falling edge DLY”) use one Filter cell or P DLY between delay blocks. Using LUTs won’t help in this case.



- Use the “Force power on” RC OSC power control option to make the RC OSC operate at all times.

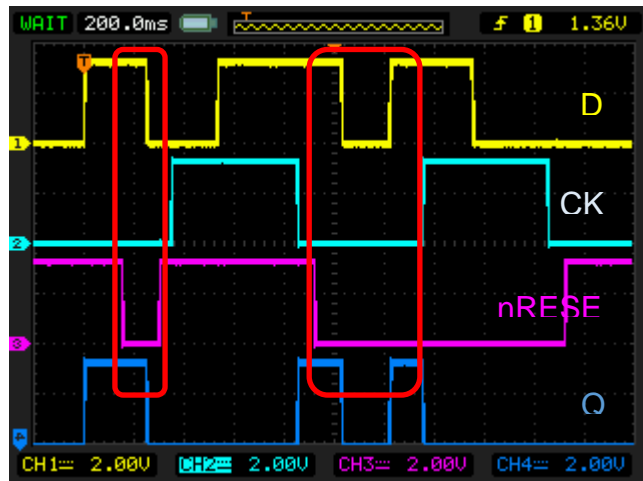
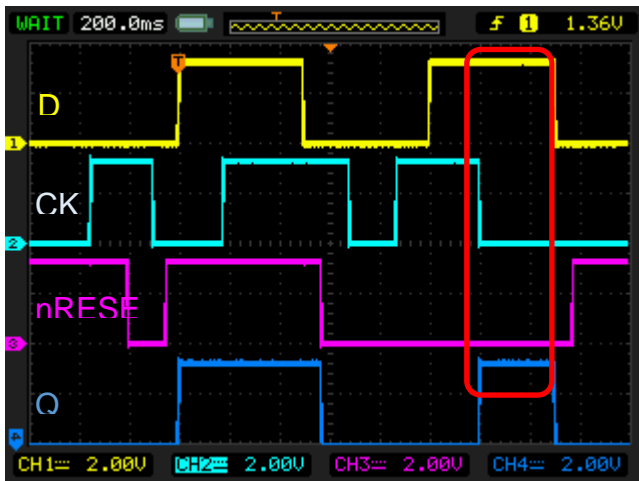
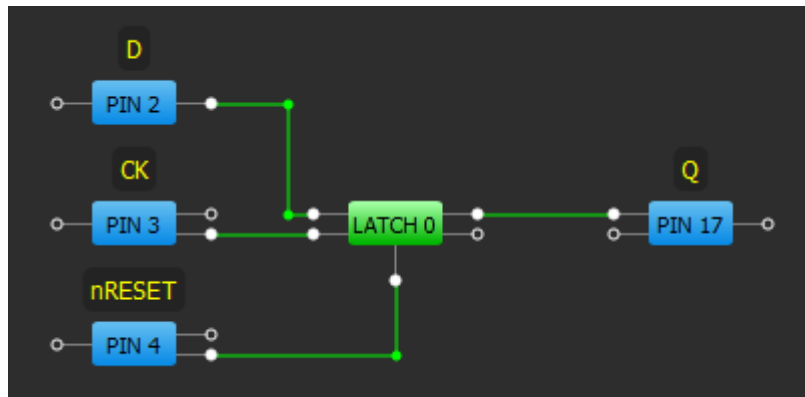


ISSUE 2: LATCH Block nRESET Incorrect Operation

Functional Block Affected: LATCH

Description:

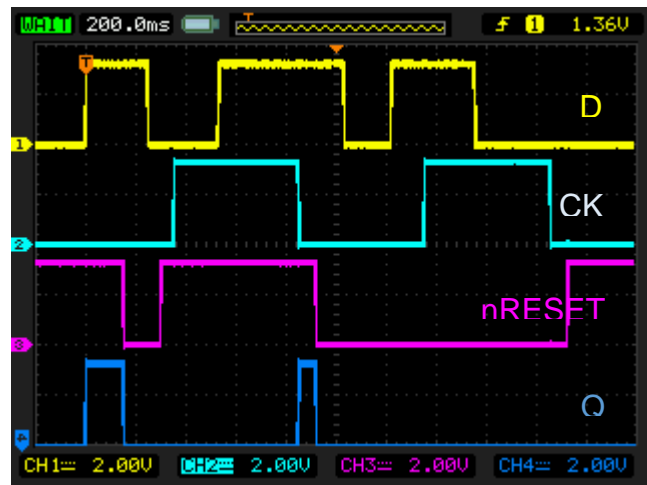
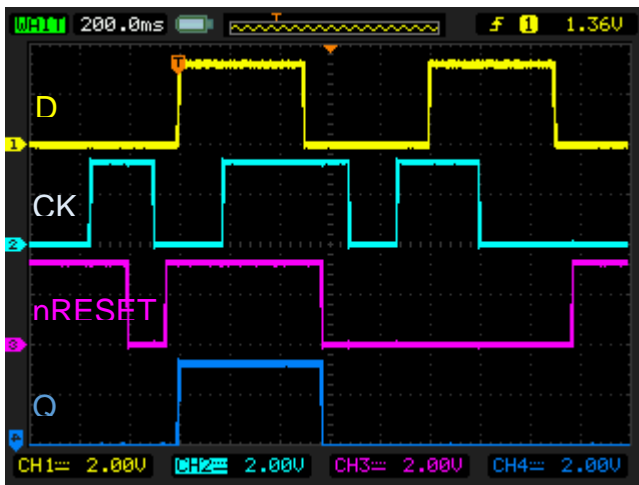
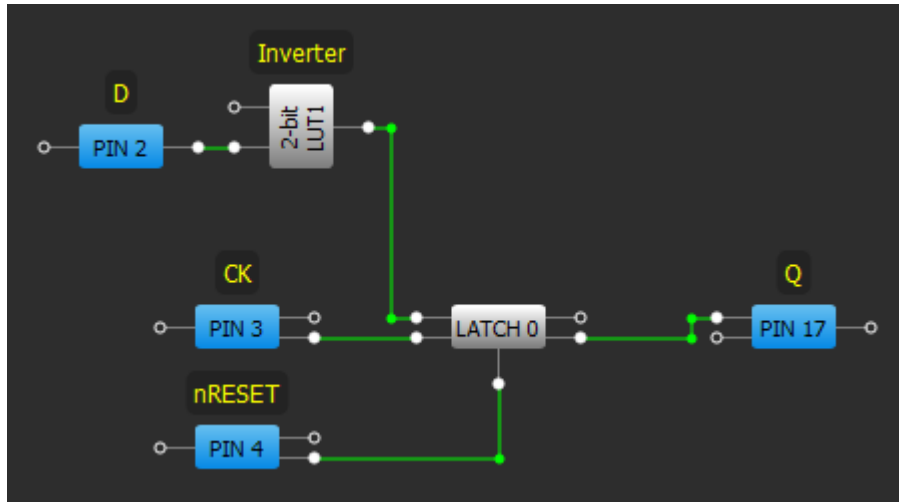
The reset function in LATCH blocks does not operate correctly. This can be described as function failure when nRESET input is set LOW.



The scope shots shown above show the incorrect nRESET function operation marked with red rectangles. From these waveforms can be seen that the reset function operates only when the CK signal is HIGH, in all other cases it is inoperational.

Workaround:

- Avoid using nRESET function in LATCH blocks in SLG46721/722 devices, if possible use SLG46110/120 devices, where this function operates correctly.
- Use nSET configuration, initial state HIGH, add inverter on D input and use nQ (inverted) output of the LATCH block:



ISSUE 3: Delay Lock-up by a Short Pulse Functional Block Affected: Delay

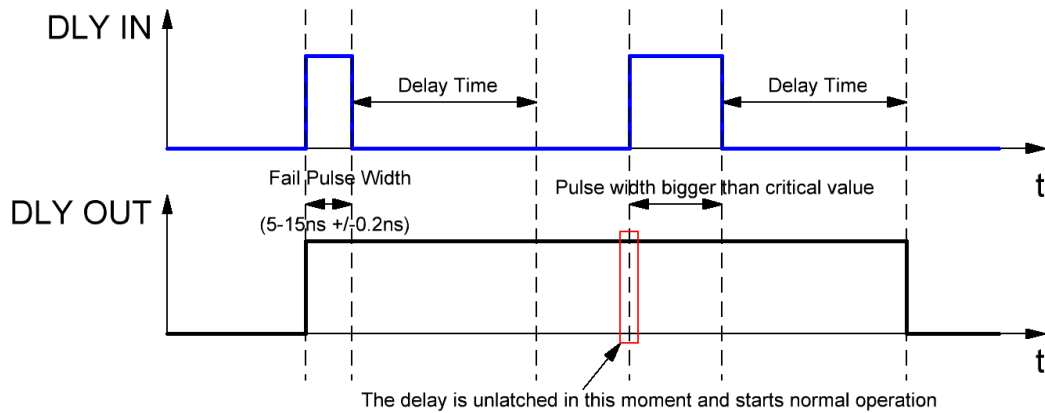
Description:

The delay output could be latched despite the input change when a short pulse is input. For example, if the delay cell is configured as a falling edge delay, the short pulse (see NOTE) appears on its input the delay cell output will switch from LOW to HIGH but may not switch from HIGH to LOW even after the delay time has passed.

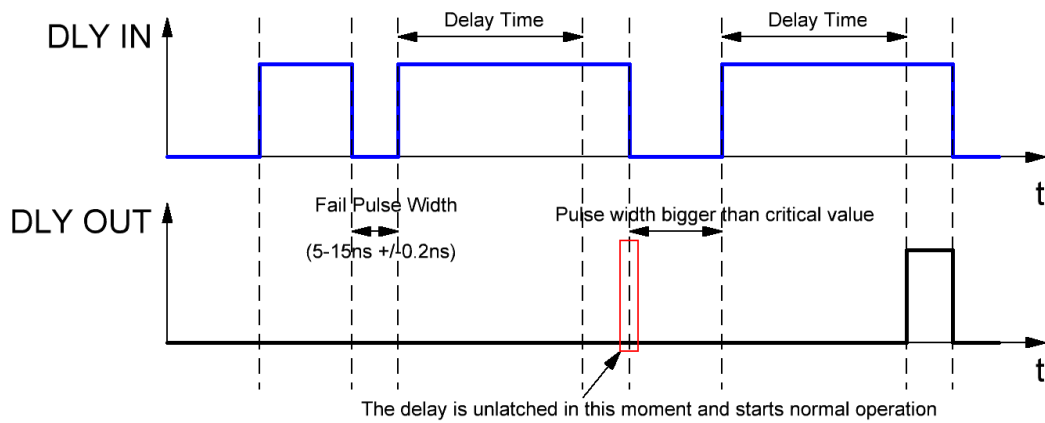
NOTE: The pulse width varies from chip to chip and with different VDD voltage. It is in range of 5-15ns and in the window +/-0.2ns, so it should be very precise for issue happen.



Falling Edge Delay



Rising Edge Delay



Also, note that both edge delays does not have such issue.

Workaround:

- Use FILTER block on the Delay block input;
- Use P DLY block configured as a both edge delay.



SILEGO

Silego Technology**Corporate Headquarters**

1515 Wyatt Drive
Santa Clara, CA 95054
USA
Phone: 408-327-8800

Silego Taiwan Office (Hsin Chu)

6F-12, Number 38, Tai Yuan Street
Tai Yuan Industrial Park, Jhubei City
Hsin Chu County, 30265, Taiwan
Phone: +886-3-560-0313
Fax: +886-3-560-0316

Silego Taiwan Office (Taipei)

9F, No.10, Ln. 321, Yangguang St,
Neihu District,
Taipei City 114, Taiwan
Phone: +886-2-2658-1038

Silego Japan Office

20F Shinjuku i-Land Tower
6-5-1 Nishi-shinjuku, Shinjuku-ku,
Tokyo 163-1320
Phone: 03-6830-5035
Fax: 03-3348-7515

Silego Korea Office (Seoul)

#402 Dongmun Building, 10,
Dogok-ro 2-gil, Gangnam-gu,
Seoul, Korea (Post code: 06258)
Phone: +82-3453-7560 or
+82-2-3453-7127

Silego Korea Office (Suwon)

#101-801 Hanwha-Ggumegreen-Hyowon,
1116-3 Ingye-dong, Paldal-gu,
Suwon-si, Gyeonggi-do, Korea

Silego China Office (Hefei)

Rm303, Building 2, No3 TianYuan Rd
High-Tech Zone
Hefei, China 230088
Phone: +86-551-65368431
Fax: +86-551-65368432

Silego Ukraine Office

Business Center Intercity-Silego
Chervonoi Kalyny ave., 62a, 5th Floor, Room 5.1
Lviv, Ukraine
Phone: +38(032)232-80-53

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