



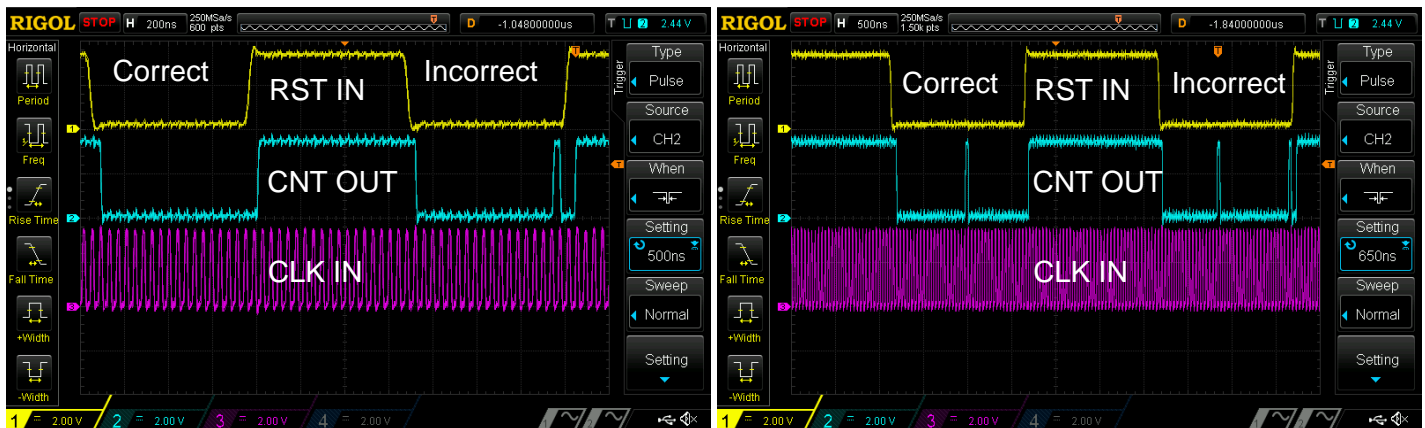
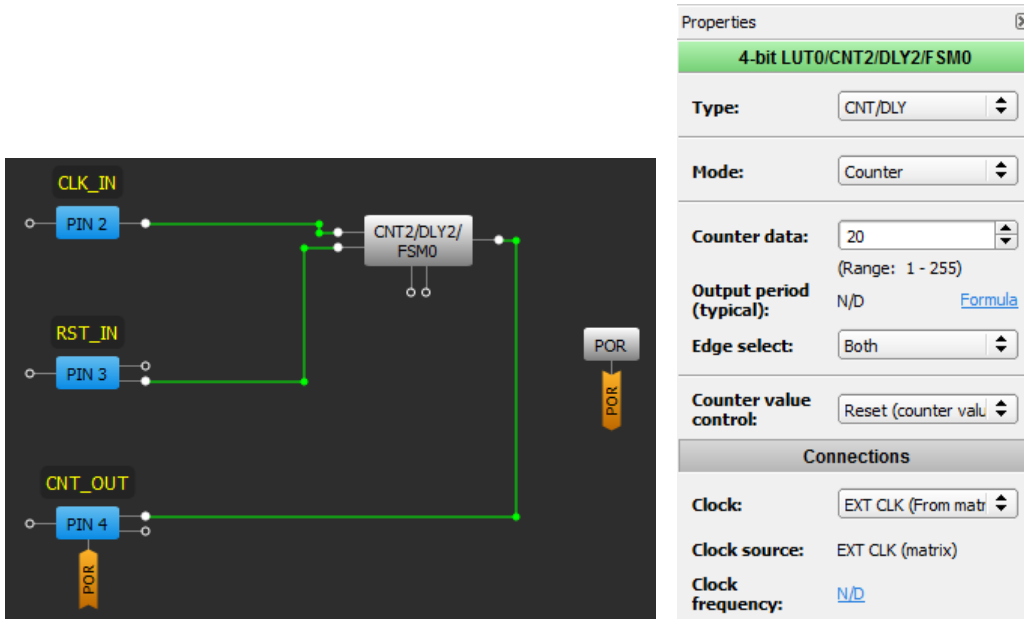
Errata disclaimer: This Errata applies to SLG46108 revision YA.

ISSUE 1: Incorrect Counter Operation after the Reset

Functional Block Affected: Counter

Description:

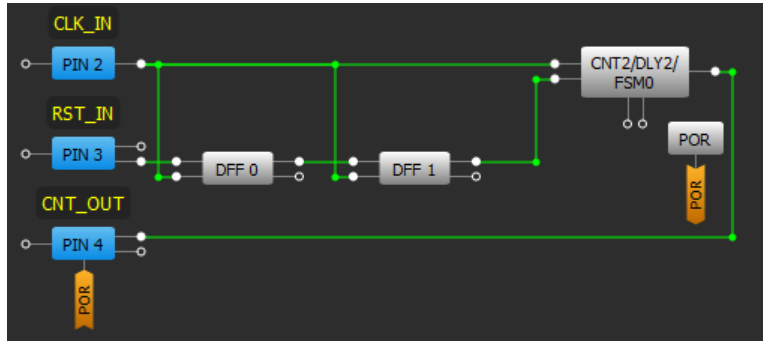
If the Counter Reset is asserted at the same time as a rising clock edge, it is possible that the Counter Data will be reset incorrectly and the counter output may appear faster than expected. This phenomenon appears more often as the clock frequency increases.





Workaround:

- Synchronize the RESET input of the Counter with its CLK using 2 DFF cells as shown in the image below.



ISSUE 2: VDD Noise Influences OSC Variation
Functional Blocks Affected: OSC, Counter/Delay

Description:

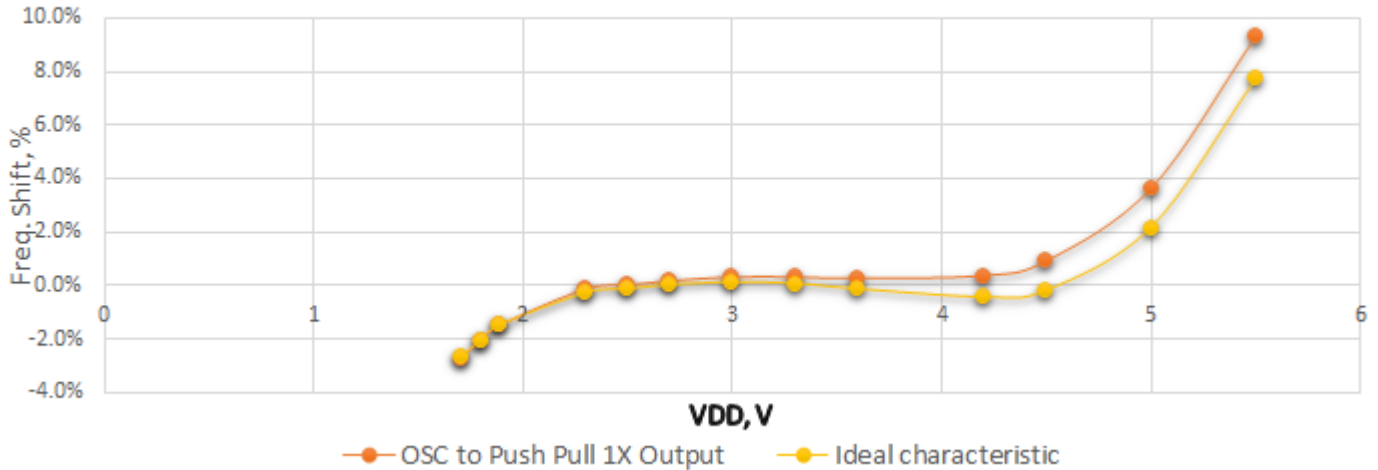
While applying some high frequency noise to the VDD, OSC inaccuracy may increase. The same behavior is also present in cases where high frequency switches are outputted from the chip using the Push Pull type driver. See, test results below.

Additional frequency Shift by different PINs

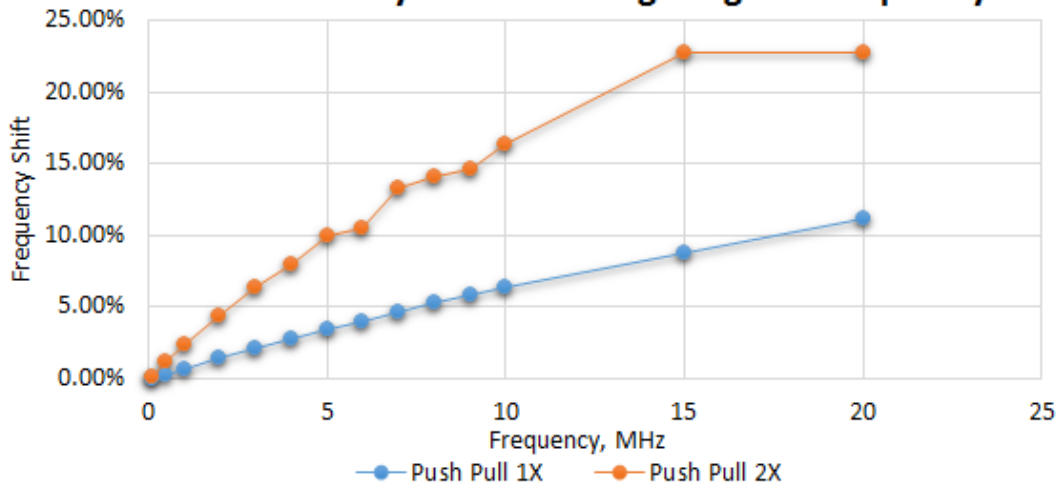
VDD =5V Trim VDD = 3.3V	Push Pull 1X	Push Pull 2X	Push Pull 1X	Push Pull 2X
OUT PIN #	f shifted, %	f shifted, %	average	average
4	1.42%	3.63%	1.52%	3.81%
6	1.67%	4.03%		
7	1.62%	3.98%		
8	1.38%	3.59%		
4 ... 8	6.73%	11.98%		



OSC Accuracy vs VDD



OSC Accuracy vs Pass-through Signal Frequency



Workaround:

Currently there are no viable workarounds for this issue.

However the issue can be minimized by doing the following:

- Only use frequencies lower than 2 MHz when switching the output
- Do not use parallel PIN connections to output high speed switching signals.



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