I2C Level Shifter

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Introduction

I2C level-shifters are very useful when two I2C-enabled devices need to communicate to each other across different voltage domains (VDD). This problem occurs often when new designs with lower VDD are added to existing designs with higher VDD. Silego Technology's dual-rail programmable logic IC can be programmed to function as an I2C level-shifter. This application note explains how to build an I2C level-shifter that meets I2C Fast Mode specs, which has a max data rate of 400kbps.

System View

I2C is a simple two wire serial protocol consisting of serial clock (SCK) and serial data (SDA. The GreenPAK takes the SCL and SDA buses at one VREF level and shifts them to another SCL and SDA bus at a second VREF level. These SCL and SDA buses are open drain NMOS pulled up to their respective VREFs. See Figure 1 for a block diagram view of the level-shifter. Inside the GreenPAK, level buffered IOs translate signals across different voltage domains and use digital switching to arbitrate input and output without a direction pin. There is no voltage difference requirement between VREF1 and VREF2, which is an advantage over analog solutions. The enable pin turns off internal oscillator to save power when level shifting is not needed.

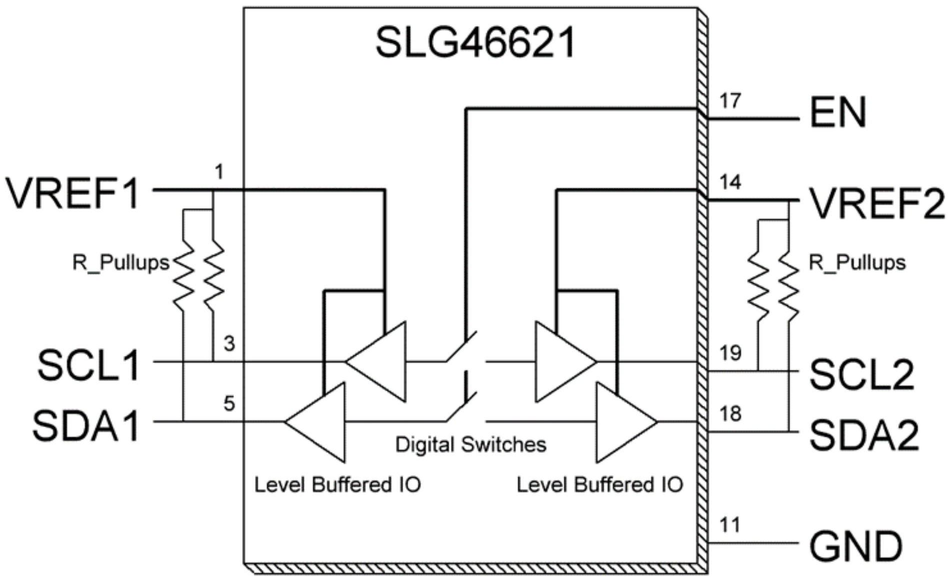

Figure 1. System Level I2C Level-shifter Block Diagram

GreenPAK Configuration

By using a handful of small lookup tables (LUTs) and delay macro cells, a dual-rail GPAK can be configured as an I2C level-shifter. Figure 2 shows the full PAK schematic. The top half connects the SCL while the bottom half connects the SDA. The AND gates are pass gates controlled by the enable signal (EN). The NOR gates control the Output Enable's (OE's) of each GPIO. When OE is low, the pin becomes a high impedance input pulled to VREF by an external resistor. When OE is high, the pin becomes an open drain NMOS output pulling to GND. The ports, labeled P0/P1/P10/P11/P18 connect signals between the two matrices of the SLG46620V. The DLY blocks feed a delayed falling edge back from the NOR gates.

When the bus is idle (logic high), all I2C pins are pulled high externally. During this time these GPIOs are in a high impedance input mode set via the OE pins. As soon as one input is externally pulled low, the inversion through the NOR gate will drive OE line HIGH, which causes the pin to pull low. When the input lets go and is pulled high by the external resistor, a short delay holds the OE signal, to account for slow rise times of pulled up signals.

Let's analyze an example when a signal propagates from the VREF1 side (left) to the VREF2 side (right), or from Pin 3 to Pin 19. When the bus is idle, Pins 3 and 19 are high and all macro-cell outputs are LOW.

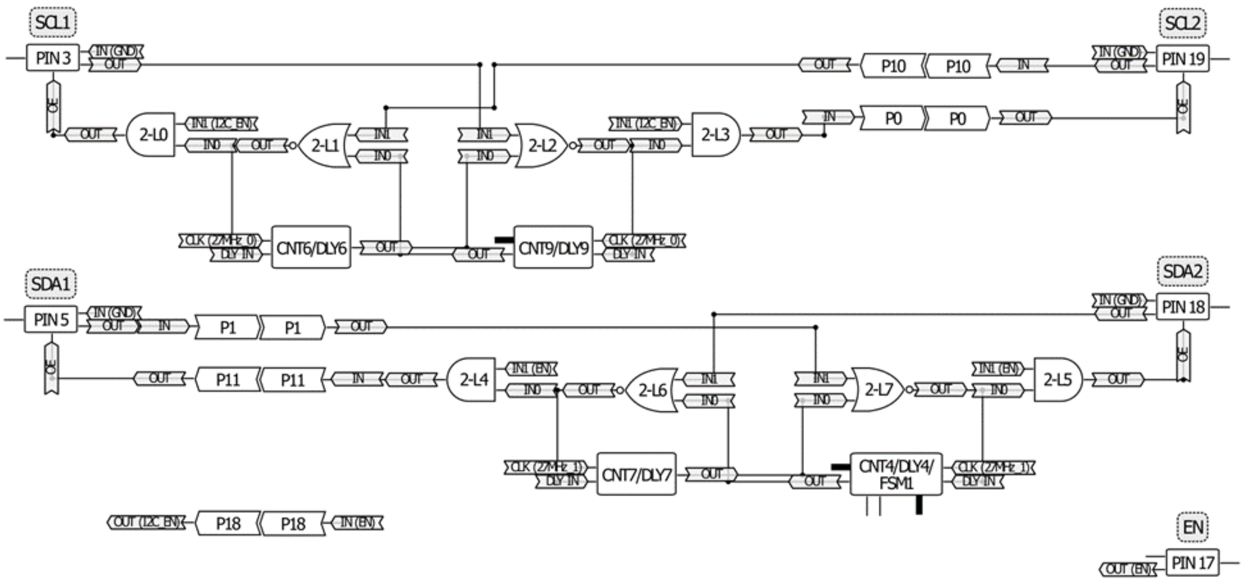

Figure 2. I2C Level-shifter Schematic

When Pin 3 is pulled LOW externally by an I2C device, this LOW signal will be sent to the 2-L2 NOR gate. If the other input is already LOW, the NOR gate will output a HIGH to the 2-L3 AND gate. If the enable is HIGH, the AND gate will output HIGH and change Pin 19 from input mode to output mode. Since Pin 19 is tied to GND in output mode, it will output LOW and pull the 1.8V bus to ground. This completes the Pin 3 high to low signal propagation.

When the I2C device releases Pin 3 from GND, it is pulled back to VDD. This action will send a HIGH signal to the 2-L2 NOR gate, which causes its output to transition LOW and to turn Pin 19 back to an input. The high-z state of the input pin allows the pull-up to return the voltage to 1.8V. The OE transition low is held by DLY9 for a short period to force pin 3 as an input through 2-L1 while the pull-up resistor is transitioning low to high.

Conclusion

Since the SLG46621 is very flexible, a custom solution can be optimized to a specific I2C setup. Delay times, output strength, and internal pull-ups are among the customizable options for this level-shifter. The example design was done with a SLG46621V chip. One I2C level-shifter system uses about 20% of the SLG46621V's resources; this means that after implementing two I2C level-shifters, 60% of the chip's resources will still be available to implement other functionalities such as push button reset, power sequencing, or voltage supervision.

The SLG46532V could also be used to implement I2C level-shifter; it has built-in I2C slave function for added design flexibility. For a custom design that fits your system needs, please contact **sales@silego.com.**

Appendix

CH1 – PIN#3 (SCL1) with external pullup

CH2 – PIN#19 (SCL2) with external pullup

CH3 – PIN#05 (SDA1) with external pullup

CH4 – PIN#18 (SDA2) with external pullup

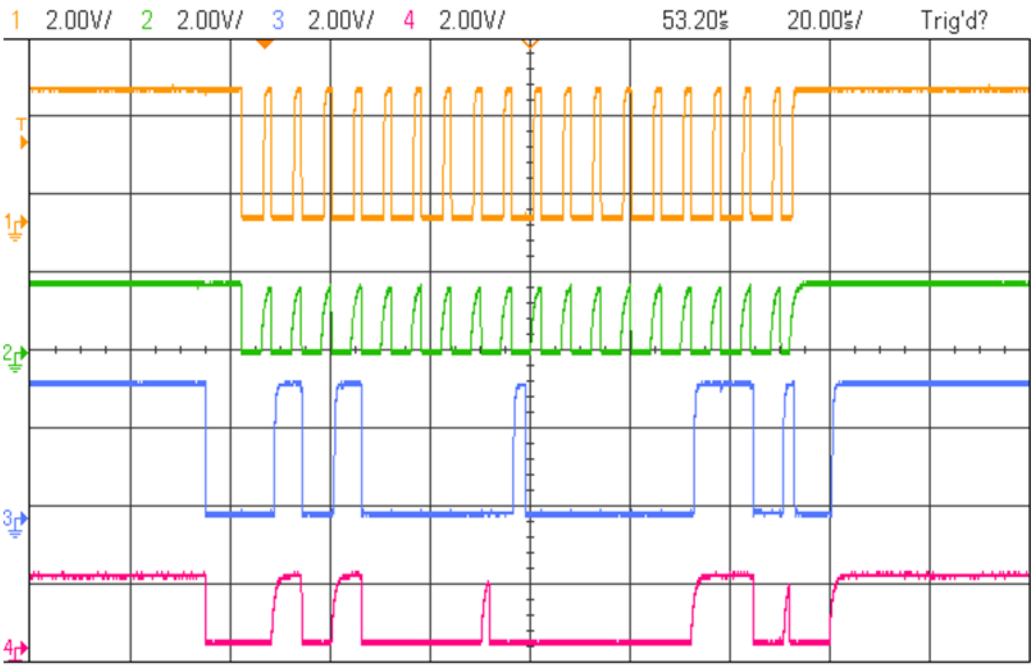

Figure 3. A Level-shifted I2C Message

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A	Roger Liang, Luke Thomas	05/09/2016	New application note

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