

## Introduction

DC motors are more and more frequently used these days, often replacing legacy AC motors because of increasing advantages in efficiency due to continuing improvements in controller hardware and driver methodologies.

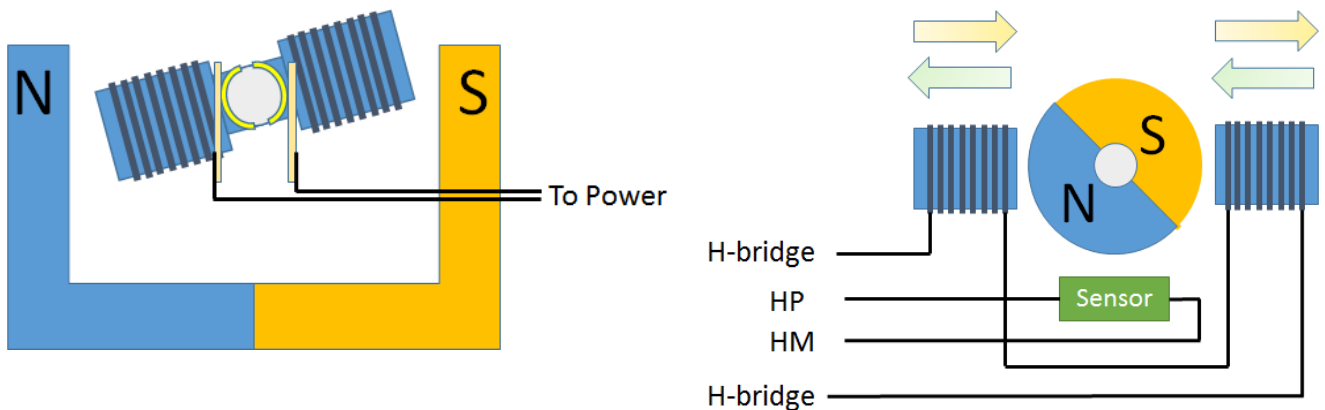
Among DC motors, brushless DC motors are prevalent in industrial applications as well as some of consumer applications as it has no abrasion from physical contact of brushes. Instead, you need to control the driving timings in accordance with the rotation angle sensed with magnetic sensor. Hall sensor is one of the most commonly used sensors.

A simple DC motor (on the left) and a brushless DC motor (on the right) that show the basic operation principles are described in Fig.1.

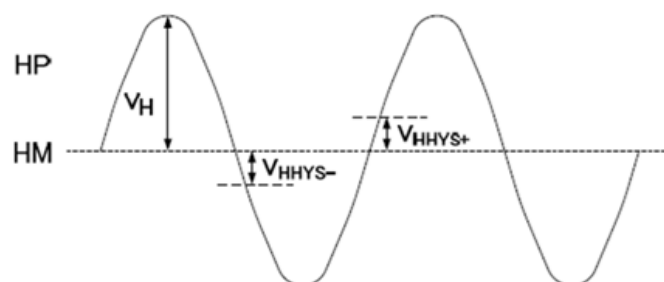
A DC motor (on the left) has a brush to switch the direction of current flow in rotor coil.

This changes the direction of magnetic field to control one end of the rotor pulled and the other end repelled by the stator magnet. In case of a brushless DC motor (on the right), it is necessary to control the current switching by not a brush but a driver in sync with magnetic sensor (hall sensor). The sensor output is fed into a controller that handles the timings and directions of current flow in the stator coil.

A typical hall sensor output waveform in a DC motor is in Fig.2. This signal has the same frequency as the rotation of the rotor. Usually the amplitude  $V_H$  is several tens of millivolts with a wide range of offset voltage.



**Figure 1. DC motor and Brushless DC motor**



**Figure 2. Hall sensor output**

In order to compensate for the offset and to obtain a square waveform from the hall signal an external op-amp or a comparator are recommended.

The rising edge of this square wave is used for generating drive signal timings as described below.

In this application note a single-phase brushless DC motor is discussed.

Fig. 3 shows an example of a brushless DC motor schematic with the components and their connections used in this system. HP and HM are from the hall sensor of the target motor representing its rotation angle and speed.

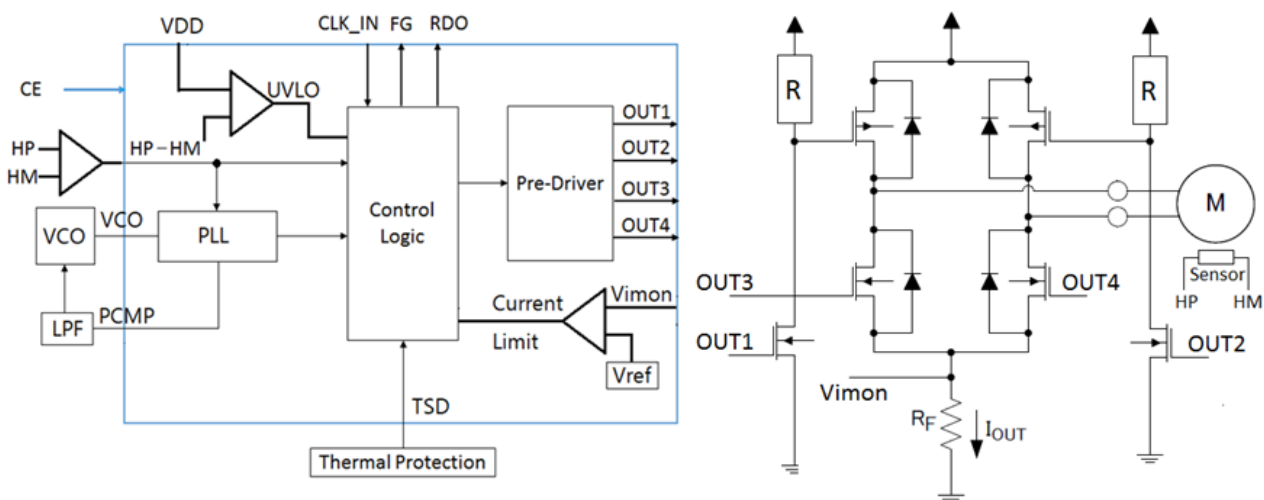
HP and HM voltage levels are compared to produce a square wave HP-HM. This signal works as the reference signal for PLL and as a selector signal for pre-driver outputs.

OUT1 to OUT4 are connected to H-bridge that drives the target motor.

Protection from rotation stuck, overcurrent, overheat and UVLO are incorporated to turn off H-bridge FET's.

A VCO (Voltage Controlled Oscillator) is placed in front of GreenPAK to synchronize with the hall sensor signals. The purpose of this synchronization is to time the soft start and soft stop of PWM driving signals. Soft start can be triggered by the transition edges of a hall sensor signal, while soft stop needs to be triggered at some point before the end of it. With a counter in sync with the hall signal, you should be able to program the counter value where to start controlling PWM duty cycle of the driving signal.

In constant rotation speed application PLL is not necessary. You only need program counter values for PWM duty cycle control.



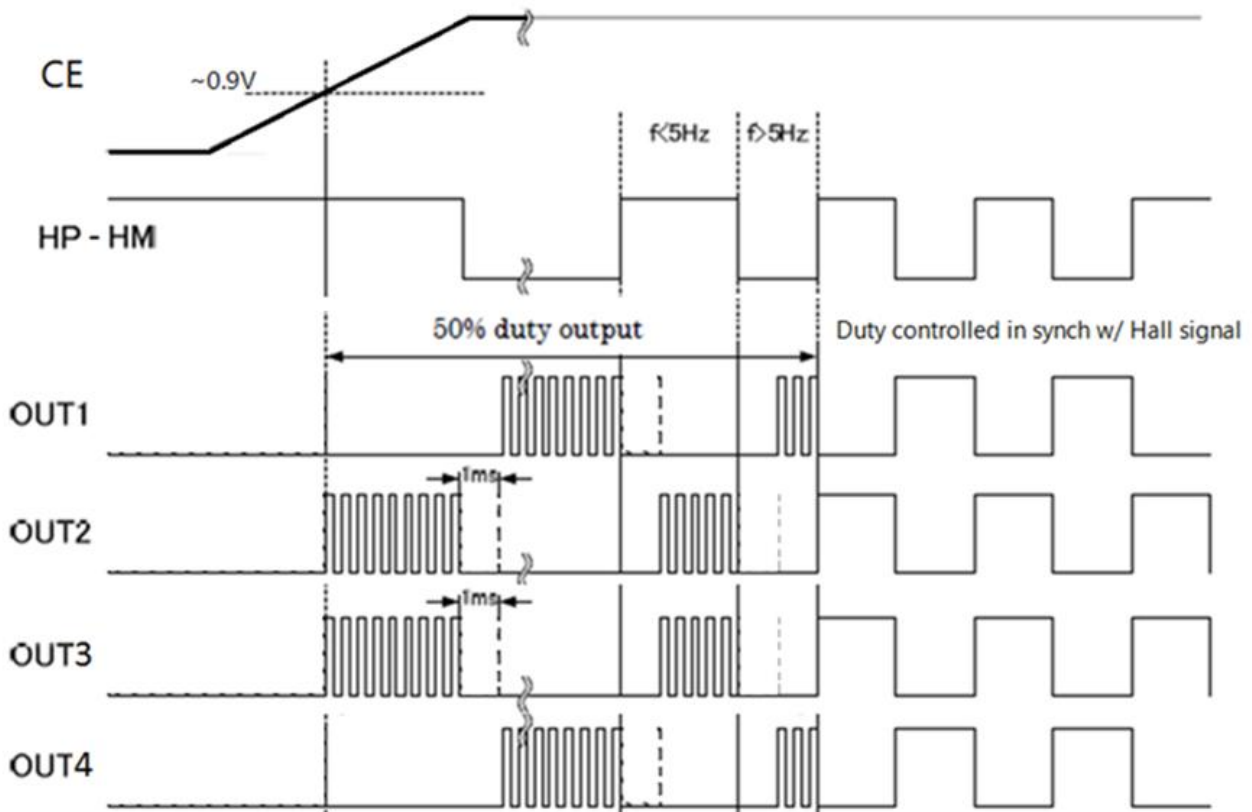
**Figure 3. BLDC motor driver configuration example**



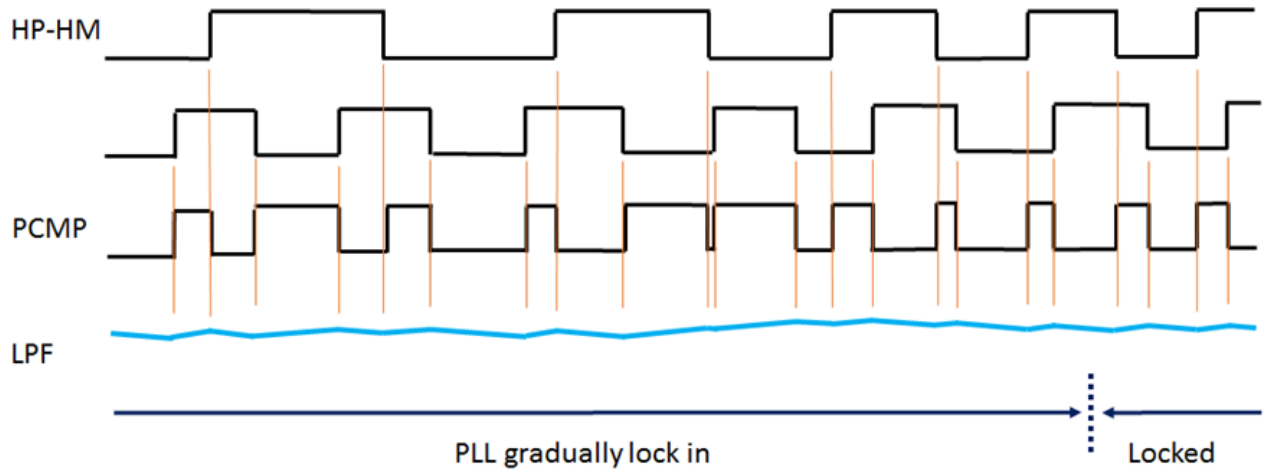
**Power on**

At power ON all I/Os of GreenPAK become high impedance until internal POR (Power On Reset) output turns from low to high. When CE input exceeds 0.9V, the internal circuits become active to drive the PWM outputs. Fig.4 shows the operation at start up.

At first, there is no rotation of motor and no hall sensor signal output. In this state VCO oscillates at its free-running frequency. With this VCO clock GreenPAK outputs PWM signals of 50% duty cycle at OUT1 and OUT2. Driven by this square waveform, the motor starts to rotate generating hall signals.



**Figure 4. Start-up sequence**



**Figure 5. PLL lock-in operation at start up**

Fig.5 shows HP-HM and VCO clock divided by counter lock in during start-up operation. Phase comparator (PCMP) output is fed to external VCO to control its frequency through a LPF (Low Pass Filter). When LPF output voltage increases, so does VCO frequency and vice versa. The LPF output voltage is an averaged PCMP output. When VCO divided clock is slower (lower frequency) than hall signal, the high period of PCMP output increases to increase LFP output voltage. This feedback loop continuously adjusts VCO frequency until PCMP output becomes constant. This is where VCO is synchronized with the hall signal. The counter and phase comparator are shown in Fig.7.

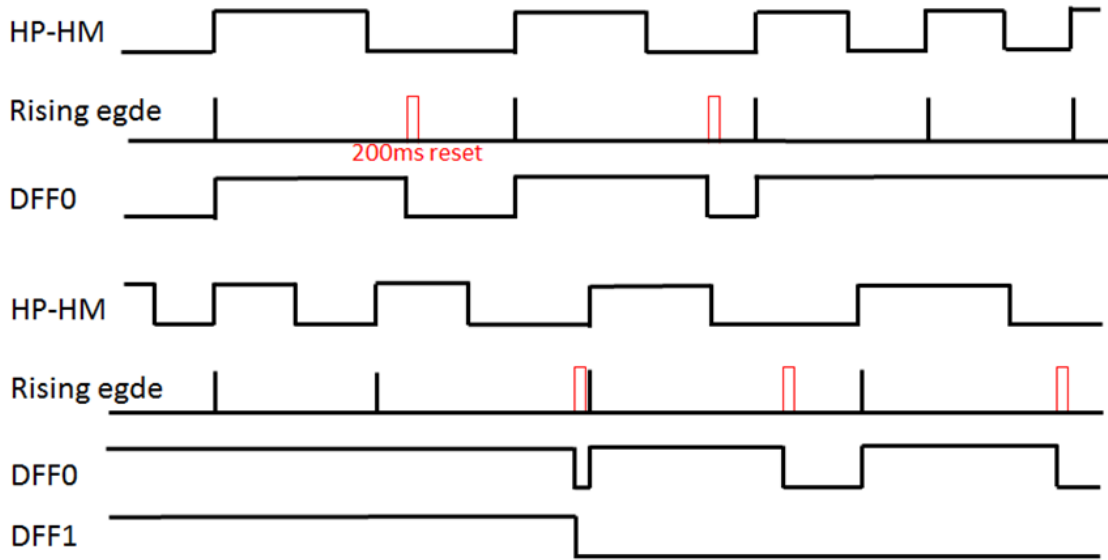
### Hall sensor signal detection

A hall sensor signal is connected to HP-HM to show the frequency and angle of rotation. At the initial driving state, the driver outputs PWM signals at 50% duty cycle.

When the frequency of the hall sensor input signal becomes 5Hz or higher, PWM output is switched from 50% duty to soft start operation (PWM duty cycle ramp).

H-bridge drive outputs in sync with hall signal and PLL lock in operation both at start-up are shown in Fig.4 and Fig.5 respectively.

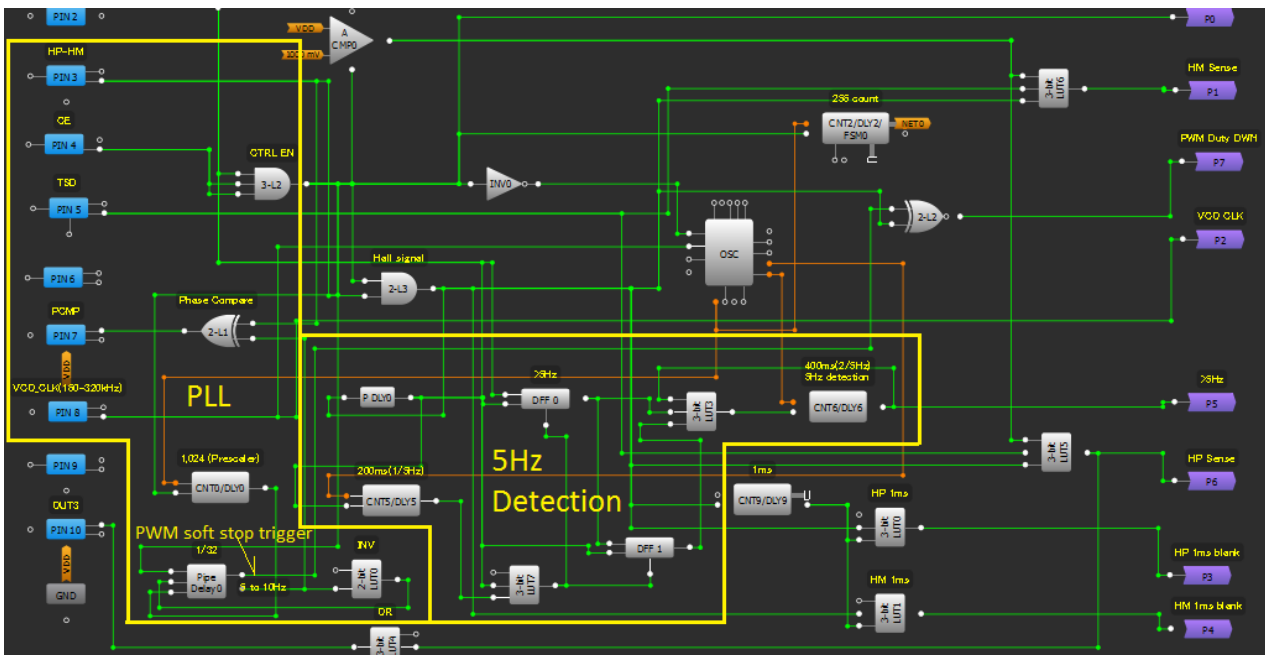
5Hz detection is performed by the following sequence. There is a 200ms timer (CNT5/DLY5) and a 400ms delay cell (CNT6/DLY6) for 5Hz hall signal detection. After power on and CE is asserted, the hall sensor input signal is fed into the reset of CNT5/DLY5 through rising edge detector. If the hall sensor signal frequency is lower than 5Hz, CNT5 resets DFF0 and DFF1; otherwise, their outputs stay high and the GPAK detects motor frequency to be faster than 5Hz.



**Figure 6. 5Hz detection timing**

On the other hand, when the motor frequency decreases below 5Hz, CNT5 resets DFF0 and DFF1. Unless the hall sensor signal has two rising edges within 200ms, DFF1 output stays low to negate DLY6 output.

Fig.6 shows the timings in detail. Corresponding schematic is in Fig.7.

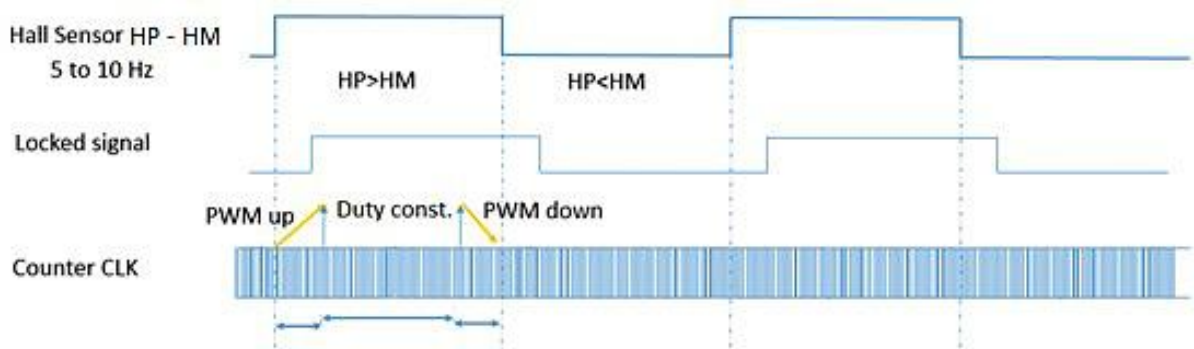


**Figure 7. PLL and 5Hz detection**

### Clock synchronization

In order to obtain a clock synchronized with the hall signal a PLL is composed with an external VCO and LPF (low pass filter), internal counter and a phase comparator. VCO clock is divided by 32,768 to be phase-compared with HP-HM waveform. Clock divider number of 32,768 was chosen to have 128 PWM cycles in one half of the rotation period so that it makes sense to control PWM duty cycles increase, keep and decrease within the period. VCO clock is also supplied to the control logic to generate PWM soft start/stop waveform.

In case of constant rotation frequency motor applications you would not need a PLL. You only need to program counters for PWM soft start/stop timings. And because GreenPAK (SLG46620V) has fixed programmed timings, the hall signal input frequency is assumed to be within 5 to 10Hz range suggesting that VCO frequency is roughly from 160k to 320kHz. There is a delay time shift in PLL depending on the frequency it locks. So there is a limitation in input hall signal frequency range for timing adjustments.



**Figure 8. PWM soft start/stop timings**

### Soft start operation

Soft start gradually increases the driving signal's PWM duty cycle and is, in this design, triggered at each HP-HM rising/falling edge. This operation is controlled by initializing FSM0 and FSM1 in sync with HP-HM. The FSM1 clock is slower than the FSM0 clock. At initialization, both FSM0 and FSM1 are set to a programmable counter value. And the values are compared with each other by DCMP0, where the PWM duty cycle is generated. The PWM duty cycle increase rate is controlled by the count value in CNT7/DLY7.

### Constant PWM duty cycle operation

When PWM duty cycle reaches the value defined by the register for DCMP1, the PWM reference counter CNT4/DLY4 keeps its value until DFF6 output (keeps signal for CNT4/DLY4) resets.

### Soft stop operation

PWM soft stop is triggered by a synchronous timing with the locked signal in Fig.8, where you start decreasing PWM duty cycle toward the hall sensor signal transition.

This timing is dependent on the PLL lock delay. Therefore, you need to adjust it after external components are selected and PLL waveform is confirmed. When the duty cycle reaches the lowest that is defined by a register of DCMP1, the duty is kept unchanged until the next trigger of soft start occurs.

### PWM control configuration

There are three PWMs used in this application: 50% duty cycle generation, minimum and maximum duty cycle definition and PWM driving signal generation. PWM period is determined by the count value and the clock source to FSM0 in Fig.4. PWM duty cycle is controlled by FSM1 in Fig.9 where its clock is sourced by CNT7/DLY7. In case you want different ramp speeds for duty increase and decrease, add another CNT/DLY cell. This CNT/DLY and CNT7/DLY7 must be multiplexed in accordance with UP pin of FSM1.

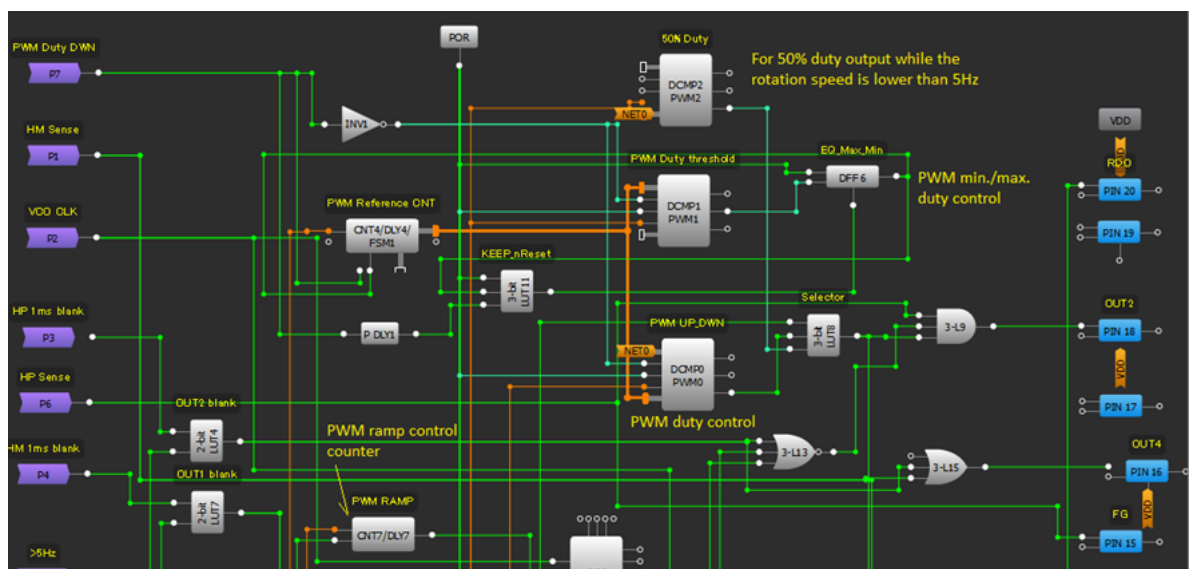
### Protection features

There are three protection features incorporated: lock (rotation stuck) detection, overcurrent detection and under-voltage lock out (UVLO). There is also a thermal shut down input pin to negate all the output pins with a "High" input.

Rotation speed is expressed by a hall signal frequency. A motor with the hall signal frequency less than 5Hz is considered to be in a locked state.

When a DC motor is under a torque larger than it can accommodate, the rotation stops and supply current increases. In order to avoid too much current drain, the lock detection is implemented through a series of logic blocks, where hall signal frequency is compared with a 400ms frequency signal.

If the rotation gets stuck, the output driver will pause for at least four seconds.



**Figure 9. PWM control with DCMPs**

The basic idea of protection is to turn off the H-bridge transistors by driving the gates low. In normal operation OUT3 and OUT4 drive the gates High for 1ms after each HP-HM transition to let the regenerated current flow.

Overcurrent in H-bridge is detected by external shunt resistor implemented in series with H-bridge to GND. The voltage across the shunt resistor is monitored by ACMP1 in Fig.10, where a short delay of microseconds is implemented at its output, in order to ignore inrush current immediately after switching.

ACMP0 in Fig.4 is for UVLO where VDD divided by internal voltage divider is compared to a reference voltage. TSD (thermal shut down) is a logic input to negate all the output driver pins for H-bridge. You could also use another ACMP to detect the analog level of a thermistor.

## Waveforms

Screenshots of PWM soft start/stop operations can be found in Fig.11 and Fig.12 respectively. PWM output (OUT2) starts to increase its duty cycle at the transition of hall sensor signal (HP-HM).

At a point, defined by the pipe delay, the PWM output starts to decrease its duty cycle. This delay is adjusted empirically so that the soft stop is completed before the next HP-HM transition.

The PWM duty increase/decrease rate is, in this case, determined by the CNT7/DLY7 count value. You can set these rates independently by using two different counter values.

CH1 (yellow): OUT1

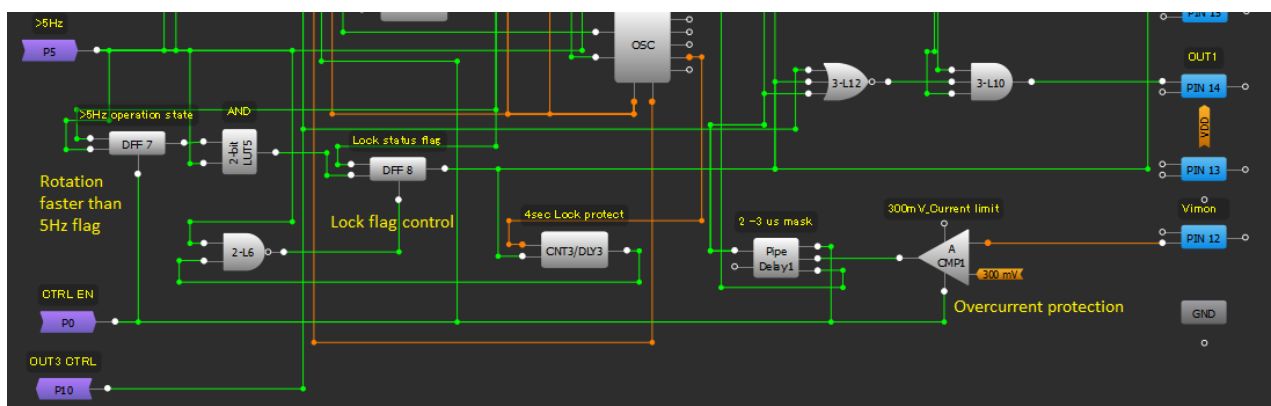
CH2 (light blue): OUT2

CH3 (pink): OUT3

CH4 (blue): OUT4

## Conclusion

A GreenPAK configuration applicable for a single-phase BLDC motor is introduced using SLG46620V (GreenPAK4). For flexibility a VCO and PLL are incorporated in order to output the drive signals synchronized with rotation angle. PWM soft start/stop operation is realized using counters and PWM controller.

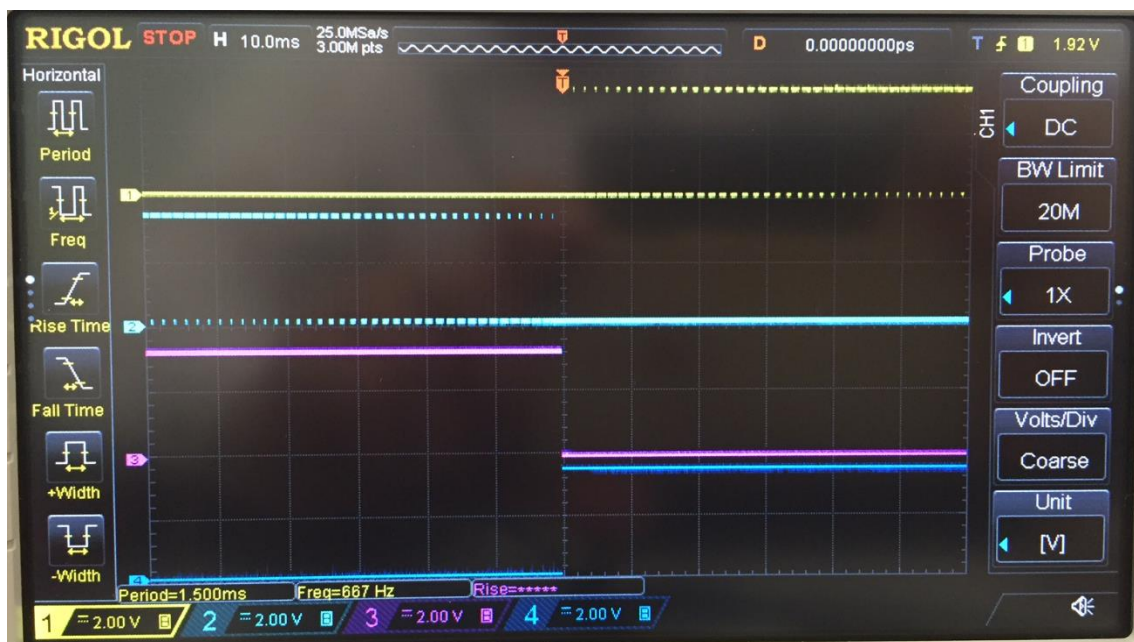


**Figure. 10 Rotation stuck and overcurrent protection**





**Figure 11. PWM 50% duty**



**Figure 12. PWM soft start/stop**



### **About the Author**

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**Document History**

Document Title: Brushless DC Motor Control

Document Number: AN-1114

<b>Revision</b>	<b>Orig. of Change</b>	<b>Submission Date</b>	<b>Description of Change</b>
A	Yuji Hishiki	07/15/2016	New application note

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