SLG8LP465

Low Power Clock Synthesizer for Intel mobile PCI Express

Features

- Low Power Intel CK410M solution
- Seven selectable CPU output frequencies - 100, 133, 166 and 200
- High PPM accuracy SRC outputs for SATA and PCI Express interfaces
- -0.5% Spread Spectrum support for EMI reduction
- 96MHz or 100MHz LCD clock support with additional spread spectrum options
- 27MHz clock to support external graphic controller
- 3.3 Volt power supply
- 72 Pin QFN package

Output Summary

- 2 - differential CPU clock outputs @ 0.7V
- 1 - selectable differential CPU/SRC clock output @ 0.7V
- 1 - selectable differential SRC/LCD clock output @ 0.7V
- 9 - differential Serial Reference Clock (SRC) clock outputs @ 0.7V
- 1 - selectable differential 96MHz/27MHz clock output @ 0.7V
- 1 - single-ended 48MHz clock output @ 3.3V
- 5 - single-ended 33MHz clock outputs @ 3.3V
- 2 - single-ended 14.318MHz clock output @ 3.3V

Table 1. CPU Frequency Select Table (FS_C, FS_B, FS_A)

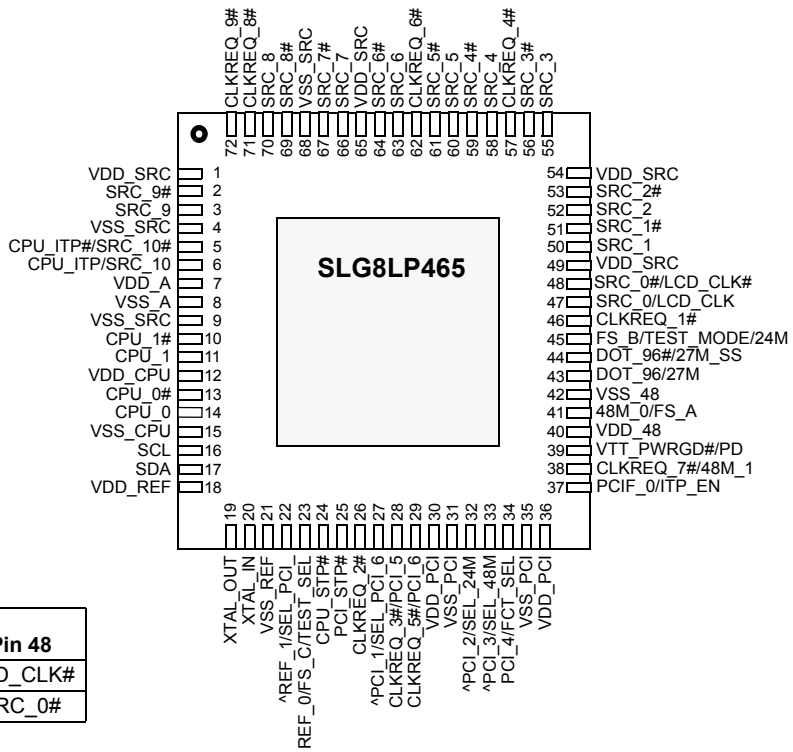
FS_C	FS_B	FS_A	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)
0	0	1	133.3	100.0	33.3	14.318
0	1	0	200.0	100.0	33.3	14.318
0	1	1	166.6	100.0	33.3	14.318
1	0	1	100.0	100.0	33.3	14.318

Table 2. FCT_SEL Input Functional Table

FCT_SEL	Pin 43	Pin 44	Pin 47	Pin 48
0	DOT_96	DOT_96#	LCD_CLK	LCD_CLK#
1	27MHz	27MHz w/ SS	SRC_0	SRC_0#

Pin Configuration

(Top View)



^ This pin has internal pull-down to VSS

72-Pin QFN
10.0x10.0mm body, 0.50mm pitch

Pin Description

Pin #	Name	Type	Description
1	VDD_SRC	PWR	3.3V power supply for outputs.
2	SRC_9#	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
3	SRC_9	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
4	VSS_SRC	GND	Ground for outputs.
5	CPU_ITP#/SRC_10#	O, LP-DIF	Selectable differential CPU or SRC clock output. It will configure as SRC clock when ITP_EN is sampled LOW. It will configure as CPU clock when ITP_EN is sampled HIGH.
6	CPU_ITP/SRC_10	O, LP-DIF	Selectable differential CPU or SRC clock output. It will configure as SRC clock when ITP_EN is sampled LOW. It will configure as CPU clock when ITP_EN is sampled HIGH.
7	VDD_A	PWR	3.3V power supply for PLL.
8	VSS_A	GND	Ground for PLL.
9	VSS_SRC	GND	Ground for outputs.
10	CPU_1#	O, LP-DIF	Differential CPU Clock output. Low voltage output buffer with integrated terminations.
11	CPU_1	O, LP-DIF	Differential CPU Clock output. Low voltage output buffer with integrated terminations.
12	VDD_CPU	PWR	3.3V power supply for outputs.
13	CPU_0#	O, LP-DIF	Differential CPU Clock output. Low voltage output buffer with integrated terminations.
14	CPU_0	O, LP-DIF	Differential CPU Clock output. Low voltage output buffer with integrated terminations.
15	VSS_CPU	GND	Ground for outputs.
16	SCL	I	Serial Interface bus clock input.
17	SDA	I/O, SE	Serial Interface bus data input and output.
18	VDD_REF	PWR	3.3V power supply for outputs.
19	XTAL_OUT	O, SE	14.318MHz crystal output.
20	XTAL_IN	I	14.318MHz crystal input.
21	VSS_REF	GND	Ground for outputs.
22	REF_1/SEL_PCI_5	O, SE	14.318 reference clock output. When SEL_PCI_5 input is sampled HIGH during VTT_PWRGD# assertion, it will configure CLKREQ_3#/PCI_5 as PCI_5 output. When it is sampled LOW, it will configure CLKREQ_3#/PCI_5 as CLKREQ_3# input.
23	REF_0/FS_C/TEST_SEL	I/O, SE	14.318 reference clock output. Frequency Select input to determine CPU output frequency. When FS_C/TEST_SEL input is pulled to 3.3V during VTT_PWRGD# assertion, the device will configure into TEST MODE. Refer to DC Parameters section for FS input voltage threshold.
24	CPU_STP#	I	3.3V tolerant input to disable CPU clock outputs.
25	PCI_STP#	I	3.3V tolerant input to disable PCI and SRC clock outputs.

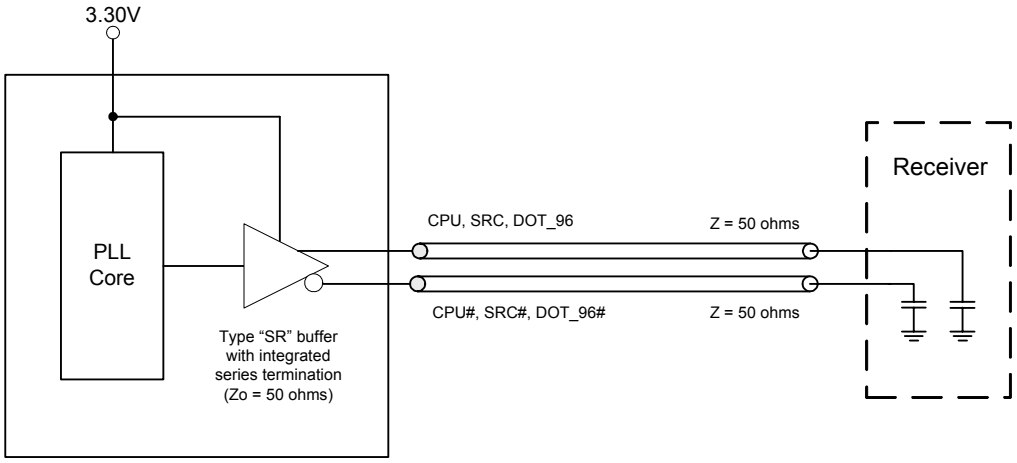
Pin Description (continued)

Pin #	Name	Type	Description
26	CLKREQ_2#	I	3.3V tolerant input to control SRC_2 output.
27	PCI_1/SEL_PCI_6	O, SE	PCI clock output. When SEL_PCI_6 input is sampled HIGH during VTT_PWRGD# assertion, it will configure CLKREQ_5#/PCI_6 as PCI_6 output. When it is sampled LOW, it will configure CLKREQ_5#/PCI_6 as CLKREQ_5# input.
28	CLKREQ_3#/PCI_5	I	Configurable 3.3V tolerant input to control SRC_3 output or PCI clock output.
29	CLKREQ_5#/PCI_6	I	Configurable 3.3V tolerant input to control SRC_5 output or PCI clock output.
30	VDD_PCI	PWR	3.3V power supply for outputs.
31	VSS_PCI	GND	Ground for outputs.
32	PCI_2/SEL_24M	O, SE	PCI clock output. When SEL_24M input is sampled HIGH during VTT_PWRGD# assertion, it will configure FS_B/Test_Mode/24M as 24MHz output. When it is sampled LOW, it will configure FS_B/Test_Mode/24M as FS_B/Test_mode input.
33	PCI_3/SEL_48M	O, SE	PCI clock output. When SEL_48M input is sampled HIGH during VTT_PWRGD# assertion, it will configure CLKREQ_7#/48M_1 as 48MHz output. When it is sampled LOW, it will configure CLKREQ_7#/48M_1 as CLKREQ_7# input.
34	PCI_4/FCT_SEL	I/O, SE	PCI clock output. FCT_SEL input is sampled during VTT_PWRGD# assertion. FCT_SEL controls the output function of pin 43/44 and pin 47/48. Please refer to FCT_SEL functional table for details.
35	VSS_PCI	GND	Ground for outputs.
36	VDD_PCI	PWR	3.3V power supply for outputs.
37	PCIF_0/ITP_EN	I/O, SE	Free running PCI clock output. When ITP_EN input is sampled HIGH during VTT_PWRGD# assertion, it will configure CPU_ITP/SRC_10 as CPU output.
38	CLKREQ_7#/48M_1	I	Configurable 3.3V tolerant input to control SRC_7 output or 48MHz output.
39	VTT_PWRGD#/PD	I	VTT_PWRGD# is a 3.3V LVTTL iput. It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs. After VTT_PWRGD# assertion, it becomes a real time input for asserting power down (active high).
40	VDD_48	PWR	3.3V power supply for outputs.
41	48M_0/FS_A	I/O, SE	USB clock output. Frequency Select input to determine CPU output frequency.
42	VSS_48	GND	Ground for outputs.
43	DOT_96/27M	O, LP-DIF	Selectable 96MHz or 27MHz clock output.
44	DOT_96#/27M_SS	O, LP-DIF	Selectable 96MHz or 27MHz clock output.
45	FS_B/TEST_MODE/24M	I	Frequency Select input to determine CPU output frequency. When in test mode, FS_B/TEST_MODE will configure outputs to run at Ref or Hi-Z. 0 = Hi-Z, 1 = Ref 24MHz output clock.
46	CLKREQ_1#	I	3.3V tolerant input to control SRC_1 output.
47	SRC_0/LCD_CLK	O, LP-DIF	Selectable differential SRC or LCD clock output. It will configure as SRC clock when FCT_SEL is sampled HIGH. It will configure as LCD clock when FCT_SEL is sampled LOW.

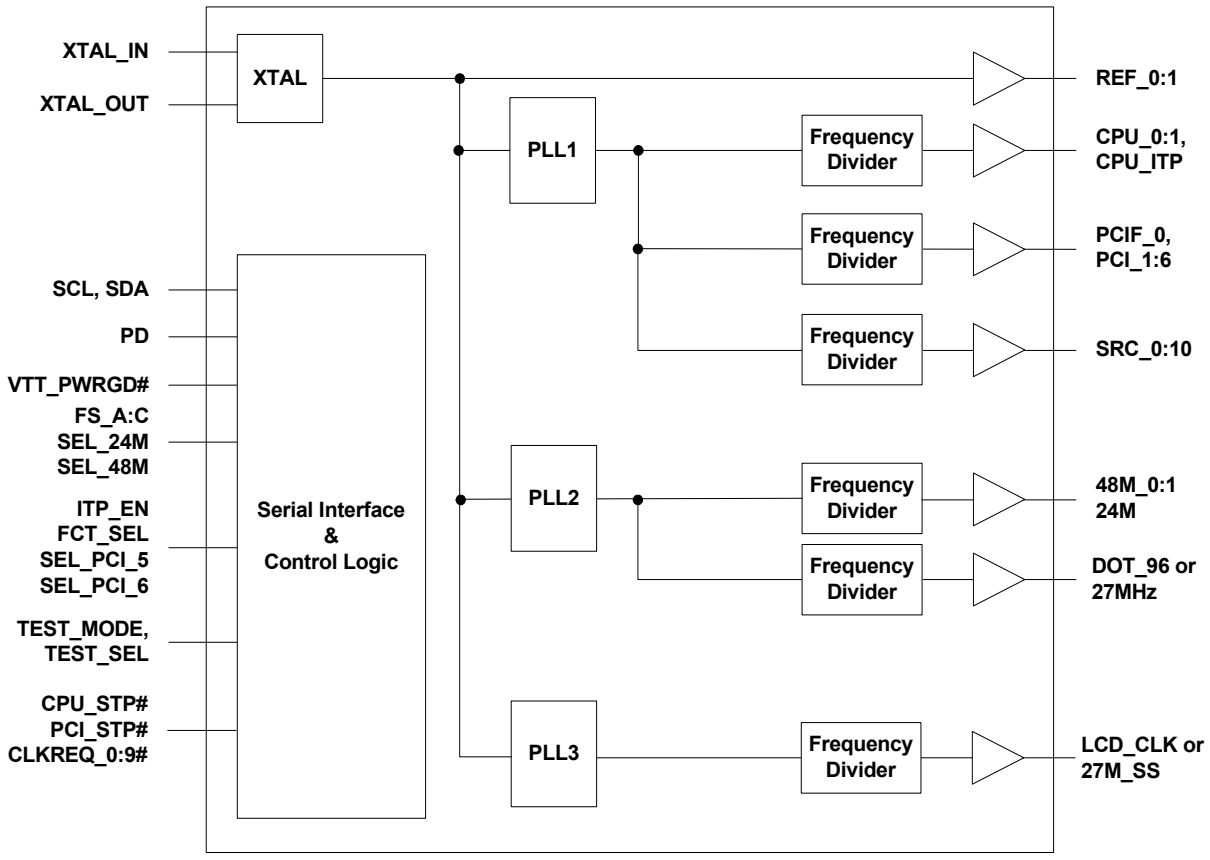
Pin Description (continued)

Pin #	Name	Type	Description
48	SRC_0#/LCD_CLK#	O, LP-DIF	Selectable differential SRC or LCD clock output. It will configure as SRC clock when FCT_SEL is sampled HIGH. It will configure as LCD clock when FCT_SEL is sampled LOW.
49	VDD_SRC	PWR	3.3V power supply for outputs.
50	SRC_1	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
51	SRC_1#	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
52	SRC_2	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
53	SRC_2#	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
54	VDD_SRC	PWR	3.3V power supply for outputs.
55	SRC_3	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
56	SRC_3#	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
57	CLKREQ_4#	I	3.3V tolerant input to control SRC_4 output.
58	SRC_4	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
59	SRC_4#	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
60	SRC_5	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
61	SRC_5#	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
62	CLKREQ_6#	I	3.3V tolerant input to control SRC_6 output.
63	SRC_6	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
64	SRC_6#	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
65	VDD_SRC	PWR	3.3V power supply for outputs.
66	SRC_7	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
67	SRC_7#	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
68	VSS_SRC	GND	Ground for outputs.
69	SRC_8#	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
70	SRC_8	O, LP-DIF	Differential Serial Reference Clock output. Low voltage output buffer with integrated terminations.
71	CLKREQ_8#	I	3.3V tolerant input to control SRC_8 output.
72	CLKREQ_9#	I	3.3V tolerant input to control SRC_9 output.

Low Power differential output buffer with integrated series termination



Block Diagram



Frequency Select Pins (FS_A, FS_B, FS_C)

Host clock frequency selection is achieved by applying the appropriate logic levels to Frequency Select (FS) inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled low by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS input values. VTT_PWRGD# employs a one-shot functionality in that once a valid low on VTT_PWRGD# has been sampled low, all further VTT_PWRGD#, FS input transitions will be ignored. Please refer to Frequency Select Table for different CPU frequency configurations.

FS_C/TEST_SEL Clarification

The FS_C/TEST_SEL input is a three level input. When voltage levels are below Vih min., the frequency selection latched on the assertion of VTT_PWRGD# is determined by Vih_FS and Vil_FS thresholds in the DC Electrical Characteristics section. However, if the voltage level sampled during VTT_PWRGD# assertion is equal or greater than Vih min., the device will invoke test clock operation. Test clock operation is used in bed of nails testing to verify clock functionality. Test clock operation can be invoked in two ways, via writing a logic “1” to the “Test Clock Mode Entry Control” bit in the control register or by placing a logic high equal or greater than Vih min. on the FS_C/TEST_SEL pin prior to the assertion of VTT_PWRGD#. Once test clock operation has been invoked, the device will remain in test clock operation until power is cycled with the voltage on FS_C/TEST_CLK is less than Vih min.

TEST_SEL Hardware Control Via FS_B/TEST_MODE pin

Once test clock operation has been invoked, the FS_B/TEST_MODE pin will select between the Hi-Z and REF mode as shown in the table below using the standard low voltage Vih_FS and Vil_FS thresholds.

Table 3. Test Mode Selection Table

TEST_MODE	CPU	SRC/LCD_CLK	PCIF/PCI	REF	DOT_96/27M	48M
1	REF	REF	REF	REF	REF	REF
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

TEST_CLK Software Control via Control Register bits

When the “Test Clock Mode Entry Control” bit in the control register is set high, the device will invoke test clock operation. Once test clock operation has been invoked via software control, the Test_Mode bit in the control register will select between Hi-Z and REF modes taking priority over the external FS_B/TEST_MODE pin.

PD (Power Down) Clarification

The VTT_PWRGD#/PD pin is a dual function pin. During initial power-up, the pin functions as VTT_PWRGD#. Once VTT_PWRGD# has been sampled low by the device, the pin assumes PD functionality. The PD pin is an asynchronous active high input used to shut off ALL clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. When PD is asserted high, all clocks are driven to a low value and held prior to turning off the VCOs and the crystal oscillator.

Table 4. PD Functionality

PD	CPU	CPU#	SRC/ LCD_CLK	SRC#/ LCD_CLK#	DOT_96	DOT_96#	PCIF/PCI/48M/REF/27M
0	Normal	Normal	Normal	Normal	Normal	Normal	Normal
1	Iref*2 or Float	Float	Iref*2 or Float	Float	Iref*2 or Float	Float	Low

PD# - Assertion

When PD is sampled high by two consecutive rising edges of CPU#, all single-ended outputs will be held low on their next high to low transition and differential clocks will be held high or tristated (depending on the state of the control register drive mode bit) on the next “Diff clock#” high to low transition. When the PD drive mode bit corresponding to the differential (CPU, SRC and DOT_96) clock output of interest is programmed to ‘0’, the clock output will be held with the “Diff clock” pin driven high at 2 x Iref, and “Diff clock#” tristated. If the control register PD drive mode bit corresponding to the output of interest is programmed to ‘1’, then both the “Diff clock” and the “Diff clock#” are tristated.

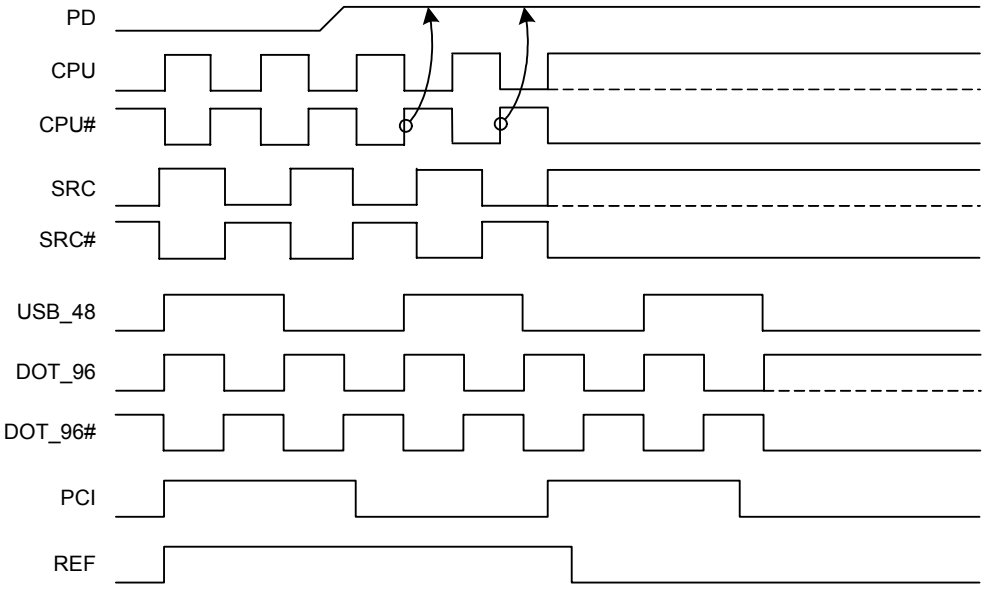


Figure 1. Power Down Assertion

PD De-assertion

The power-up latency is less than 1.8ms. This is the time from the de-assertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock device. All differential outputs stopped in a tristate condition resulting from power down will be driven high in less than 300us of PD de-assertion to voltage greater than 200mV

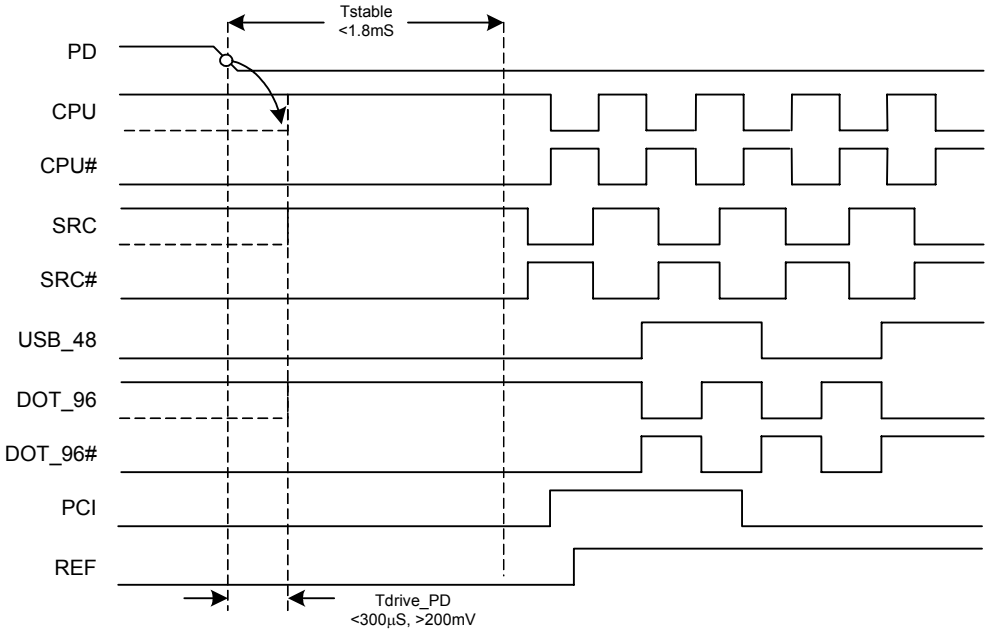


Figure 2. Power Down De-assertion

VTT_PWRGD# Operation

VTT_PWRGD# is an active low signal to indicate when the processor VTT voltage has stabilized. The significance of the VTT supply being stable is that only after VTT is stable are the processor frequency select (FS) and VID bits become valid.

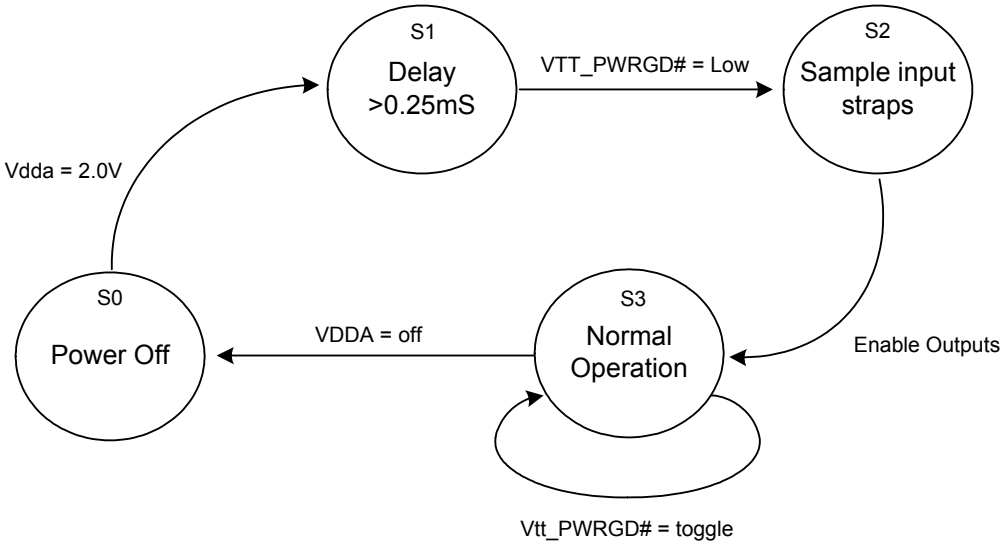


Figure 3. Clock Generator Power Up/Run State Diagram

PCI_STOP# Clarification

The PCI_STOP# signal is an active low input used for cleanly stopping and starting the PCI and SRC outputs while the rest of the clock generator continues to function. The PCIF and SRC clocks are special in that they can be programmed to ignore PCI_STOP# by setting the register bit corresponding output of interest to become free-running. Outputs set to be free-running will ignore both PCI_STOP# pin and the PCI_STOP# register bit.

PCI_STOP Control via Software Control

The purpose of the PCI_STOP# control register bit is to allow system designers to implement PCI_STOP functionality in one of two ways. Either the system designer can choose to use the externally provided PCI_STOP# pin to asssert or de-assert PCI_STOP mode or the system designer can pull the external pin high and use software to control PCI_STOP functionality via SMBus.

Table 5. PCI_STOP# Functionality

PCI_STOP#	CPU	CPU#	SRC	SRC#	PCIF/PCI	DOT_96/ LCD_CLK	DOT_96#/ LCD_CLK#	48M/REF/27M
1	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal
0	Normal	Normal	Iref*6 or Float	Low	Low	Normal	Normal	Normal

PCI_STOP# Assertion (Transition from ‘1’ to ‘0’)

The clock chip will sample the PCI_STOP# signal on a rising edge of PCIF clock. After detecting the PCI_STOP# asserting low, all PCI and stoppable PCIF clocks will latch low on their next high to low transition. After the PCI clocks are latched low, the SRC clocks, (if set to be stoppable) will latch high at Iref*6 (or tristate if the SRC_STOP# drive mode bit in the control register is set high) upon its next low to high transition and SRC# will latch low. The Tsu is the setup time required by the clock generator to correctly sample the PCI_STOP# assertion, this time is 10ns minimum.

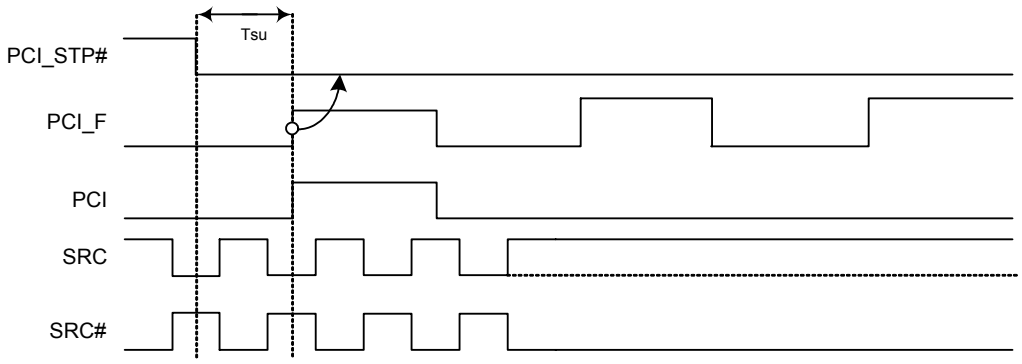


Figure 4. Assertion of PCI_STOP#

PCI_STOP# De-Assertion (Transition from '0' to '1')

The de-assertion of the PCI_STOP# signal is to be sampled on the rising edge of the PCIF free running clock domain. After detecting PCI_STOP# de-assertion, all PCI, stoppable PCIF and stoppable SRC clocks will resume in a glitch free manner. The PCI and SRC clock resume latency will match the one PCI clock latency required for PCI_STOP# entry. If the SRC_STOP drive mode bit is programmed to '1' (tristate), then the stopped SRC clocks will be driven high within 15ns of PCI_STOP# de-assertion. The Tsu is the setup time required by the clock generator to correctly sample the PCI_STOP# de-assertion, this time is 10ns minimum.

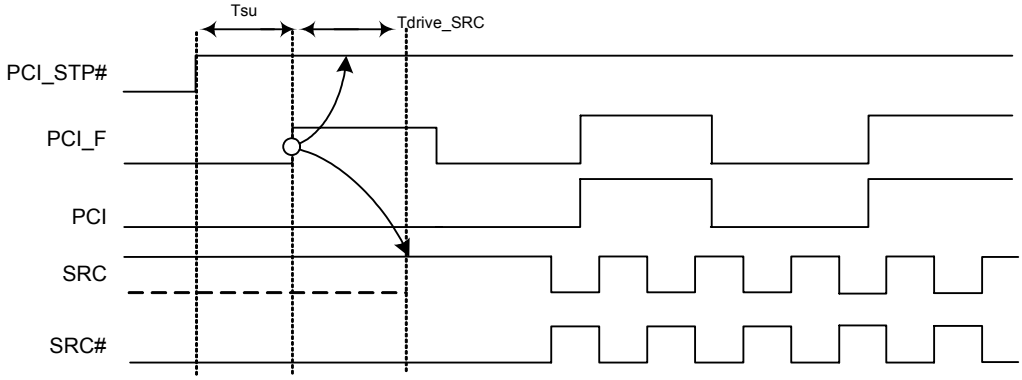


Figure 5. De-Assertion of PCI_STOP#

CPU_STOP# Clarification

The CPU_STOP# signal is an active low asynchronous input used for cleanly stopping and starting the CPU outputs while the rest of the clock generator continues to function.

Table 6. CPU_STOP# Functionality

PCI_STOP#	CPU	CPU#	SRC	SRC#	PCIF/PCI	DOT_96	DOT_96#	48M	REF
1	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal
0	Iref*6 or Float	Low	Normal	Normal	Normal	Normal	Normal	Normal	Normal

CPU_STOP# Assertion (Transition from '1' to '0')

When CPU_STOP# is asserted, all CPU outputs that are set in the control registers to be stoppable are to be stopped after their next transition. When the control register CPU_STOP tristate bit corresponding to the output of interest is programmed to '0', the final state of the stopped CPU signals is "CPU = High" and "CPU# = Low". There will be no change to the output drive current values, CPU will be driven high with a current value equal 6*Iref, and CPU# will not be driven. When the control register CPU_STOP tristate bit corresponding to the output of interest is programmed to '1', the final state of the stopped CPU clock is low, both CPU clock and CPU clock# outputs will not be driven.

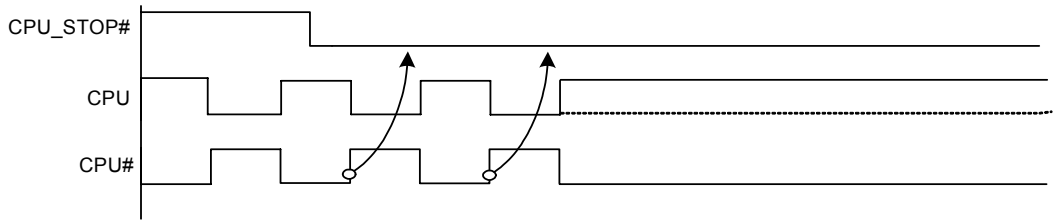


Figure 6. Assertion of CPU_STOP#

CPU_STOP# De-Assertion (Transition from '0' to '1')

All differential outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the de-assertion to active outputs is between 2-6 CPU clock periods. If the control register CPU_STOP# tristate bit corresponding to the output of interest is programmed to '1', then the stopped CPU outputs will be driven high within 10ns of CPU_STOP# de-assertion to a voltage greater than 200mV.

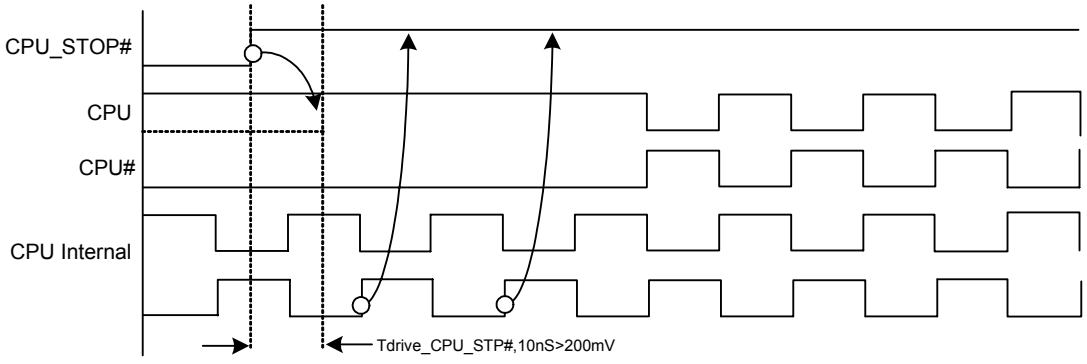


Figure 6. CPU_STOP# De-Assertion

Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 7*. The slave receiver address is 11010010 (D2h).

Table 7. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit '00000000' stands for block operation	11:18	Command Code - 8 Bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop

Table 8. Byte Read and Byte Write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte 0 - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Control Register Summary

Control Register 0

Bit	Type	Description/Function	Power up condition
7	RW	SRC_7 Output Enable 0 = Disabled 1 = Enabled	1
6	RW	SRC_6 Output Enable 0 = Disabled 1 = Enabled	1
5	RW	SRC_5 Output Enable 0 = Disabled 1 = Enabled	1
4	RW	SRC_4 Output Enable 0 = Disabled 1 = Enabled	1
3	RW	SRC_3 Output Enable 0 = Disabled 1 = Enabled	1
2	RW	SRC_2 Output Enable 0 = Disabled 1 = Enabled	1
1	RW	SRC_1 Output Enable 0 = Disabled 1 = Enabled	1
0	RW	SRC_0/LCD_CLK Output Enable 0 = Disabled 1 = Enabled	1

Control Register 1

Bit	Type	Description/Function	Power up condition
7	RW	PCIF_0 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	DOT_96 & 27M Non-spread Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	48M Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	REF_0 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	REF_1 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	CPU_1 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	CPU_0 Output Enabled 0 = Disabled 1 = Enabled	1

Control Register 1 (continued)

Bit	Type	Description/Function	Power up condition
0	RW	CPU, SRC, PCIF & PCI output Spread Spectrum Enable 0 = Disabled 1 = Enabled (-0.5%)	0

Control Register 2

Bit	Type	Description/Function	Power up condition
7	RW	PCI_4 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	PCI_3 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	PCI_2 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	PCI_1 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	PCI_6 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	PCI_5 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	CPU_ITP/SRC_10 Output Enabled 0 = Disabled 1 = Enabled	1
0	RW	Reserved	1

Control Register 3

Bit	Type	Description/Function	Power up condition
7	RW	Allow control of SRC_7 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
6	RW	Allow control of SRC_6 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
5	RW	Allow control of SRC_5 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
4	RW	Allow control of SRC_4 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
3	RW	Allow control of SRC_3 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0

Control Register 3 (continued)

Bit	Type	Description/Function	Power up condition
2	RW	Allow control of SRC_2 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
1	RW	Allow control of SRC_1 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
0	RW	Allow control of SRC_0 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0

Control Register 4

Bit	Type	Description/Function	Power up condition
7	RW	LCD_CLK powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0
6	RW	DOT_96 powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0
5	RW	Reserved	0
4	RW	Reserved	0
3	RW	Allow control of PCIF_0 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
2	RW	Allow control of CPU_ITP with assertion of CPU_STOP# 0 = Free Running 1 = Stopped with CPU_STOP# asserted	1
1	RW	Allow control of CPU_1 with assertion of CPU_STOP# 0 = Free Running 1 = Stopped with CPU_STOP# asserted	1
0	RW	Allow control of CPU_0 with assertion of CPU_STOP# 0 = Free Running 1 = Stopped with CPU_STOP# asserted	1

Control Register 5

Bit	Type	Description/Function	Power up condition
7	RW	SRC STOP drive mode 0 = Driven in PCI_STOP# mode 1 = Tristate in PCI_STOP# mode	0
6	RW	CPU_ITP CPU_STOP# drive mode 0 = Driven in CPU_STOP# mode 1 = Tristate	0
5	RW	CPU_1 CPU_STOP# drive mode 0 = Driven in CPU_STOP# mode 1 = Tristate	0
4	RW	CPU_0 CPU_STOP# drive mode 0 = Driven in CPU_STOP# mode 1 = Tristate	0

Control Register 5 (continued)

Bit	Type	Description/Function	Power up condition
3	RW	SRC_10:0 powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0
2	RW	CPU_ITP powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0
1	RW	CPU_1 powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0
0	RW	CPU_0 powerdown drive mode 0 = Driven in powerdown mode 1 = Tristate	0

Control Register 6

Bit	Type	Description/Function	Power up condition
7	RW	REF or Tristate Select for Test Mode 0 = Tristate 1 = REF	0
6	RW	Test Clock Mode Entry Control 0 = Normal operation 1 = REF or Tristate mode	0
5	RW	REF_1 Output Drive Strength 0 = Low 1 = High	1
4	RW	REF_0 Output Drive Strength 0 = Low 1 = High	1
3	RW	SW PCI_STOP# control 0 = PCI_STOP# asserted, all stoppable PCI and SRC clocks are stopped 1 = PCI_STOP# de-asserted	1
2	R	Reflected the value of FS_C pin sampled on power up	X
1	R	Reflected the value of FS_B pin sampled on power up	X
0	R	Reflected the value of FS_A pin sampled on power up	X

Control Register 7

Bit	Type	Description/Function	Power up condition
7	R	*Revision ID bit 3*	*1*
6	R	Revision ID bit 2	0
5	R	Revision ID bit 1	0
4	R	Revision ID bit 0	0
3	R	Vendor ID bit 3	0
2	R	Vendor ID bit 2	1
1	R	Vendor ID bit 1	1
0	R	Vendor ID bit 0	0

Control Register 8

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	0
4	RW	*SEL_PCI_6 SW Control* *0 = CLKREQ_5#* *1 = PCI_6*	*Latched*
3	RW	*SEL_48M SW Control* *0 = CLKREQ_7#* *1 = 48M_1*	*Latched*
2	RW	*48M_0 Output Drive Strength* *0 = Low* *1 = High*	*1*
1	RW	*48M_1 Output Enable* *0 = Disabled* *1 = Enabled*	*1*
0	RW	PCIF_0 Output Drive Strength 0 = Low 1 = High	1

Control Register 9

Bit	Type	Description/Function	Power up condition
7	RW	*LCD_CLK & 27M_SS spread spectrum % selection*	*0*
6	RW	*LCD_CLK & 27M_SS spread spectrum % selection*	*0*
5:4	RW	LCD_CLK & 27M_SS spread spectrum % selection 00 = -0.5% 01 = -1.0% 10 = -1.5% 11 = -2.0%	00
3	RW	Reserved	1
2	RW	27M_SS Output Enable 0 = Disabled 1 = Enabled	1
1	RW	LCD_CLK & 27M_SS spread spectrum enable 0 = Disabled 1 = Enabled	1
0	RW	Reserved	0

Control Register 10

Bit	Type	Description/Function	Power up condition
7	RW	*SEL_PCI_5 SW Control* *0 = CLKREQ_3#* *1 = PCI_5*	*Latched*
6	RW	*SEL_24M SW Control* *0 = FS_B/Test_Mode* *1 = 24MHz output*	*Latched*

Control Register 10 (continued)

Bit	Type	Description/Function	Power up condition
5	RW	SRC_9 Output Enable 0 = Disabled 1 = Enabled	1
4	RW	SRC_8 Output Enable 0 = Disabled 1 = Enabled	1
3	RW	*24MHz Output Drive Strength* *0 = Low* *1 = High*	*0*
2	RW	Allow control of SRC_10 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
1	RW	Allow control of SRC_9 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0
0	RW	Allow control of SRC_8 with assertion of PCI_STOP# 0 = Free Running 1 = Stopped with PCI_STOP# asserted	0

Control Register 11

Bit	Type	Description/Function	Power up condition
7	RW	Self diagnostic mode enable 0 = Normal Operation (Reset lock and powergood status bit at bit[6:4]and bit[2]) 1= Self Diagnostic Mode Enabled	0
6	R	CPU_PLL Locked Status bit 0 = Never locked 1 = Able to established a lock condition after self diagnostic mode is enabled	X
5	R	27M_LCD_CLK_PLL Locked Status bit 0 = Never locked 1 = Able to established a lock condition after self diagnostic mode is enabled	X
4	R	DOT_48M_PLL Locked Status bit 0 = Never locked 1 = Able to established a lock condition after self diagnostic mode is enabled	X
3	RW	27M & 27M_SS Output Drive Strength 0 = Low 1 = High	0
2	RW	Reserved	1
1	RW	*48M_1 Output Drive Strength* *0 = Low* *1 = High*	*0*
0	RW	*24MHz Output Enable* *0 = Disabled* *1 = Enabled*	*1*

Control Register 12

Bit	Type	Description/Function	Power up condition
7	RW	CLKREQ_9# Enable 0 = Disabled 1 = Enabled	0
6	RW	CLKREQ_8# Enable 0 = Disabled 1 = Enabled	0
5	RW	CLKREQ_7# Enable 0 = Disabled 1 = Enabled	0
4	RW	CLKREQ_6# Enable 0 = Disabled 1 = Enabled	0
3	RW	CLKREQ_5# Enable 0 = Disabled 1 = Enabled	0
2	RW	CLKREQ_4# Enable 0 = Disabled 1 = Enabled	0
1	RW	CLKREQ_3# Enable 0 = Disabled 1 = Enabled	0
0	RW	CLKREQ_2# Enable 0 = Disabled 1 = Enabled	0

Control Register 13

Bit	Type	Description/Function	Power up condition
7	RW	CLKREQ_1# Enable 0 = Disabled 1 = Enabled	0
6	RW	LCD_CLK output frequency 0 = 96MHz 1 = 100MHz	1
5	RW	*PCI_6 Output Drive Strength* *0 = Low* *1 = High*	*1*
4	RW	*PCI_5 Output Drive Strength* *0 = Low* *1 = High*	*1*
3	RW	PCI_4 Output Drive Strength 0 = Low 1 = High	1
2	RW	PCI_3 Output Drive Strength 0 = Low 1 = High	1
1	RW	PCI_2 Output Drive Strength 0 = Low 1 = High	1

Control Register 13 (continued)

Bit	Type	Description/Function	Power up condition
0	RW	PCI_1 Output Drive Strength 0 = Low 1 = High	1

Crystal Recommendations

The SLG8LP465 requires a **Parallel Resonance Crystal.** Substituting a series resonance crystal will cause the SLG8LP465 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 9. Crystal Recommendations.

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Cut Accuracy (max.)	Temp Stability (max.)	Aging (max.)
14.31818MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	35ppm	30ppm	5ppm

Absolute Maximum Ratings

Storage Temperature:–65°C to + 150°C

Supply Voltage (VDDA):-0.5 to 4.6V

Supply Voltage (VDD):-0.5 to 4.6V

3.3V Input Voltage:-0.5 to 4.6V

Operating Temperature (Ambient):0°C to +70°C

ESD Protection (Min):2000V

Lead Frame Material (for Green package): Sn/Bi

Reflow Temperature (for Green package): 260°C (10sec)

DC Electrical Characteristics

Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDDA	3.3V Core Supply Voltage	3.3V±5%	3.135		3.465	V
VDD	3.3V I/O Supply Voltage	3.3V±5%	3.135		3.465	V
Vih	3.3V Input High Voltage	VDD	2.0		VDD+0.3	V
Vil	3.3V Input Low Voltage		VSS-0.3		0.8	V
Vih_FS	3.3V Input High Voltage	VDD	0.7		VDD+0.3	V
Vil_FS	3.3V Input Low Voltage		VSS-0.3		0.35	V
Voh	3.3V Output High Voltage	Ioh = -1mA	2.4			V
Vol	3.3V Output Low Voltage	Iol = 1mA			0.4	V
Iil	Input Leakage Current	0 < Vin < VDD	-5		+5	uA
Cin	Input Pin Capacitance		3		5	pF
Cxtal	Xtal Pin Capacitance		3		5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Idd_ON	Operating Supply Current	VDD = 3.465V All static inputs = VDD or VSS			500	mA
Idd_PD_DR	Powerdown Current	VDD = 3.465V All static inputs = VDD or VSS All differential pairs driven			70	mA
Idd_ON_TRI	Powerdown Current	VDD = 3.465V All static inputs = VDD or VSS All differential pairs tristated			12	mA

AC Electrical Characteristics

Differential Outputs (CPU, SRC, DOT_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Laccurracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average CPU Period (100MHz, SSC disabled)	9.997001	10.003000	ns	Average period over 1 us
Tperiod	Average CPU Period (133MHz, SSC disabled)	7.497751	7.502251	ns	Average period over 1 us
Tperiod	Average CPU Period (166MHz, SSC disabled)	5.998201	6.001801	ns	Average period over 1 us
Tperiod	Average CPU Period (200MHz, SSC disabled)	4.998500	5.001500	ns	Average period over 1 us
Tperiod	Average CPU Period (266MHz, SSC disabled)	3.748875	3.751125	ns	Average period over 1 us
Tperiod	Average CPU Period (333MHz, SSC disabled)	2.999100	3.000900	ns	Average period over 1 us
Tperiod	Average CPU Period (400MHz, SSC disabled)	2.499250	2.500750	ns	Average period over 1 us
Tperiod	Average CPU Period (100MHz, SSC enabled)	9.997001	10.05327	ns	Average period over 1 us
Tperiod	Average CPU Period (133MHz, SSC enabled)	7.497751	7.539950	ns	Average period over 1 us
Tperiod	Average CPU Period (166MHz, SSC enabled)	5.998201	6.031960	ns	Average period over 1 us
Tperiod	Average CPU Period (200MHz, SSC enabled)	4.998500	5.026634	ns	Average period over 1 us
Tperiod	Average CPU Period (266MHz, SSC enabled)	3.748875	3.769975	ns	Average period over 1 us
Tperiod	Average CPU Period (333MHz, SSC enabled)	2.999100	3.015980	ns	Average period over 1 us
Tperiod	Average CPU Period (400MHz, SSC enabled)	2.499250	2.513317	ns	Average period over 1 us
Tperiod	Average SRC Period (100MHz, SSC disabled)	9.997001	10.003000	ns	Average period over 1 us
Tperiod	Average SRC Period (100MHz, SSC enabled)	9.997001	10.05327	ns	Average period over 1 us
Tperiod	Average DOT_96 Period (96MHz)	10.41354	10.41979	ns	Average period over 1 us
Tabs	Absolute Min/Max CPU Period (100, SSC disabled)	9.912001	10.08800	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC disabled)	7.412751	7.587251	ns	
Tabs	Absolute Min/Max CPU Period (166, SSC disabled)	5.913201	6.086801	ns	
Tabs	Absolute Min/Max CPU Period (200, SSC disabled)	4.913500	5.086500	ns	
Tabs	Absolute Min/Max CPU Period (266, SSC disabled)	3.663875	3.836125	ns	
Tabs	Absolute Min/Max CPU Period (333, SSC disabled)	2.914100	3.085900	ns	
Tabs	Absolute Min/Max CPU Period (400, SSC disabled)	2.414250	2.585750	ns	
Tabs	Absolute Min/Max CPU Period (100, SSC enabled)	9.912001	10.13827	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC enabled)	7.412751	7.624950	ns	
Tabs	Absolute Min/Max CPU Period (166, SSC enabled)	5.913201	6.116960	ns	
Tabs	Absolute Min/Max CPU Period (200, SSC enabled)	4.913500	5.111634	ns	
Tabs	Absolute Min/Max CPU Period (266, SSC enabled)	3.663875	3.854975	ns	
Tabs	Absolute Min/Max CPU Period (333, SSC enabled)	2.914100	3.100980	ns	
Tabs	Absolute Min/Max CPU Period (400, SSC enabled)	2.414250	2.598317	ns	
Tabs	Absolute Min/Max SRC Period (100, SSC disabled)	9.872001	10.12800	ns	
Tabs	Absolute Min/Max SRC Period (100, SSC enabled)	9.872001	10.17827	ns	
Tabs	Absolute Min/Max DOT_96 Period (96MHz)	10.16354	10.66979	ns	
Trise	Rise Time	175	700	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system

Differential Outputs (CPU, SRC, DOT_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Tfall	Fall Time	175	700	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Δ Trise	Rise Time Variation		125	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Δ Tfall	Fall Time Variation		125	ps	Measured from 0.175V to 0.525V on test board and measured from 35% to 65% in system
Rise/Fall matching	Rise and Fall Time Matching		20	%	2* (Tr-Tf)/(Tr+Tf)
Vhigh	Voltage High (typ 0.70v)	660	850	mV	Vhigh is defined as the statistical average “high” value as obtained by using the oscilloscope Vhigh Math function
Vlow	Voltage Low (typ 0.0v)	-150		mV	Vhigh is defined as the statistical average “high” value as obtained by using the oscilloscope Vhigh Math function
Vcross Absolute	Absolute Crossing Point Voltage	250	550	mV	
Vcross Relative	Relative Crossing Point Voltage	Calc.	Calc.	mV	For Vhigh < 0.7V, Vcross (rel) Max. = 0.550 - 0.5*(0.7 - Vhavg) For Vhigh > 0.7V, Vcross (rel) Min. = 0.250 + 0.5*(Vhavg - 0.7)
Total Δ Vcross	Total Variation of Vcross over all Edges		140	mV	It is defined as the total variation of all crossing voltages of Rising Clock and Falling Clock#.
Tccjitter	Cycle to Cycle Jitter (CPU)		85	ps	
Tccjitter	Cycle to Cycle Jitter (SRC)		125	ps	
Tccjitter	Cycle to Cycle Jitter (DOT_96)		250	ps	
Duty Cycle	Duty Cycle	45	55	%	
Vovs	Maximum Voltage (Overshoot)		Vhigh + 0.3	V	
Vuds	Minimum Voltage (Undershoot)	-0.3		V	
Vrb	Ringback Voltage		0.2	V	
Tskew	Pin-to-Pin Skew (CPU_0 & CPU_1)		100	ps	
Tskew	Pin-to-Pin Skew (CPU_ITP)		150	ps	
Tskew	Pin-to-Pin Skew (all SRC outputs)		250	ps	

PCI Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period (SSC disabled)	29.99100	30.00900	ns	Average period over 1 us
Tperiod	Average Period (SSC enabled)	29.99100	30.15980	ns	Average period over 1 us
Tabs	Absolute Min/Max Period (SSC disabled)	28.49100	30.50900	ns	
Tabs	Absolute Min/Max Period (SSC enabled)	28.49100	30.65980	ns	
Thigh	CLK high time	12	N/A	ns	
Tlow	CLK low time	12	N/A	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system

PCI Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		500	ps	
Duty Cycle	Duty Cycle	45	55	%	
Tskew	Pin-to-Pin Skew		500	ps	

48M Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period	20.83125	20.83542	ns	Average period over 1 us
Tabs	Absolute Min/Max Period	20.48125	21.18542	ns	
Thigh	CLK high time	8.094	10.036	ns	
Tlow	CLK low time	7.694	9.836	ns	
Edge Rate	Rising edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		350	ps	
Duty Cycle	Duty Cycle	45	55	%	

24M Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		100	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period	41.66250	41.67084	ns	Average period over 1 us
Tabs	Absolute Min/Max Period	40.96250	42.37084	ns	
Thigh	CLK high time	16.188	20.072	ns	
Tlow	CLK low time	15.388	19.672	ns	
Edge Rate	Rising edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		100	ps	
Duty Cycle	Duty Cycle	45	55	%	

REF Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second

REF Timing Characteristics

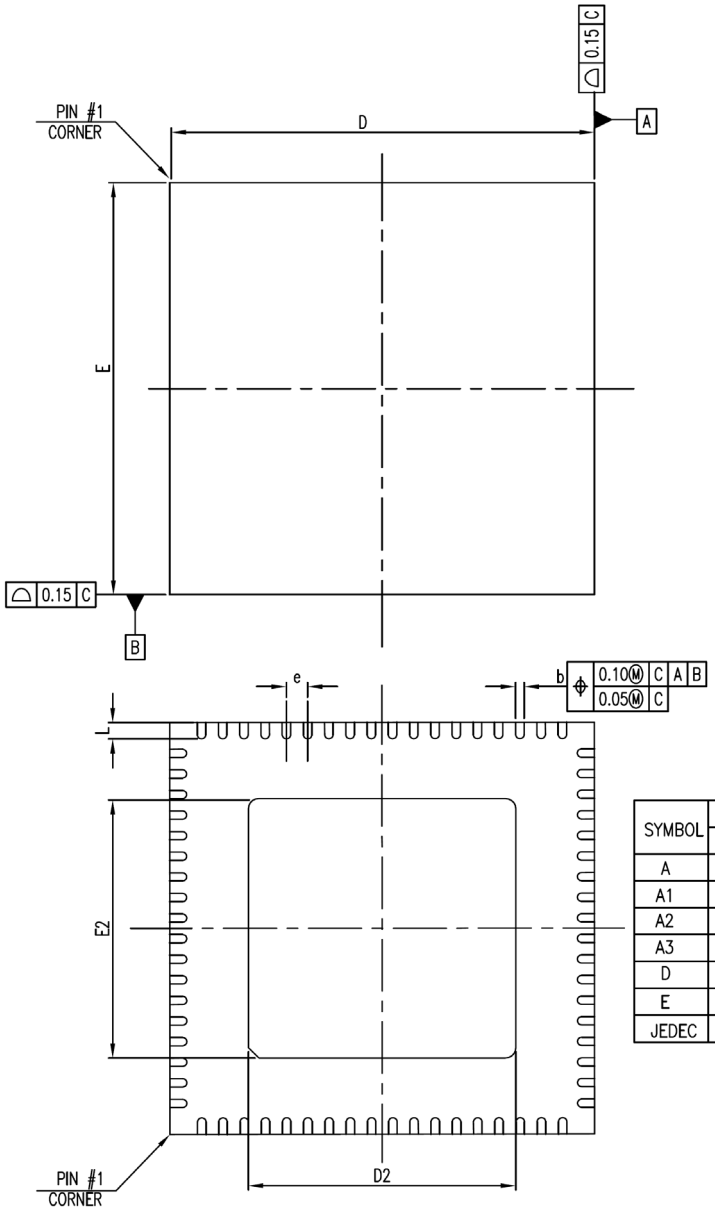
Symbol	Description	Min	Max	Units	Conditions
Tperiod	Average Period	69.82033	69.86224	ns	Average period over 1 us
Tabs	Absolute Min/Max Period	68.82033	70.86224	ns	
Thigh	CLK high time	TBD	TBD	ns	
Tlow	CLK low time	TBD	TBD	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		1000	ps	
Duty Cycle	Duty Cycle	45	55	%	

Ordering Information

Part Number	Package Type	Temperature Range
SLG8LP465V	72-pin QFN	Commercial, 0° to 70°C
SLG8LP465VTR	72-pin QFN - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

72 Pin QFN Package



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.76	0.80	0.84	0.030	0.031	0.033
A1	0.00	0.02	0.04	0.0000	0.0008	0.0015
A2	0.57	0.60	0.63	0.022	0.024	0.025
A3	0.20 REF.			0.008 REF.		
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
JEDEC	MO-220(REF.)					

N	b			D2			E2			e	L			JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
72L	0.15	0.20	0.25	6.25	6.30	6.35	6.25	6.30	6.35	0.500 BSC	0.30	0.40	0.50	