



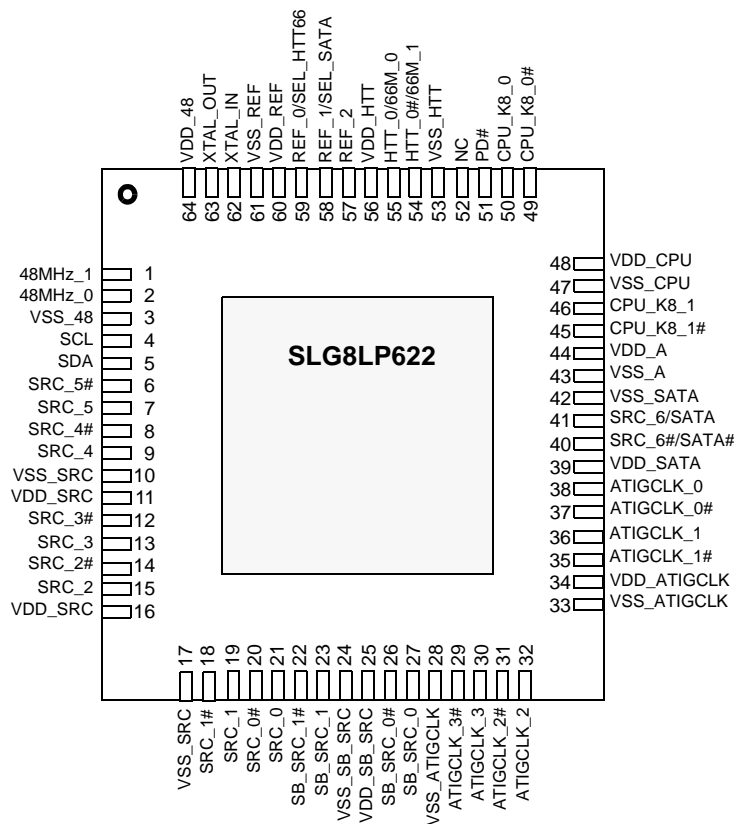
### Features

- Supports AMD 700 series chipset family
- Optimized for desktop application
- High PPM accuracy SRC outputs for PCI Express interfaces
- PCI Express revision 2.0 compliant
- Low Power differential outputs with integrated series termination resistors (50 ohm resistor to GND and 33 ohm series resistor not needed)
- Spread Spectrum support for EMI reduction
- 3.3V Core Power Supply
- 64 pin QFN package

### Output Summary

- 2 - 200MHz AMD K8 CPU clock outputs @ 0.7V
- 6 - differential Serial Reference Clock (SRC) clock outputs @ 0.7V
- 1 - selectable SRC or SATA clock output @ 0.7V
- 4 - differential ATI Graphic clock (SRC) clock outputs @ 0.7V
- 2 - differential Serial Reference Clock (SB\_SRC) clock outputs @ 0.7V
- 1 - HyperTransport 66.6MHz (single-ended) or 100MHz (differential) clock output
- 2 - single-ended 48MHz clock output @ 3.3V
- 3 - single-ended 14.318MHz clock output @ 3.3V

### Pin Configuration (Top View)



Note: Signals with "\*\*\*\*" have internal pull-up resistors



## Pin Description

Pin #	Name	Type	Description
1	48MHz_1	O, SE	USB clock output.
2	48MHz_0	O, SE	USB clock output.
3	VSS_48	GND	Ground for outputs.
4	SCL	I	Serial Interface bus clock input.
5	SDA	I/O, SE	Serial Interface bus data input and output.
6	SRC_5#	O, DIF	Differential Serial Reference Clock output.
7	SRC_5	O, DIF	Differential Serial Reference Clock output.
8	SRC_4#	O, DIF	Differential Serial Reference Clock output.
9	SRC_4	O, DIF	Differential Serial Reference Clock output.
10	VSS_SRC	GND	Ground for outputs.
11	VDD_SRC	PWR	3.3V power supply for outputs.
12	SRC_3#	O, DIF	Differential Serial Reference Clock output.
13	SRC_3	O, DIF	Differential Serial Reference Clock output.
14	SRC_2#	O, DIF	Differential Serial Reference Clock output.
15	SRC_2	O, DIF	Differential Serial Reference Clock output.
16	VDD_SRC	PWR	3.3V power supply for outputs.
17	VSS_SRC	GND	Ground for outputs.
18	SRC_1#	O, DIF	Differential Serial Reference Clock output.
19	SRC_1	O, DIF	Differential Serial Reference Clock output.
20	SRC_0#	O, DIF	Differential Serial Reference Clock output.
21	SRC_0	O, DIF	Differential Serial Reference Clock output.
22	SB_SRC_1#	O, DIF	Differential Serial Reference Clock output.
23	SB_SRC_1	O, DIF	Differential Serial Reference Clock output.
24	VSS_SB_SRC	GND	Ground for outputs.
25	VDD_SB_SRC	PWR	3.3V power supply for outputs.
26	SB_SRC_0#	O, DIF	Differential Serial Reference Clock output.
27	SB_SRC_0	O, DIF	Differential Serial Reference Clock output.
28	VSS_ATIGCLK	PWR	3.3V power supply for outputs.
29	ATIGCLK_3#	O, DIF	Differential ATI graphic clock output.
30	ATIGCLK_3	O, DIF	Differential ATI graphic clock output.
31	ATIGCLK_2#	O, DIF	Differential ATI graphic clock output.
32	ATIGCLK_2	O, DIF	Differential ATI graphic clock output.
33	VSS_ATIGCLK	GND	Ground for outputs.
34	VDD_ATIGCLK	PWR	3.3V power supply for outputs.
35	ATIGCLK_1#	O, DIF	Differential ATI graphic clock output.
36	ATIGCLK_1	O, DIF	Differential ATI graphic clock output.



### Pin Description (continued)

Pin #	Name	Type	Description
37	ATIGCLK_0#	O, DIF	Differential ATI graphic clock output.
38	ATIGCLK_0	O, DIF	Differential ATI graphic clock output.
39	VDD_SATA	PWR	3.3V power supply for outputs.
40	SRC_6#/SATA#	O, DIF	Differential Serial Reference Clock output, recommended reference clock for SATA.
41	SRC_6/SATA	O, DIF	Differential Serial Reference Clock output, recommended reference clock for SATA.
42	VSS_SATA	GND	Ground for outputs.
43	VSS_A	GND	Ground for PLL core.
44	VDD_A	PWR	3.3V power supply for PLL core.
45	CPU_K8_1#	O, SE	K8 CPU Clock output.
46	CPU_K8_1	O, SE	K8 CPU Clock output.
47	VSS_CPU	GND	Ground for outputs.
48	VDD_CPU	PWR	3.3V power supply for outputs.
49	CPU_K8_0#	O, SE	K8 CPU Clock output.
50	CPU_K8_0	O, SE	K8 CPU Clock output.
51	PD#	I	Power down input.
52	NC	NC	No Connect.
53	VSS_HTT	GND	Ground for outputs.
54	HTT_0#/66M_1	O, DIF	Selectable differential (100MHz) or single-ended (66MHz) HTT clock output.
55	HTT_0/66M_0	O, DIF	Selectable differential (100MHz) or single-ended (66MHz) HTT clock output.
56	VDD_HTT	PWR	3.3V power supply for outputs.
57	REF_2	I/O, SE	14.318 reference clock output.
58	REF_1/SEL_SATA	I/O, SE	14.318 reference clock output. 3.3V latched input to configure SRC_6/SATA as normal SRC clock or fixed SATA output. SEL_SATA = 0, configure as normal SRC (SRC_6) output SEL_SATA = 1, configure as SATA output
59	REF_0/SEL_HTT66	I/O, SE	14.318 reference clock output. 3.3V latched input to configure HTT clock as 100MHz differential or single-ended 66MHz clock. SEL_HTT66 = 0, configure as differential 100MHz output SEL_HTT66 = 1, configure as single-ended 66MHz output
60	VDD_REF	PWR	3.3V power supply for outputs.
61	VSS_REF	GND	Ground for outputs.
62	XTAL_IN	I	14.318MHz crystal input.
63	XTAL_OUT	O, SE	14.318MHz crystal output.
64	VDD_48	PWR	3.3V power supply for outputs.



Block Diagram

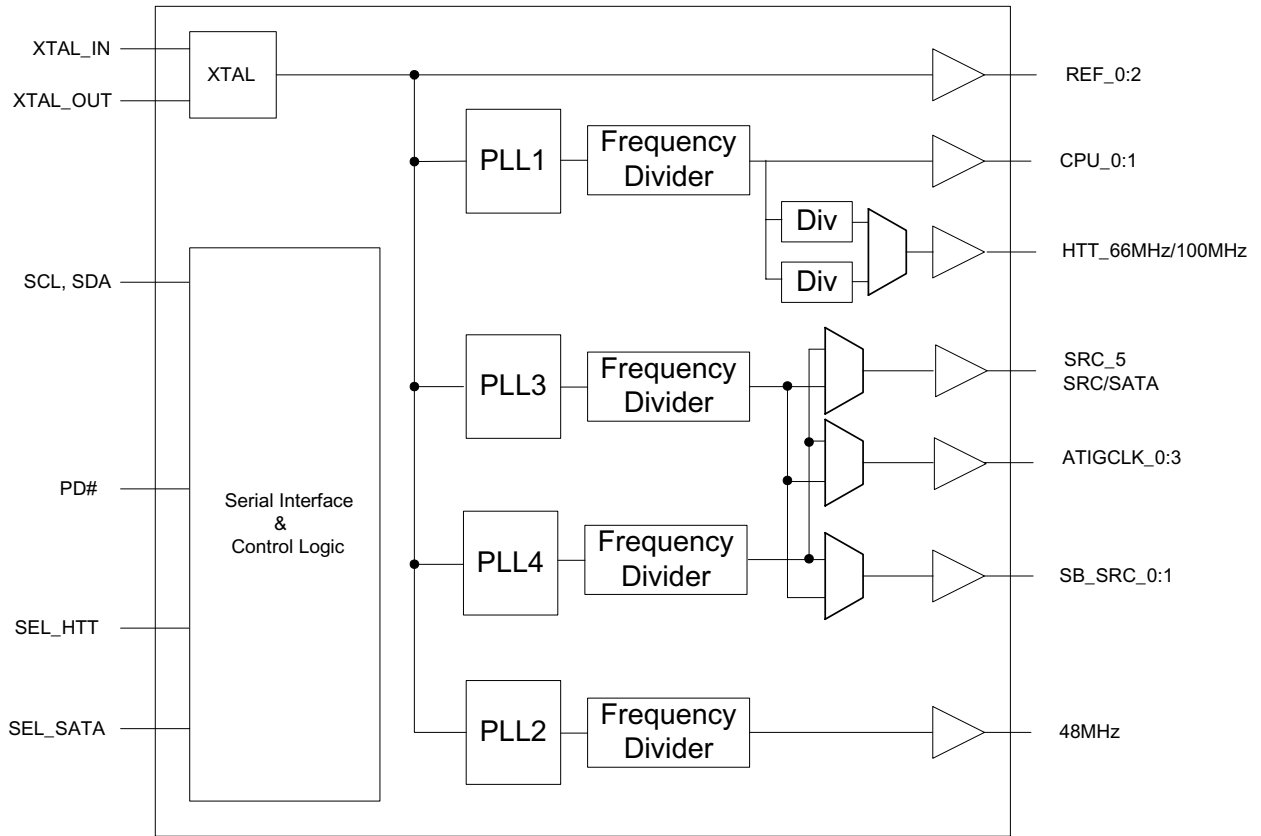




Table 1. PLL 1 (CPU) Frequency Select Table

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CPU (MHz)	SEL_HTT66 =1 (MHz)	SEL_HTT66 =0 (MHz)	Overclock %
0	0	0	0	0	Reserved			
0	0	0	0	1	Reserved			
0	0	0	1	0	Reserved			
0	0	0	1	1	Reserved			
0	0	1	0	0	Reserved			
0	0	1	0	1	Reserved			
0	0	1	1	0	160.18	53.39	80.09	-20%
0	0	1	1	1	164.21	54.74	82.11	-18%
0	1	0	0	0	168.24	56.08	84.12	-16%
0	1	0	0	1	174.06	58.02	87.03	-13%
0	1	0	1	0	178.08	59.36	89.04	-11%
0	1	0	1	1	182.11	60.70	91.05	-9%
0	1	1	0	0	186.14	62.05	93.07	-7%
0	1	1	0	1	191.95	63.98	95.98	-4%
0	1	1	1	0	195.98	65.33	97.99	-2%
0	1	1	1	1	200.01	66.67	100.00	0%
1	0	0	0	0	200.01	66.67	100.00	0%
1	0	0	0	1	206.27	68.76	103.14	3%
1	0	0	1	0	212.09	70.70	106.04	6%
1	0	0	1	1	218.35	72.78	109.18	9%
1	0	1	0	0	226.41	75.47	113.20	13%
1	0	1	0	1	232.22	77.41	116.11	16%
1	0	1	1	0	238.04	79.35	119.02	19%
1	0	1	1	1	244.30	81.43	122.15	22%
1	1	0	0	0	250.12	83.37	125.06	25%
1	1	0	0	1	256.38	85.46	128.19	28%
1	1	0	1	0	262.20	87.40	131.10	31%
1	1	0	1	1	268.02	89.34	134.01	34%
1	1	1	0	0	276.07	92.02	138.04	38%
1	1	1	0	1	281.89	93.96	140.94	41%
1	1	1	1	0	288.15	96.05	144.08	44%
1	1	1	1	1	293.97	97.99	146.99	47%



Table 2. PLL 3 (ATIGCLK, SRC, SB\_SRC) Frequency Select Table

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ATIGCLK (MHz)	SRC (MHz)	SB_SRC (MHz)	Overclock %
0	0	0	0	0	Reserved			
0	0	0	0	1	Reserved			
0	0	0	1	0	Reserved			
0	0	0	1	1	Reserved			
0	0	1	0	0	Reserved			
0	0	1	0	1	Reserved			
0	0	1	1	0	Reserved			
0	0	1	1	1	Reserved			
0	1	0	0	0	Reserved			
0	1	0	0	1	Reserved			
0	1	0	1	0	Reserved			
0	1	0	1	1	Reserved			
0	1	1	0	0	Reserved			
0	1	1	0	1	97.99	97.99	97.99	-2%
0	1	1	1	0	98.88	98.88	98.88	-1%
0	1	1	1	1	100.00	100.00	100.00	0%
1	0	0	0	0	100.00	100.00	100.00	0%
1	0	0	0	1	101.12	101.12	101.12	1%
1	0	0	1	0	102.02	102.02	102.02	2%
1	0	0	1	1	103.14	103.14	103.14	3%
1	0	1	0	0	103.14	103.14	103.14	3%
1	0	1	0	1	104.03	104.03	104.03	4%
1	0	1	1	0	105.15	105.15	105.15	5%
1	0	1	1	1	106.04	106.04	106.04	6%
1	1	0	0	0	107.16	107.16	107.16	7%
1	1	0	0	1	108.06	108.06	108.06	8%
1	1	0	1	0	108.95	108.95	108.95	9%
1	1	0	1	1	110.07	110.07	110.07	10%
1	1	1	0	0	110.07	110.07	110.07	10%
1	1	1	0	1	110.97	110.97	110.97	11%
1	1	1	1	0	Reserved			
1	1	1	1	1	Reserved			



Table 3. PLL 4 Frequency Select Table

Bit 4	Bit 3	Bit 2	Bit 1	ATIGCLK (MHz)	SRC (MHz)	SB_SRC (MHz)	Overclock %
0	0	0	0	Reserved			
0	0	0	1	Reserved			
0	0	1	0	Reserved			
0	0	1	1	Reserved			
0	1	0	0	87.10	87.10	87.10	-13%
0	1	0	1	91.16	91.16	91.16	-9%
0	1	1	0	95.93	95.93	95.93	-4%
0	1	1	1	99.99	99.99	99.99	0%
1	0	0	0	106.19	106.19	106.19	6%
1	0	0	1	113.11	113.11	113.11	13%
1	0	1	0	119.08	119.08	119.08	19%
1	0	1	1	125.05	125.05	125.05	25%
1	1	0	0	131.25	131.25	131.25	31%
1	1	0	1	138.17	138.17	138.17	38%
1	1	1	0	Reserved			
1	1	1	1	Reserved			



## Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 4*. The slave receiver address is 11010010 (D2h).

**Table 4. Block Read and Block Write protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit '00000000' stands for block operation	11:18	Command Code - 8 Bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop





Table 5. Byte Read and Byte Write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxx' stands for byte operationbit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxx' stands for byte operationbit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte 0 - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop



## Control Register Summary

### Control Register 0

Bit	Type	Description/Function	Power up condition
7	R	SEL_HTT66 input status 0 = 100MHz differential HTT clock 1 = 66MHz single-ended HTT clock	Latched status of SEL_HTT66 input
6	R	SEL_SATA input status 0 = SRC_6 1 = SATA	Latched status of SEL_SATA input
5	RW	REF_0 Output Enable 0 = Disabled 1 = Enabled	1
4	RW	REF_1 Output Enable 0 = Disabled 1 = Enabled	1
3	RW	REF_2 Output Enable 0 = Disabled 1 = Enabled	1
2	RW	48MHz_1 Output Enable 0 = Disabled 1 = Enabled	1
1	RW	48MHz_0 Output Enable 0 = Disabled 1 = Enabled	1
0	RW	PLL1 (CPU_K8_0, CPU_K8_1, HTT_0) Spread Spectrum Enable 0 = Spread Spectrum off 1 = Spread Spectrum on	0

### Control Register 1

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	1
6	RW	SRC_6/SATA Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	SRC_5 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	SRC_4 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	SRC_3 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	SRC_2 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	SRC_1 Output Enabled 0 = Disabled 1 = Enabled	1



### Control Register 1 (continued)

Bit	Type	Description/Function	Power up condition
0	RW	SRC_0 Output Enabled 0 = Disabled 1 = Enabled	1

### Control Register 2

Bit	Type	Description/Function	Power up condition
7	RW	SB_SRC_1 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	SB_SRC_0 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	ATIGCLK_3 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	ATIGCLK_2 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	ATIGCLK_1 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	ATIGCLK_0 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	48MHz_1 Drive Strength select 0 = 1 Load 1 = 2 Load	1
0	RW	48MHz_0 Drive Strength select 0 = 1 Load 1 = 2 Load	1

### Control Register 3

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	0
4:0	RW	PLL1 (CPU_K8_0, CPU_K8_1, HTT_0) FS_4:0 Frequency Select inputs <i>See Frequency Select Table</i>	01111

### Control Register 4

Bit	Type	Description/Function	Power up condition
7	RW	REF_0 Drive Strength select 0 = 1 Load 1 = 2 Load	1



### Control Register 4 (continued)

Bit	Type	Description/Function	Power up condition
6	RW	REF_1 Drive Strength select 0 = 1 Load 1 = 2 Load	1
5	RW	REF_2 Drive Strength select 0 = 1 Load 1 = 2 Load	1
4:0	RW	PLL3 (SB_SRC PLL) FS_4:0 Frequency Select inputs <i>See Frequency Select Table</i>	01111

### Control Register 5

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	00001111

### Control Register 6

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	0
4:1	RW	PLL4 FS_4:1 Frequency Select inputs <i>See Frequency Select Table</i>	0111
0	RW	Reserved	1

### Control Register 7

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	1
5	RW	Reserved	1
4	RW	Reserved	1
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

### Control Register 8

Bit	Type	Description/Function	Power up condition
7	R	Revision ID bit 3	0
6	R	Revision ID bit 2	0
5	R	Revision ID bit 1	0
4	R	Revision ID bit 0	0
3	R	Vendor ID bit 3	0



### Control Register 8 (continued)

Bit	Type	Description/Function	Power up condition
2	R	Vendor ID bit 2	1
1	R	Vendor ID bit 1	1
0	R	Vendor ID bit 0	0

### Control Register 9

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	X
4	RW	Reserved	X
3	RW	Reserved	0
2	RW	Reserved	1
1	RW	Reserved	1
0	RW	Reserved	1

### Control Register 10

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	1
6	RW	Reserved	1
5	RW	Reserved	1
4	RW	Reserved	0
3	RW	Reserved	1
2	RW	Reserved	1
1	RW	Reserved	1
0	RW	Reserved	1

### Control Register 11

Bit	Type	Description/Function	Power up condition
7:6	RW	Reserved	00
5:0	RW	Byte Count register for block read operation Note: The default value is 15. To read more than 15 bytes, system BIOS needs to change this register to the number of bytes it intends to read.	001111

### Control Register 12

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	0
4	RW	Reserved	0



### Control Register 12

Bit	Type	Description/Function	Power up condition
3	RW	Reserved	0
2:0	RW	Differential Output Voltage Control 000 = 0.3V 001 = 0.4V 010 = 0.5V 011 = 0.6V 100 = 0.7V 101 = 0.8V 110 = 0.9V 111 = 1.0V	101

### Control Register 13

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	00000000

### Control Register 14

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	00000000

### Control Register 15

Bit	Type	Description/Function	Power up condition
7	RW	Test Mode Enable 0 = Normal 1 = All outputs are REF clock	0
6:0	RW	Reserved	00000000

### Control Register 16

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	00000000

### Control Register 17

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	00000000

### Control Register 18

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	1
6	RW	PLL1 (CPU_K8_0, CPU_K8_1, HTT_0) Spread Spectrum control 0 = Down Spread 1 = Center Spread	0
5:4	RW	Reserved	00
3	RW	Reserved	0



### Control Register 18

Bit	Type	Description/Function	Power up condition
2	RW	ATIGCLK PLL source selection 0 = PLL 3 1 = PLL 4	0
1	RW	SRC PLL source selection 0 = PLL 3 1 = PLL 4	0
0	RW	SB_SRC PLL source selection 0 = PLL 3 1 = PLL 4	0

### Control Register 19

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	00000000

### Control Register 20

Bit	Type	Description/Function	Power up condition
7	RW	PLL3 (SRC/ATIGCLK/SB_SRC PLL) Spread Spectrum Enable 0 = Spread Spectrum OFF 1 = Spread Spectrum ON	0
6	RW	PLL3 (SRC/ATIGCLK/SB_SRC PLL) Spread Spectrum control 0 = Down Spread 1 = Center Spread	0
5:4	RW	PLL3 (SRC/ATIGCLK/SB_SRC PLL) Spread Spectrum Magnitude 00 = 0.5% 01 = Reserved 10 = 0.3% 11 = Reserved	00
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

### Control Register 21

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	0

### Control Register 22

Bit	Type	Description/Function	Power up condition
7	RW	PLL4 Spread Spectrum Enable 0 = Spread Spectrum OFF 1 = Spread Spectrum ON	0
6	RW	PLL4 Spread Spectrum control 0 = Down Spread 1 = Center Spread	0
5:4	RW	Reserved	00



**Control Register 22**

Bit	Type	Description/Function	Power up condition
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

**Control Register 23 to 28 (Reserved)**

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	00000000





## Crystal Recommendations

The SLG8LP622 requires a **Parallel Resonance Crystal**. Substituting a series resonance crystal will cause the SLG8LP622 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

**Table 6. Crystal Recommendations.**

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Cut Accuracy (max.)	Temp Stability (max.)	Aging (max.)
14.31818MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	35ppm	30ppm	5ppm

## Absolute Maximum Ratings

Storage Temperature: -65°C to +150°C

Supply Voltage (VDDA): -0.5 to 4.6V

Supply Voltage (VDD): -0.5 to 4.6V

3.3V Input Voltage: -0.5 to 4.6V

Operating Temperature (Ambient): 0°C to +70°C

ESD Protection (Min): 2000V

Lead Frame Material (for Green package): Sn/Bi

Reflow Temperature (for Green package): 260°C (10sec)

## DC Electrical Characteristics

### Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDDA	3.3V Core Supply Voltage	3.3V±5%	3.135		3.465	V
VDD	3.3V I/O Supply Voltage	3.3V±5%	3.135		3.465	V
Vih	3.3V Input High Voltage	VDD	2.0		VDD+0.3	V
Vil	3.3V Input Low Voltage		VSS-0.3		0.8	V
Voh	3.3V Output High Voltage	Ioh = -1mA	2.4			V
Vol	3.3V Output Low Voltage	Iol = 1mA			0.4	V
Iil	Input Leakage Current	0 < Vin < VDD	-5		+5	uA
Cin	Input Pin Capacitance		3		5	pF
Cxtal	Xtal Pin Capacitance		3		5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Idd_ON	Operating Supply Current	VDD = 3.465V All static inputs = VDD or VSS			180	mA



## AC Electrical Characteristics

### Differential Outputs (CPU, HTT100) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Trise	Rise edge rate	0.5	10	V/ns	Measured at CPU test load. 0V +/- 100mV (differential measurement)
Tfall	Fall edge rate	0.5	10	V/ns	Measured at CPU test load. 0V +/- 100mV (differential measurement)
Vdiff (pk-pk)	Differential Voltage (peak to peak)	0.40	2.40	V	Measured at CPU test load (single ended measurement)
Vdiff	Differential Voltage	0.20	1.20	V	Measured at CPU test load (single ended measurement)
Δ Vdiff	Change in Vdiff_dc magnitude	-75	+75	mV	Measured at CPU test load (single ended measurement)
Δ Vcross	Change in crossing point voltage		140	mV	Measured at CPU test load (single ended measurement)
Δ Vcm	Change in common mode voltage	-200	+200	mV	Measured at CPU test load (single ended measurement)
Tccjitter	Cycle to Cycle Jitter	0	150	ps	Measured at differential cross point
Duty Cycle	Duty Cycle	45	55	%	
Tja	Accumulated jitter	-1000	1000	ps	Measured using JIT2 software package with a Tek7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50ps Sample duration = 10us
Tfs	Frequency stabilization from power up	0	3	ms	Measured from full supply voltage

### Differential Outputs (ATI\_GCLK, SRC) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tab	Absolute Min/Max Period (100, SSC disabled)	9.872001	10.12800	ns	
Tab	Absolute Min/Max Period (100, SSC enabled)	9.872001	10.17827	ns	
Slew_rise	Rising slew rate	2.5	8.0	V/ns	1. Use 'average' acquisition mode of the scope 2. Measurement taken from differential waveform 3. Slew rate measured through V_swing voltage range centered about differential zero
Slew_fall	Falling slew rate	2.5	8.0	V/ns	1. Use 'average' acquisition mode of the scope 2. Measurement taken from differential waveform 3. Slew rate measured through V_swing voltage range centered about differential zero
Slew_var	Slew rate matching		20	%	1. Use 'average' acquisition mode of the scope 2. Measurement taken from single ended waveform 3. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculation
V_swing	Differential output swing	300		mV	Measurement taken from differential waveform
V_cr	Crossing point voltage	300	550	mV	1. Measurement taken from single ended waveform 2. V_cross is defined as the voltage where Clock = Clock# 3. Only applies to the differential rising edge (i.e. Clock rising and Clock# falling)



### Differential Outputs (ATI\_GCLK, SRC) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
V_cr_dlt	Variation of V_cr		140	mV	1. Measurement taken from single ended waveform 2. V_cross is defined as the voltage where Clock = Clock# 3. V_cross delta is defined as the total variation of all crossing voltages of rising Clock and falling Clock#
Tccjitter	Cycle to Cycle Jitter (SRC)		125	ps	
Duty Cycle	Duty Cycle	45	55	%	
Tskew	Pin-to-Pin Skew (all SRC outputs)		3	ns	

### PCI Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period (SSC disabled)	29.99100	30.00900	ns	Average period over 1 us
Tperiod	Average Period (SSC enabled)	29.99100	30.15980	ns	Average period over 1 us
Tabs	Absolute Min/Max Period (SSC disabled)	28.49100	30.50900	ns	
Tabs	Absolute Min/Max Period (SSC enabled)	28.49100	30.65980	ns	
Thigh	CLK high time	12	N/A	ns	
Tlow	CLK low time	12	N/A	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		500	ps	
Duty Cycle	Duty Cycle	45	55	%	
Tskew	Pin-to-Pin Skew		500	ps	

### HTTCLK (66.6MHz) Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Thigh	CLK high time	5	N/A	ns	
Tlow	CLK low time	5	N/A	ns	
Trise	Rise Time		1.5	ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tfall	Fall Time		1.5	ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		300	ps	
Duty Cycle	Duty Cycle	45	55	%	
Tlong-term-jitter	Long term jitter		1	ns	1us sample period



### USB\_48 Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		100	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period	20.83125	20.83542	ns	Average period over 1 us
Tab	Absolute Min/Max Period	20.48125	21.18542	ns	
Thigh	CLK high time	8.094	10.036	ns	
Tlow	CLK low time	7.694	9.836	ns	
Edge Rate	Rising edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		130	ps	
Duty Cycle	Duty Cycle	45	55	%	

Note: USB clock is measured with AMD recommended test settings

### REF Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccuracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average Period	69.82033	69.86224	ns	Average period over 1 us
Tab	Absolute Min/Max Period	68.82033	70.86224	ns	
Trise	Rise Time		1.5	ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tfall	Fall Time		1.5	ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		200	ps	
Duty Cycle	Duty Cycle	45	55	%	
Tlong-term-jitter	Long term jitter		200	ps	1us sample period (LTJ performance depends on the quality of the Xtal being used)
Tlong-term-jitter	Long term jitter		300	ps	10us sample period (LTJ performance depends on the quality of the Xtal being used)



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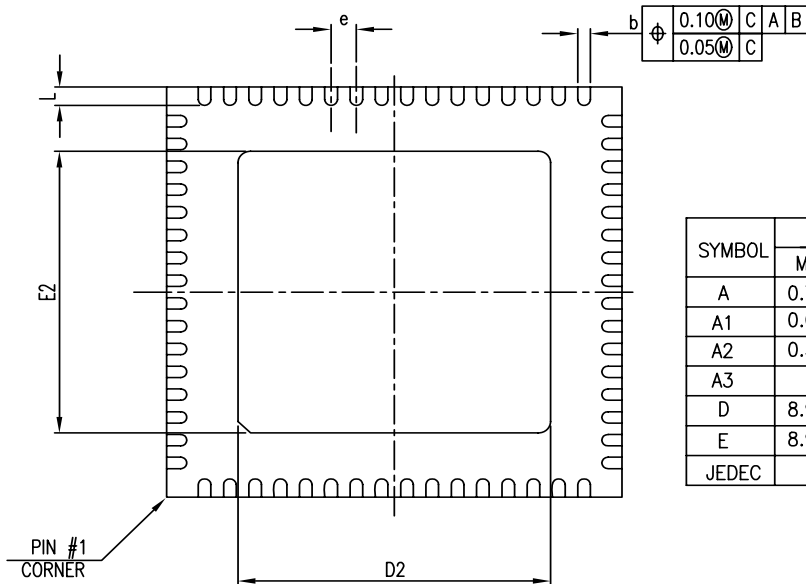
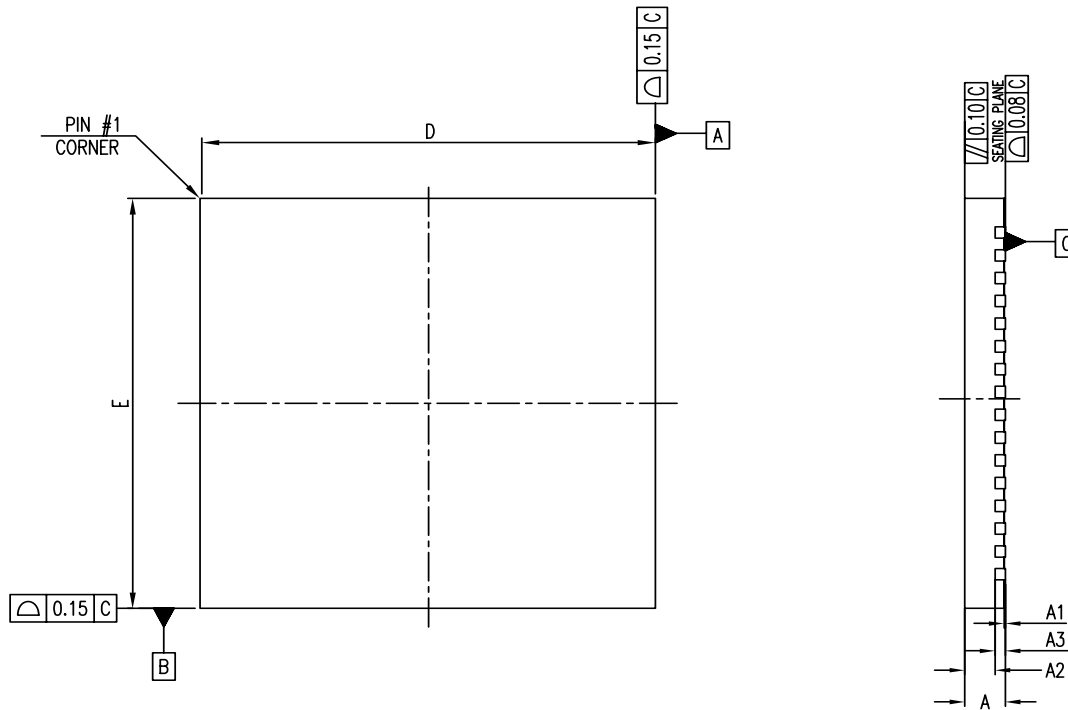
## Ordering Information

Part Number	Package Type	Temperature Range
SLG8LP622V	64 Lead Green Package QFN	Commercial, 0° to 70°C
SLG8LP622VTR	64 Lead Green Package QFN - Tape and Reel	Commercial, 0° to 70°C



Package Drawing and Dimensions

64 Lead TSSOP Package



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.76	0.80	0.84	0.030	0.031	0.033
A1	0.00	0.02	0.05	0.000	0.0008	0.0020
A2	0.57	0.60	0.63	0.022	0.024	0.025
A3	0.20 REF.			0.008 REF.		
D	8.90	9.00	9.10	0.350	0.354	0.358
E	8.90	9.00	9.10	0.350	0.354	0.358
JEDEC	MO-220(REF.)					

N	b			D2			E2			e	L			JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
64L	0.20	0.25	0.30	6.13	6.18	6.23	6.13	6.18	6.23	0.500 BSC	0.35	0.40	0.45	MO-220WMMD